# Update on SVT activities

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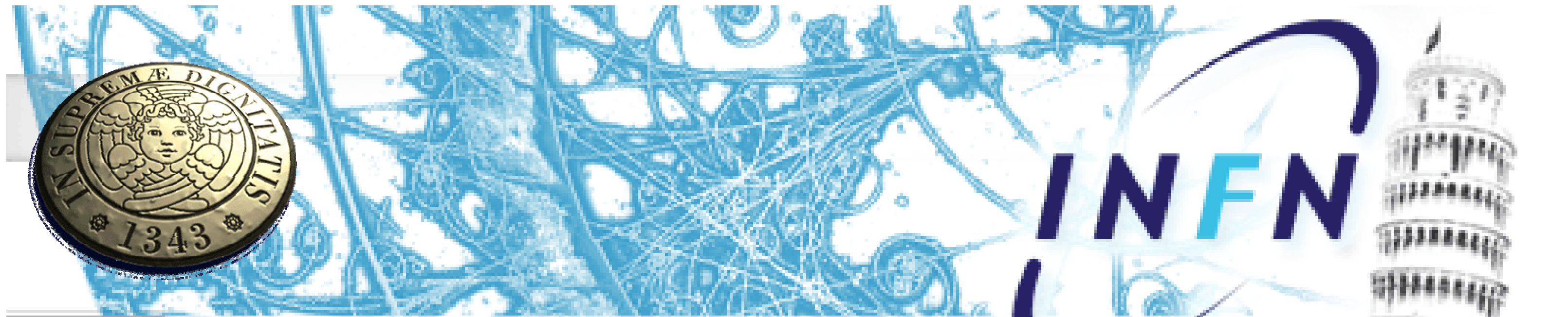
Universita' di Pisa & INFN

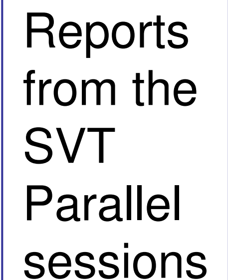
on behalf of the SuperB SVT Group



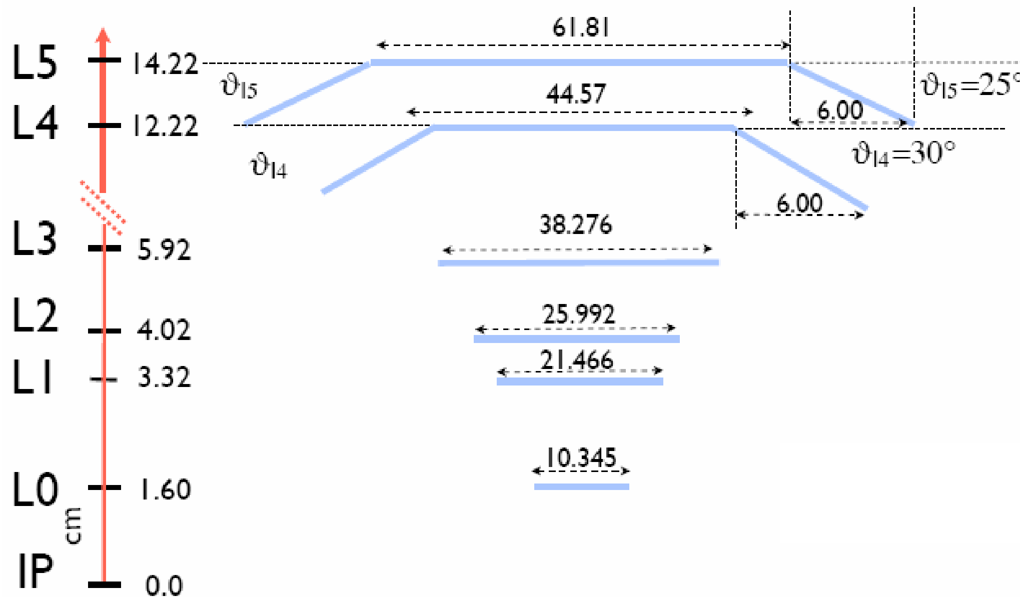

*SuperB Workshop XII – Annecy - March 17, 2010*

# Outline

- Introduction:
  – General concept and the SVT baseline
- Striplets, FSSR2 and a new test-stand
- Progress in R&D activities on pixels:
  – Pixel Front End in vertical integration technology
  – Pixel Layer0 read-out architecture
  – Aluminum bus & HDI
  – Mechanics: Layer0 support/cooling
- UK Activities on pixels
- Bkg estimate update: rad. Bhabha
- Conclusions



# SVT TDR Baseline: L0 + L1→5




**Striplet Layer0**: baseline option for TDR

better physics performance

- Lower material:0.5 % $X_0$

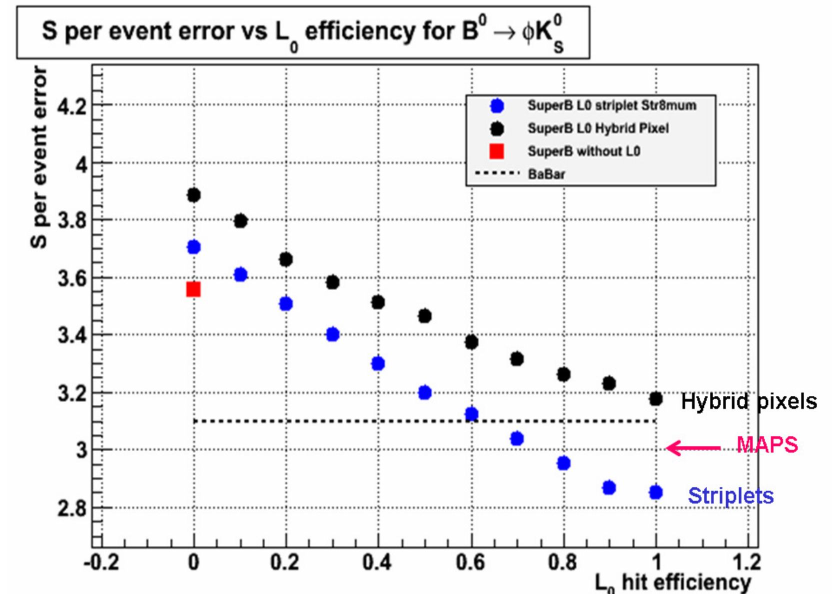
Critical point of this option: inefficiency evaluation in high occupancy conditions.

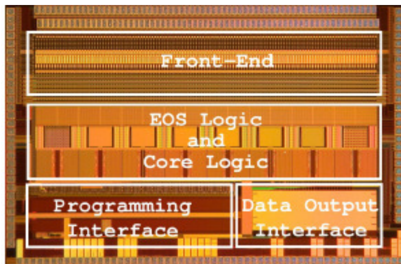
Upgrade to Pixels (Hybrid or CMOS MAPS) more robust against background, foreseen for a second generation of L0. SVT mechanics to be designed for a rapid (days) replacement of the L0.

Coverage: down to 300 mrad (BW&FW)
L0 required for maintaining adequate proper time resolution for time-dependent measurements.

**Layer1-5 strip detector**:

Readout chip evaluation:FSSR2
Analog sect. of FE requires modification for matching both external layers (long strip) and L0 (short strip, high occupancy).



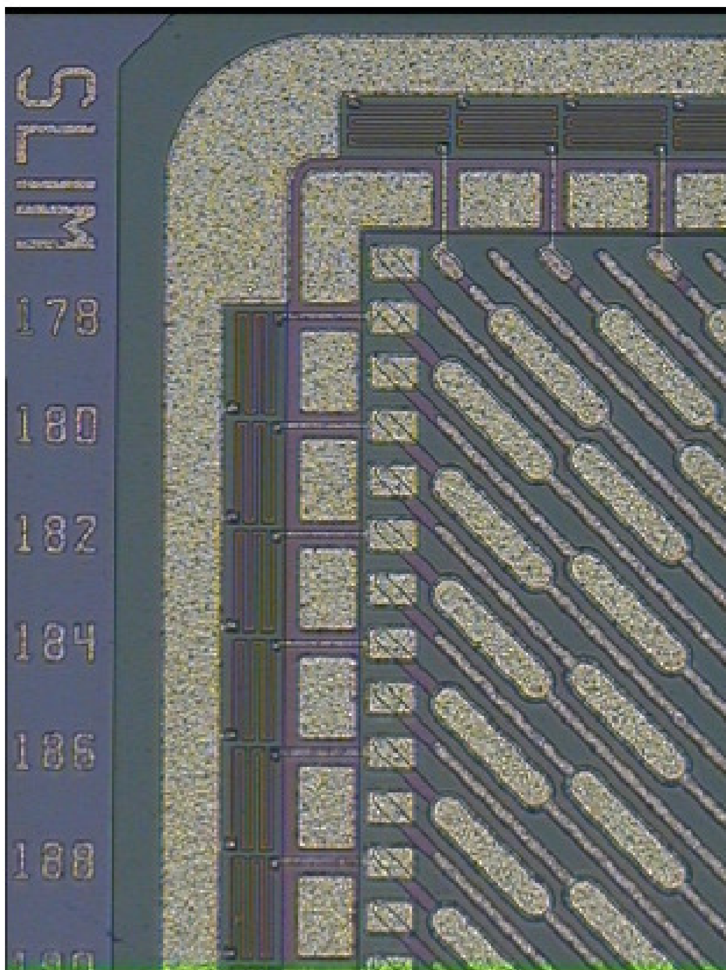



# The Striplet sensor

←read out by the FSSR2 chip

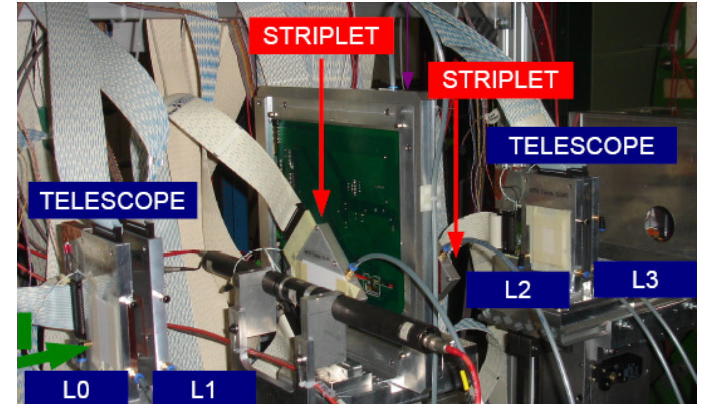
M.Bomben

Designed sensor for L0 & inner layers

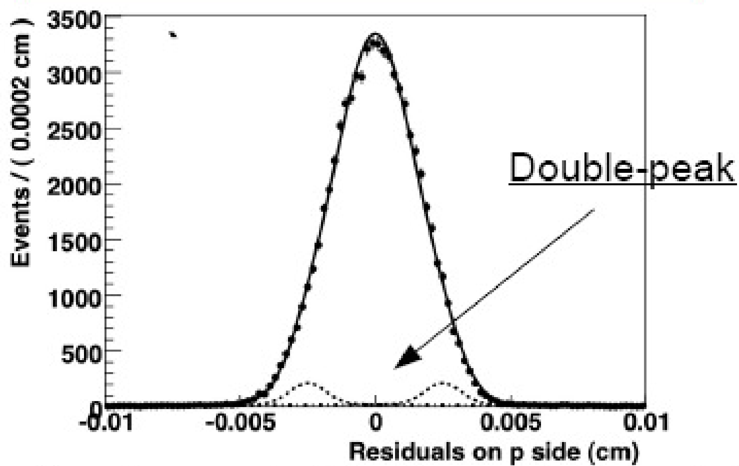



- 200 $\mu$m-thick double-sided strip detector
  - ± 45° oriented strips
- the design allows a long double-sided detector with short strips on both sides
- Active area = 27 x 12.9 mm$^2$
- 50 $\mu$m pitch on p-side
- 50 $\mu$m pitch on n-side
- Strip capacitance ~ 4 pF
- Designed & fabricated at FBK-IRST

# Striplet:
# Test-beam results



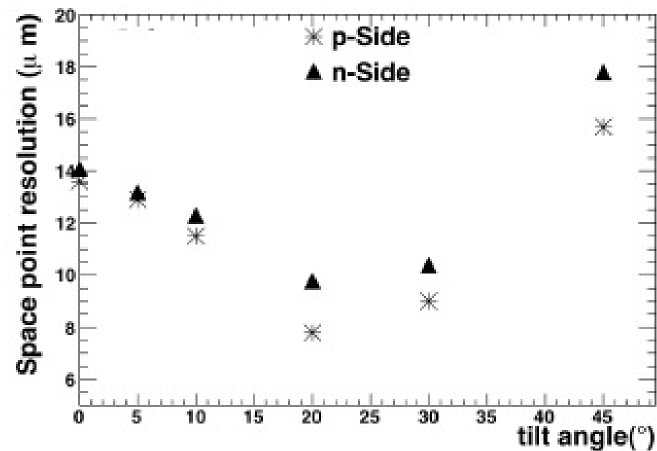

Spatial resolution



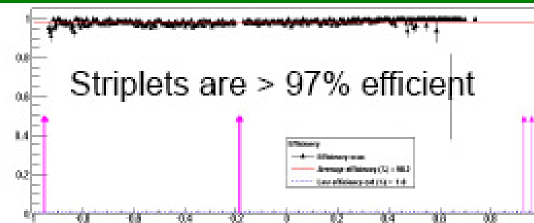

- Double-peak effect in resolution plot
- It helped in improving resolution of almost 10%

- p-Side: Space Point resolution: 13.6 $\mu m$
- n-Side: Space Point resolution: 14.1 $\mu m$
  - Pitch = 50 $\mu m$ on both sides

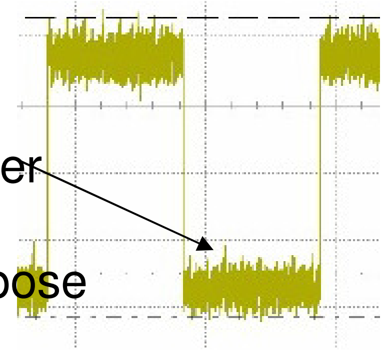
Spatial resolution Vs tilt angle




Efficiency along the detector

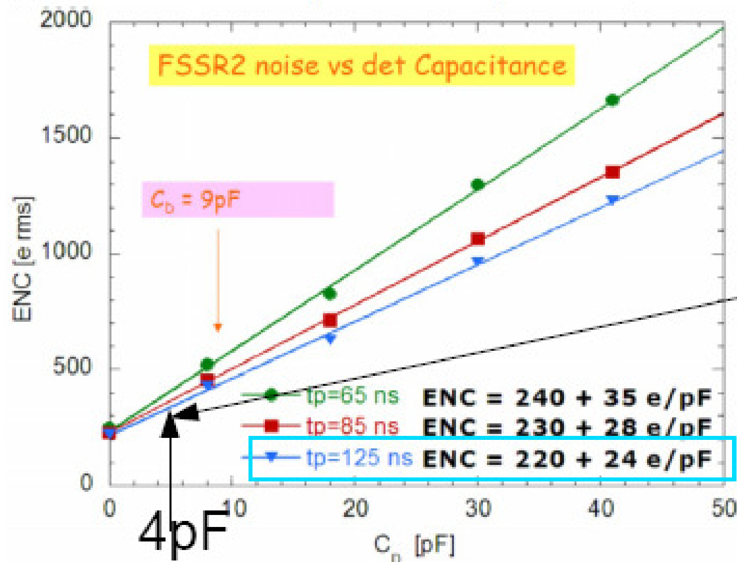


# Calibration results



- Discovered an extra source of noise(300e-) from internal (chip) pulser
- Measured noise vs. Temperature
- Under development a new DAQ test-stand, based on VME gen.purpose (i.e. FPGA based) board (V1495), with a LabVIEW based interface.

| Detector | Striplets | | Telescope | |
|---|---|---|---|---|
| Polarity | p side | n side | p side | n side |
| Noise ($e^-$ RMS) | 560 | 978 | 400 | 742 |
| S/N | 29 | 16 | 60 | 32 |
| Gain (mV/fC) | 96 | 67 | 97 | 67 |




About 316 enc*

At test-beam we were very close to benchmark for telescope detector on p-Side

*= expected for p-Side of telescope

# R&D on pixel options

G.Rizzo

Hybrid pixel:

- Prototype Front-end chip (FE32x128) for hybrid pixel produced and under test since last Friday in Pisa
  - Data push fast readout architecture
  - Target hit rate 100MHz/cm2
  - 32x128 pixels, 50x50 um pitch.

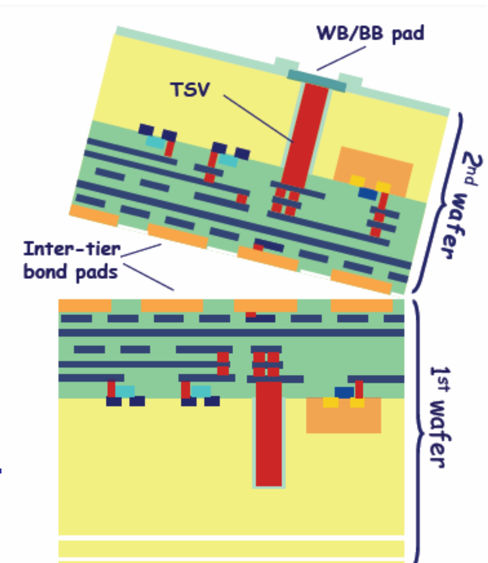
- Delay in the delivery of the pixel sensor matrix:
  - Still in production ready by mid April
  - It might be difficult to realize bump bonding with the FE chip and get ready for the test-beam foreseen in Sept. 2010.

CMOS MAPS:

- Campaign of irradiation with neutron started on APSEL test structures
- Preparing next (~October) submission of 3D MAPS (realized with 2 CMOS layers interconnected, Chartered/Tezzaron 130 nm process).
- Analog channel optimization (L.Ratti)
- New readout architecture under development with higher efficiency and better timestamp granularity (~100 ns) (F. Giorgi)
  - Still data push but could evolve easily to a triggered architecture

# Vertical Integration for the SuperB-SVT

L.Ratti



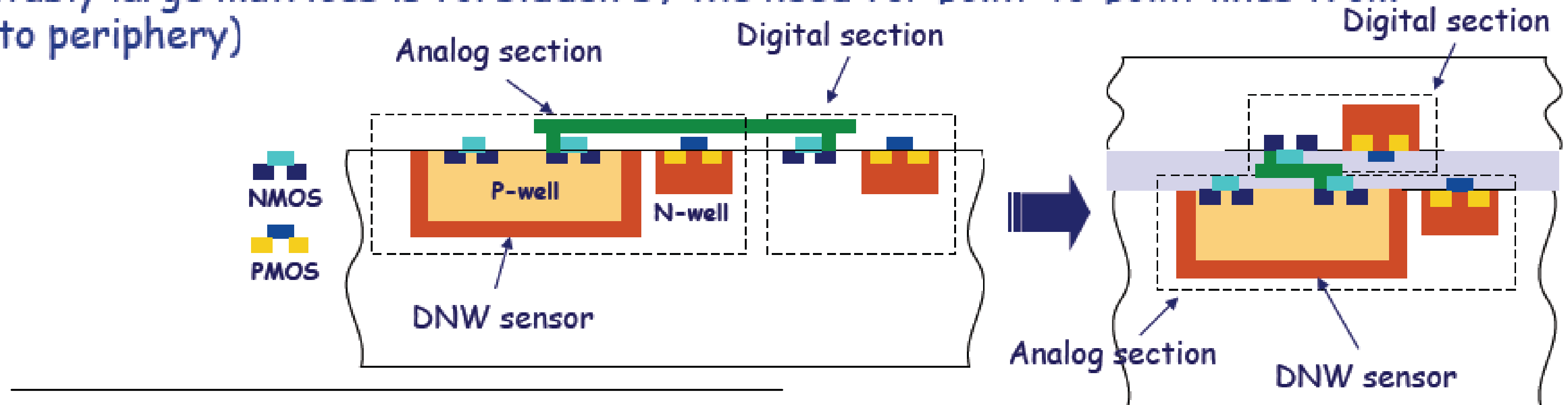

Technology leap offered by the Vertical Integration (3D)
Analog and Digital block can be integrated on separate tiers, then thinned, stacked and interconnected (through Silicon Vias).

- Two different 3D solutions are being investigated for the SVT layer0 at SuperB through extensive R&D programs, namely hybrid pixel detectors (shaperless front-end approach) and DNW MAPS (classical front-end approach), both in 130 nm *CMOS* technology
- Both MAPS and hybrid pixels can gain significant benefits from going 3D
  - increase in charge collection efficiency
  - immunity from (or reduction of) cross-talk phenomena between digital blocks and sensor/analog circuits
  - scalability to large sensor matrices

- After solving a few problems, which have been preventing the run from starting for several months, the first 3D MAPS structures (from the 2009 submission) may be available at the end of May/beginning of June

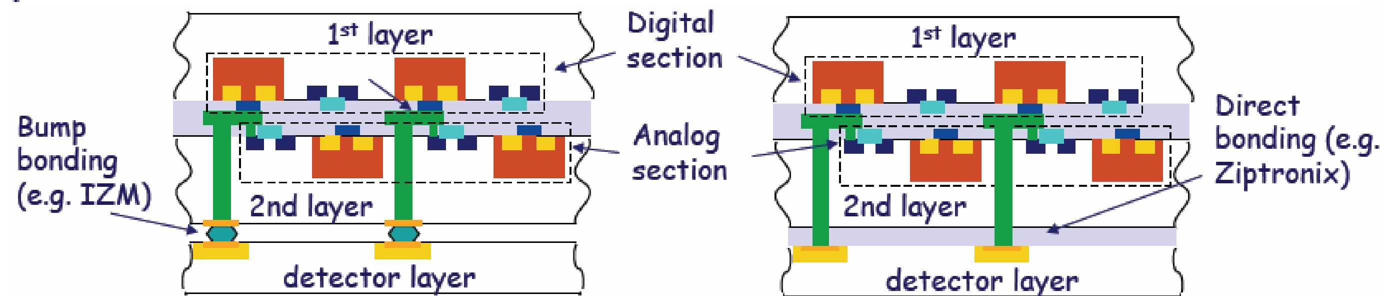
# 2D→3D MAPS

- less PMOS in the sensor layer → improved collection efficiency
- more room for both analog and digital power and signal routing (in planar CMOS MAPS scaling to suitably large matrices is forbidden by the need for point-to-point lines from macropixels to periphery)




# Hybrid Pixel

- Development of a 3D front-end chip to be vertically integrated with fully depleted detectors through some more (bump bonding) or less (direct bonding) standard technique




- Larger signal available from the detector
- More advantageous trade-off between S/N and dissipated power

# The FE design approaches

**For MAPS**

Classical front-end

(PA + shaper)

- Larger power dissipation
- Larger area (also MIM capacitors may be required)*
- Can reliably achieve large charge sensitivity**
- Noise and threshold dispersion can be optimized independently

*Might be less of a problem in 3D processes

**Large charge sensitivity= 600/800 mV/fC

**For Hybrid pixels**

Shaperless front-end

- Smaller power dissipation
- Smaller area (MIM capacitors not required)
- Not suitable for large charge sensitivity**
- Depending on the feedback network , noise optimization may affect threshold dispersion minimization

- Use of a transconductor in the feedback network can make the analog processor more robust against possible bias voltage drop in large sensor matrices and temperature changes

# Chip readout architecture for a pixel layer0

F.M.Giorgi

**TARGET**

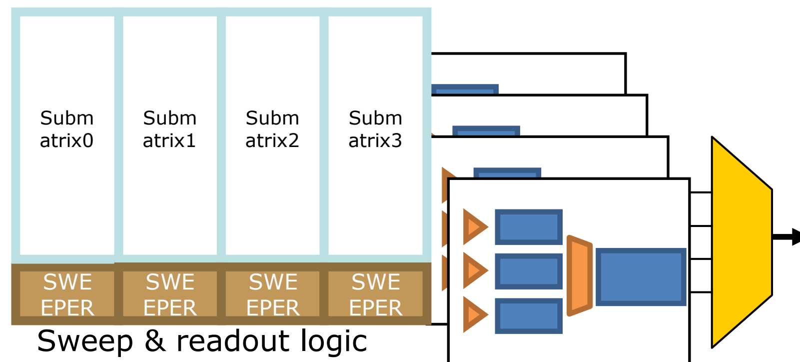
- Rate: **100** MHz/cm²
- Matrix area ~ **1.2-1.3** cm² –- **256x192** pixels - **50** µm pitch
- R.O. Architecture for **hybrid /3DMAPS** sensor
- Output bus bandwidth ~ **20**bit@**200**MHz (**4**Gbps)

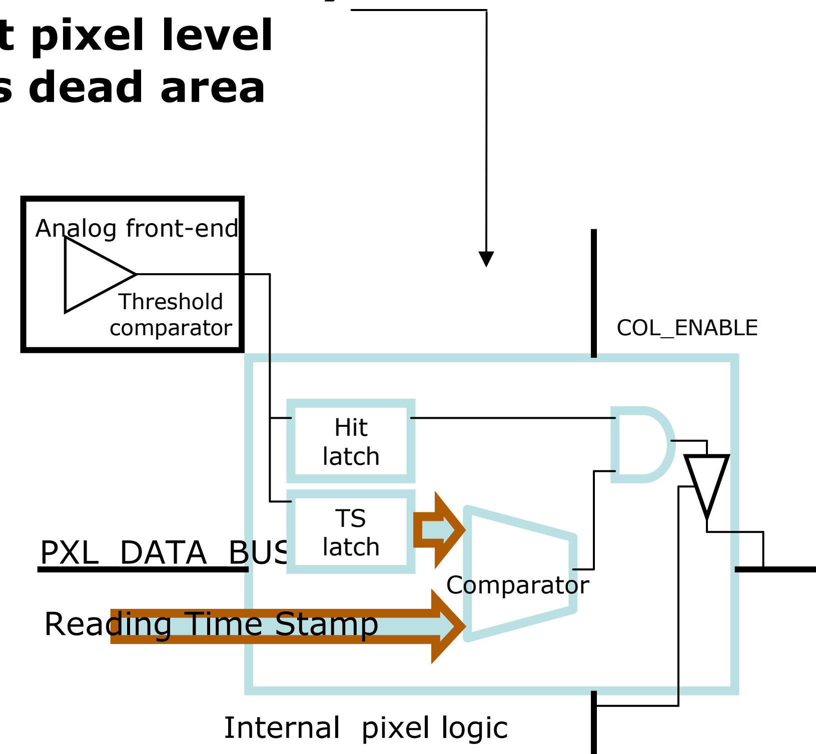
***Previous matrix architectures (2D MAPS)***:

-**Simple** in pixel digital logic (competitive N-Well) →
-control of portions of matrix area (16pxl=MP)→ freezing of empty pixels
-→ x**16** dead area → **trade off** **scalability vs efficiency**

***New matrix architecture (Hybrid or 3D MAPS)***:

- **Dense** in pixel digital logic - **now TS at pixel level**
→**NO FREEZING required** → **much less dead area**
→**Less readout memory required**
→**Smaller BC periods allowed**




- **New sweeping logic realized**
- **SPX0 readout re-integrated**

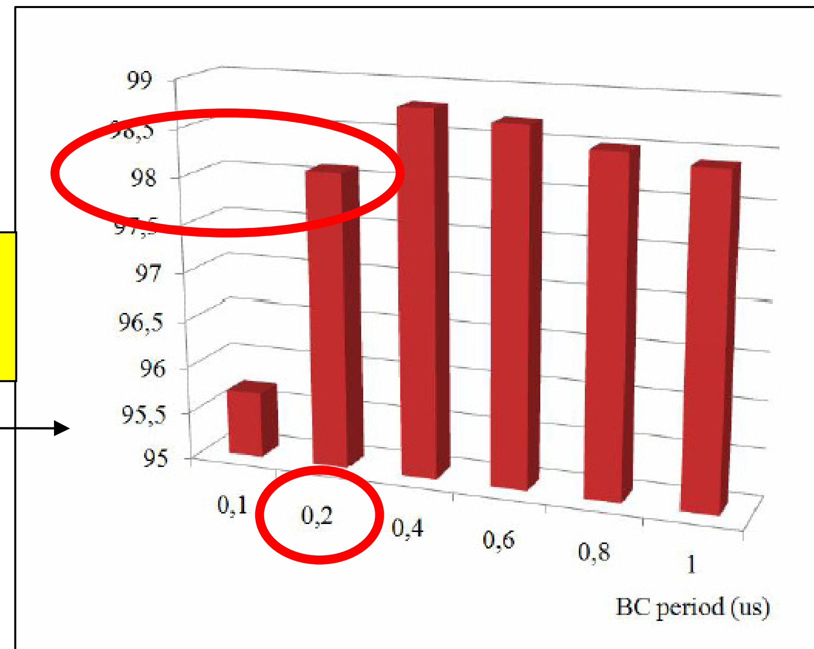
# Simulations achievements with the new architecture

(exploiting hybrid or 3D MAPS technologies)

- Reduced dead time (no x16 factor due to MP freezed area)
- Faster & easier timewise matrix scans.

**Fully integrated NEW architecture** *simulation*:
RDclk **50 MHz** - BC **200 ns** – Fast_clk **200 MHz**
**Sweep Efficiency : 99.92%**

**Compare previous 2DMAPS** *arch. simulation*:
RDclk **66.67 MHz** - BC **200 ns** – Fast_clk **200 MHz**
**Sweep Efficiency : ~ 98 %**




**BC 200 ns**: lower limit due to the recycle of old readout **taken AS IT WAS.** (designed for BC>1us)
It is **NOT** a **sweeper limit**

Several steps already taken to reach the BC=100 ns working point.
**Work in progress.**

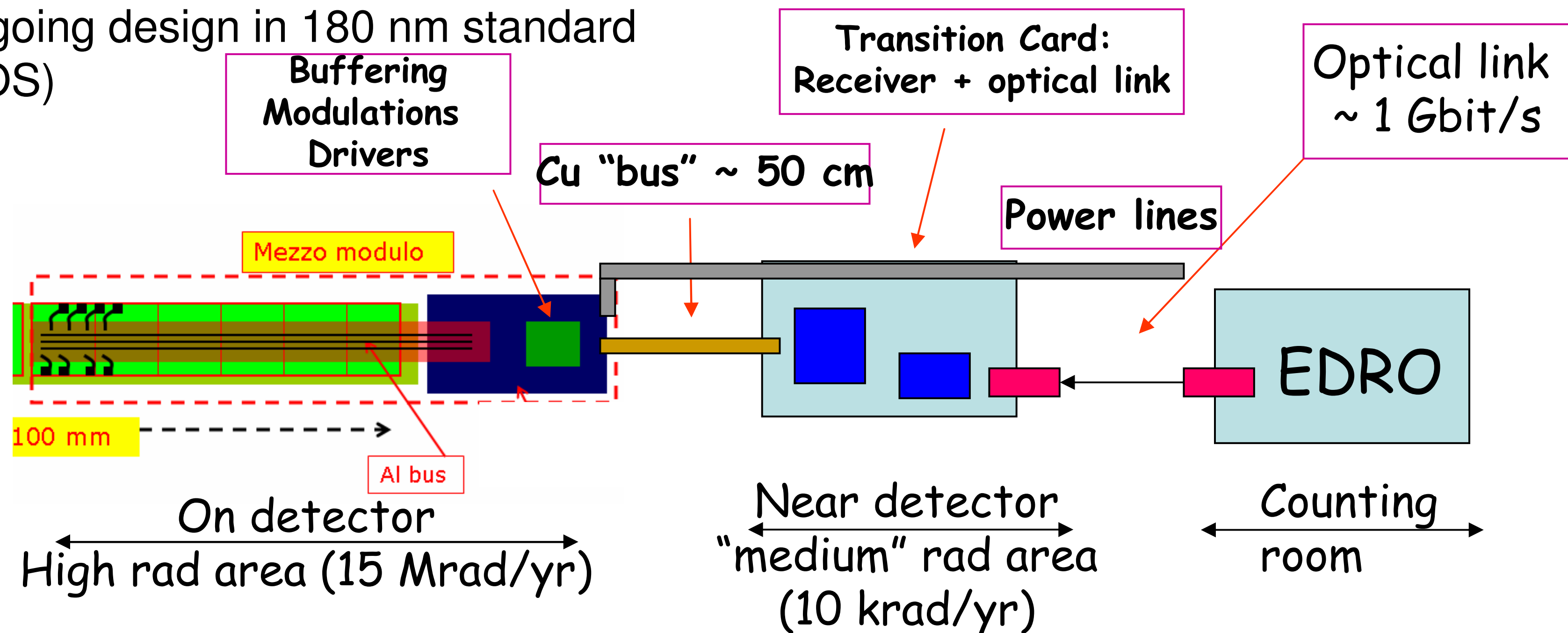
# Revision of the HDI

M.Citterio

**New Baseline will not necessarily require that all data will be transferred to the transition card**

- **the HDI could/should act as a data buffer awaiting for trigger, if necessary**
  - The SRAM project will provide guidelines
- **The HDI will drive a short copper link (up to 50 cm)**
  - How many copper lines are needed is under study
  - The line drivers will be preceded by a "formatting logic"
- **The "transition card" will do the transition between copper and fiber using the optical link**

Rad-Hard SRAM
(on-going design in 180 nm standard CMOS)



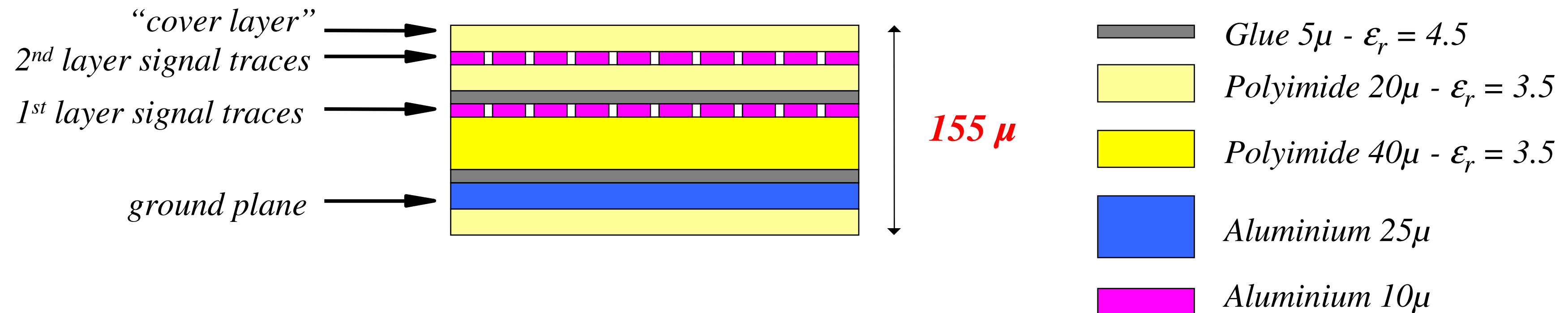
# Aluminum Bus Evaluation

**Measurements on the 1st BUS prototype are on-going**

**→ confirmed a typical impedance of ~ 60 Ohm**

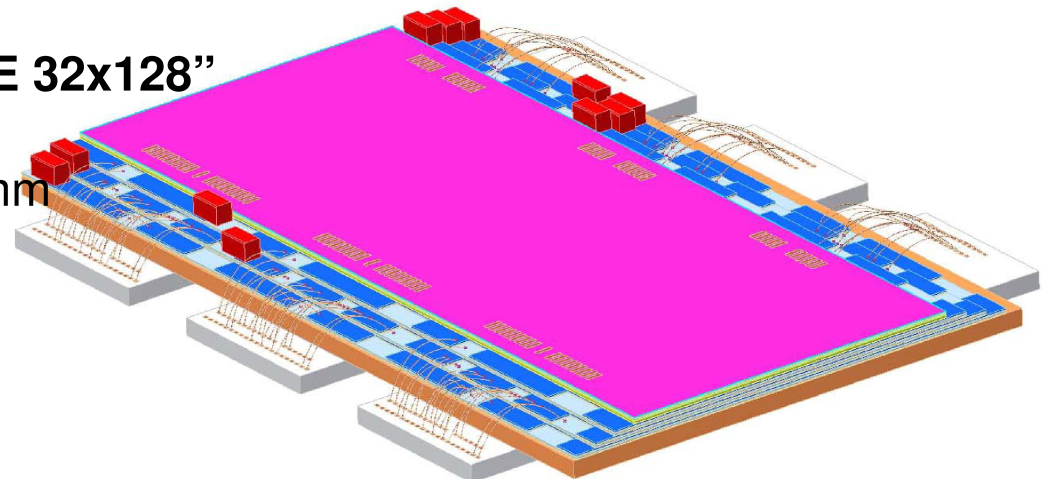
**→ crosstalk is higher than estimated ( ~10 %)**

- Discussion on the stackup is still on going with CERN
  - simulation and actual BUS properties still do not agree (cut the BUS to verify layer thickness)
  - frequency response (signal up to 200 MHz, on individual lines) are promising at BUS lenght ~ 10 cm




**Layout of a BUS for 3 front-end IC "FE 32x128"**

- Bus widht: 8.7 mm
- Signal trace layer widht: 7.5 mm
- Bus length ~ 6.5 cm



# L0 support & cooling

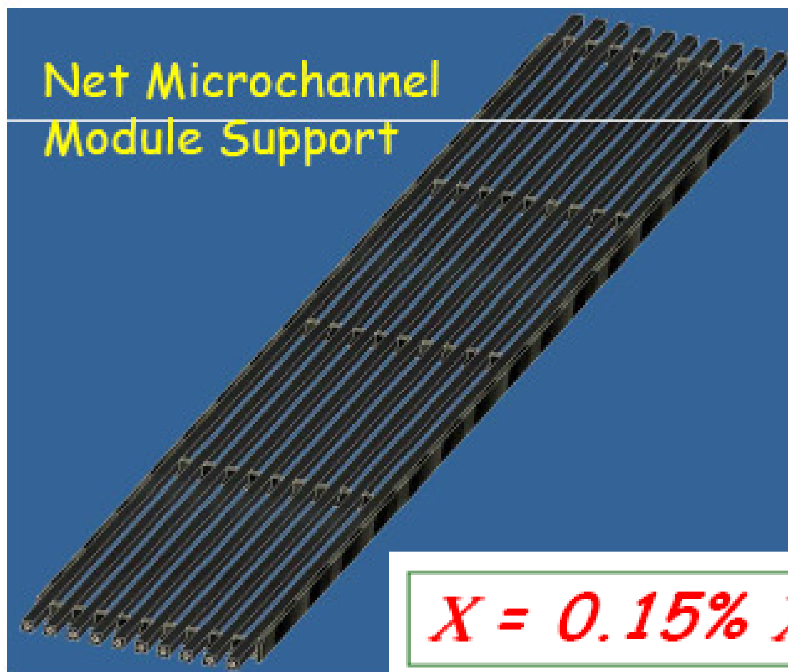
F.Bosi

Assuming further progress in MAPS sensor design, and looking to actual hybrid pixel, the required Power (analog + digit ), could step down to 1.5-1.0 W/cm$^2$.

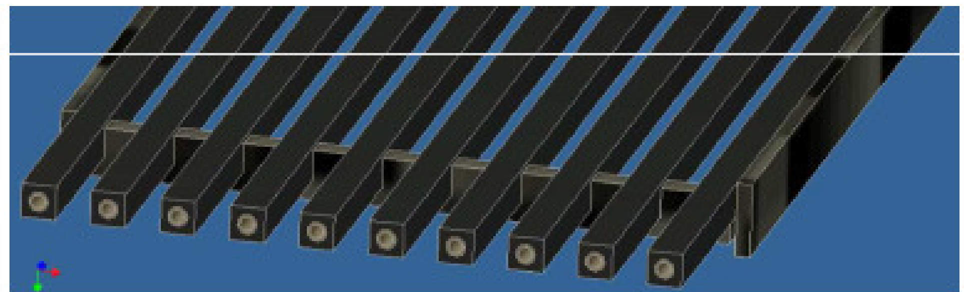
We choose to design a lighter solution for the support structure .

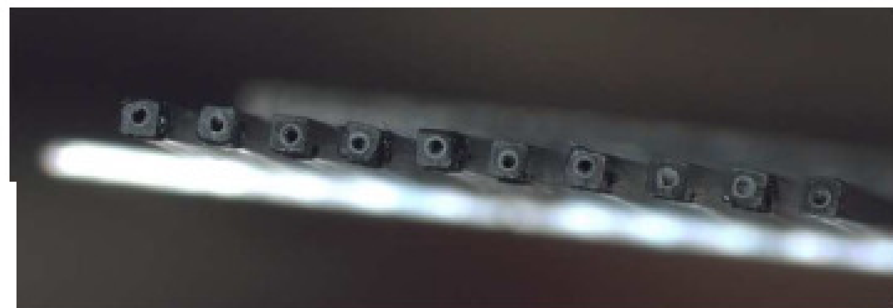
The Net Module is a micro-channel support with vacancies of tubes in the structure .

We admitted worse cooling performance for strongly gaining in $X_0$.




$X = 0.15\% \ X_0$



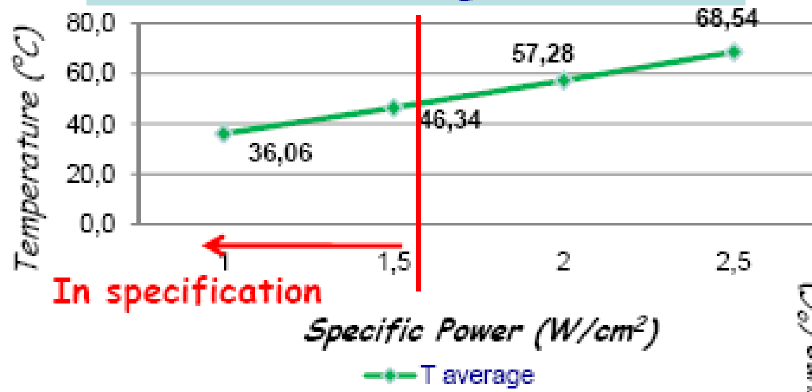


Material of the support structure: ( CFRP + peek tube + Water + CFRP Stiffeners)

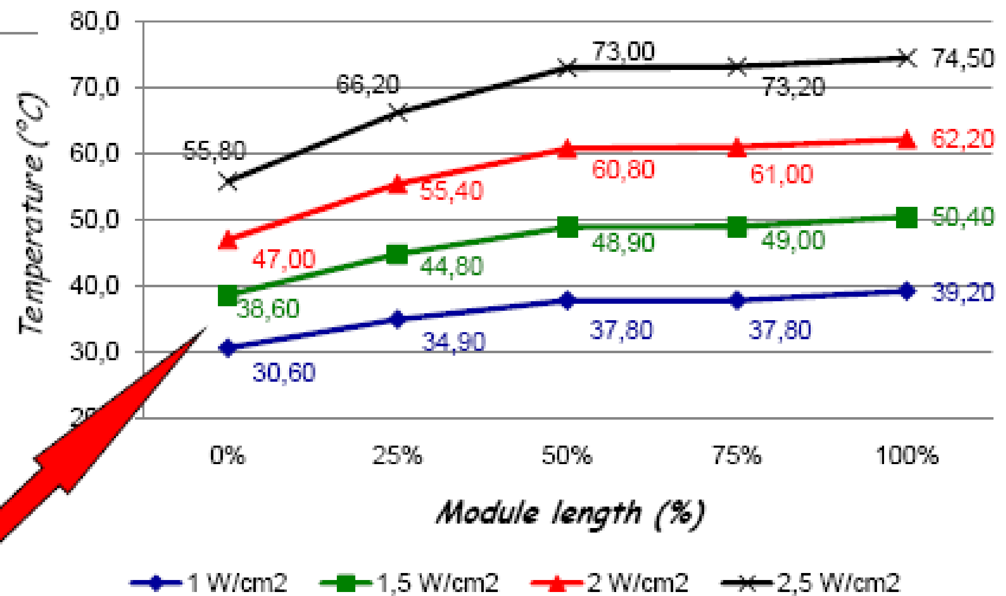
# Experimental results

*Net module average Temperature*
*Vs. Specific power density*
*Power on Single Side*

Tests performed with water-glycol @ 10 °C as coolant.

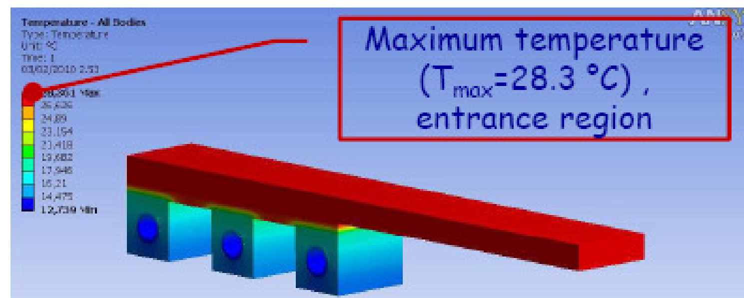



*Net module, Sensor Temperature*
*Power on Single Side*




**From this experimental data, the Net Module is able to cool power up to about 1.5 W/cm² at the max required Temperature (50 °C). This goal can also be achieved with a greater safety factor by reducing the inlet coolant temperature.**

FEA Simulations:

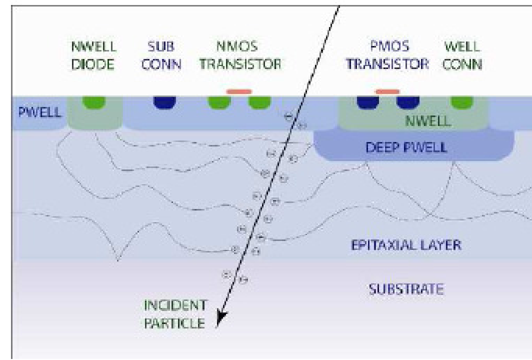



**The ~ 2 °C difference between FEA results and experimental data can be ascribed to the uncertainty of the thermal interfaces.**

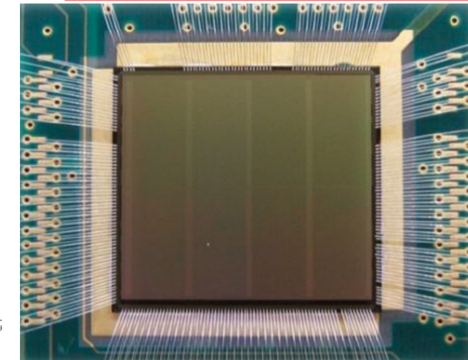
# UK Proposal for MAPS-based SVT

**Queen Mary, RAL**

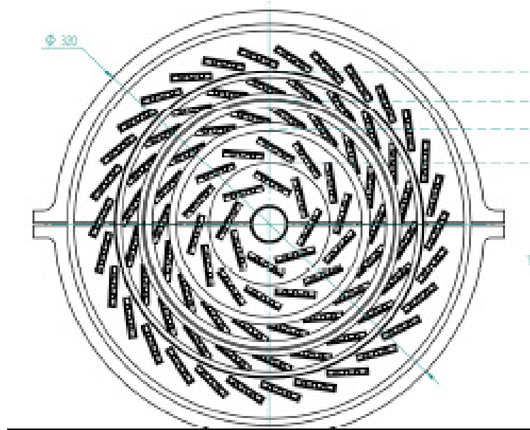
- Very interesting **MAPS technology** from UK
  - **INMAPS (180 nm)** with deep p-well to improve CMOS sensor efficiency



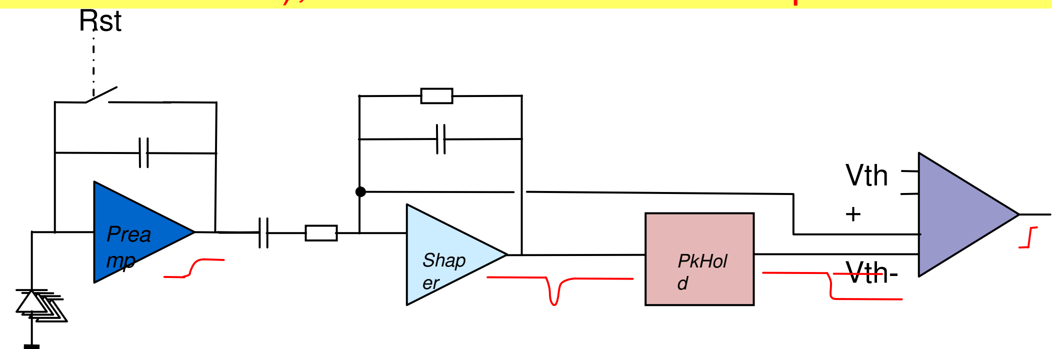
(b) CMOS MAPS with a deep P-well implant



- Mechanical Design:



Evolution of TPAC MAPS chip (50 μm pitch, realized for CALICE-ILC),candidate for a MAPS all-pixel SVT



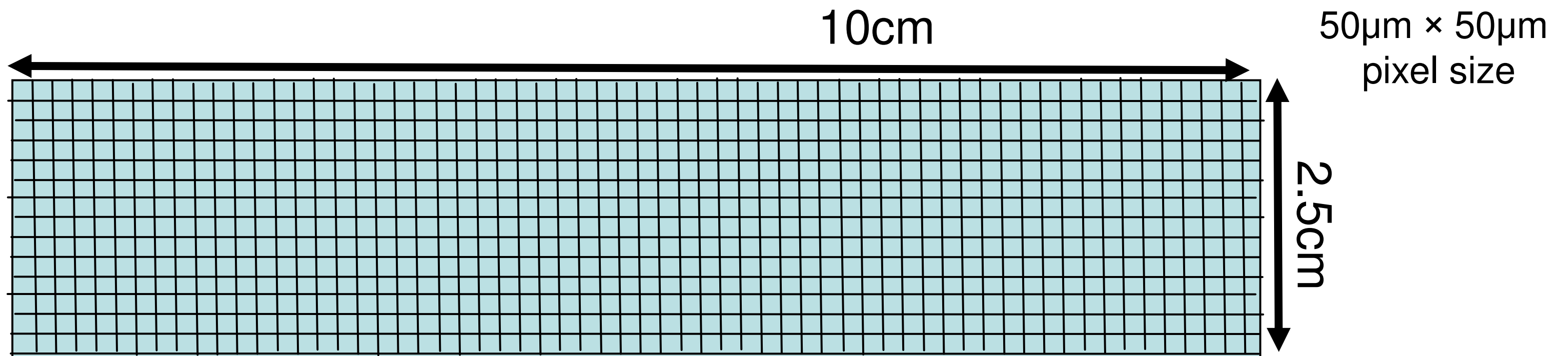

**PROS**
- Solution very robust against background
- Significantly cheaper (standard CMOS process sensors: 330K€) than strip detector.
- 5bit Ramp ADC:dE/dx information(to evaluate).
- Simpler module assembly

**CONS**
- Material of current proposal too large (1.14% $X_0$ per layer instead of 0.5% $X_0$)
- New technology
- Radiation hardness to be proven

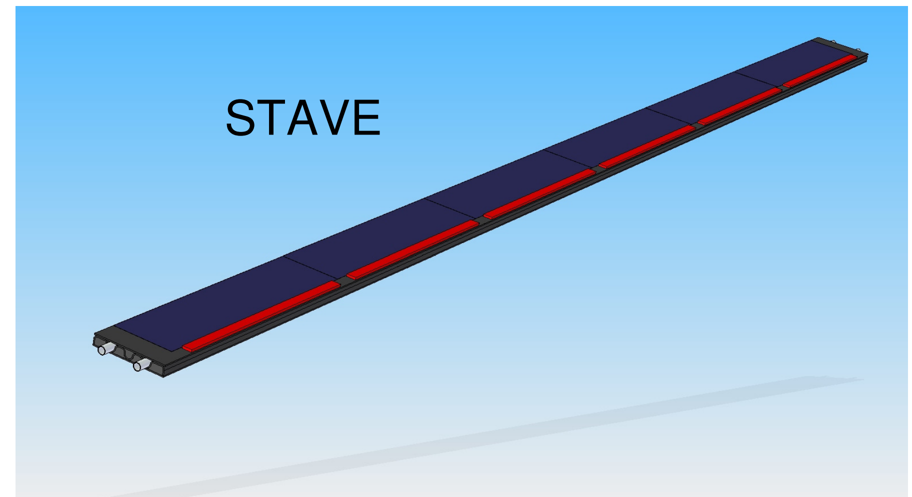
# Sensor module for SuperB

A.Bevan

- Alter layout of the chip: ($4\times2.5cm^2$ chip stitched together)
  - 1 module = a 10cm × 2.5 cm × 50μm sensor.



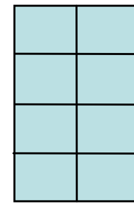

- Radiation hardness should be acceptible~$10^{13}$ n/cm$^2$.
- 10 W power per module: < 5KW per 6 layer SVT.
  - Requires active cooling.
  - Ramifications for:
    - Material Budget.
    - Utility hook-up (cooling/power/readout).

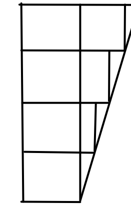
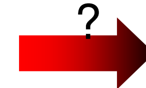


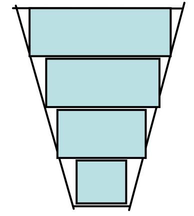
# Pick of some Items on the “to do list(s)”

A recent visit @ Pisa useful to exchange ideas to better match the SuperB SVT spec’s:

- ArchModules
  (need trapezoidal det’s):

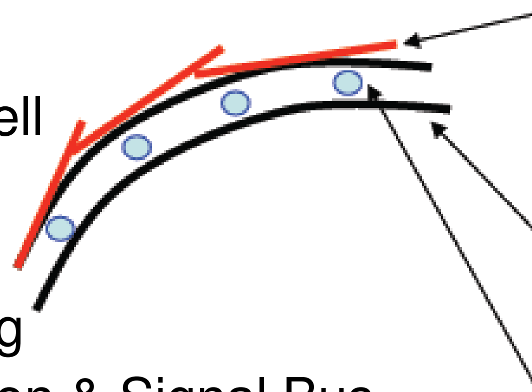




- Reduce material

Investigate the concept of half-shell space frame



Retain pinwheel for the silicon sensors (50um thick).

Superstructure would support sensors at ends (struts in the middle as/if needed).

Cooling infrastructure would support the sensor along z (into page).

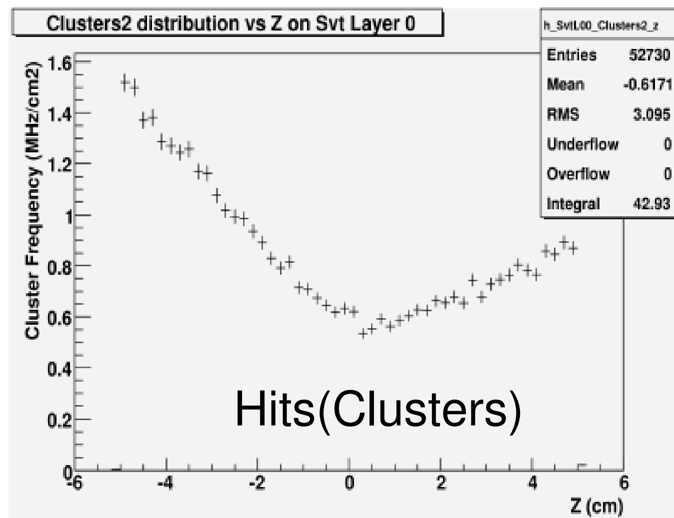
- Optimize cooling
- Power distribution & Signal Bus
- Perform RAD.Test
- Physics studies: low Pt tracking performance (implementing a model of the detector in FastSim)

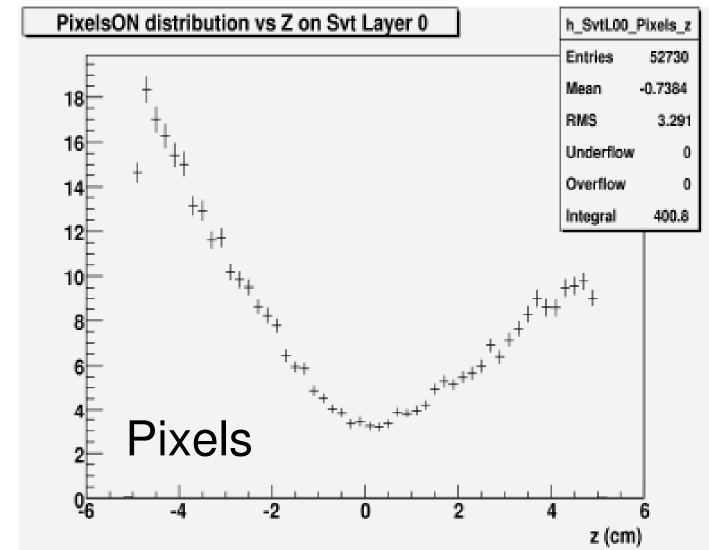
We are looking forward to the evolution of the UK proposal in the next months in order to include the MAPS all-pixel SVT in the TDR.

# Update on the Rad-Bhabha bkg in SVT

R.Cenci

- The main source of bkg for SVT comes from pair-production.
- It's worth evaluating the Rad-Bhabha source:




- No significant change in rates, but magnetic field configuration needed for RadBhabha generates wrong results for L0. Need a common configuration asap (work in progress)

- Most part of the bkg on L0 are particles coming directly from IP

| SVT Layer | Cluster rate ($kHz/cm^2$) | Pixel rate ($kHz/cm^2$) |
|---|---|---|
| Layer 0 | 858 | 8016 |
| Layer 1 | 62 | 116 |
| Layer 2 | 38 | 71 |
| Layer 3 | 15 | 28 |
| Layer 4 | 3.4 | 5.4 |
| Layer 5 | 2.1 | 3.4 |

# Conclusions

- The technologically mature SVT design as baseline for the TDR: L0 striplet + L1→5 Strip module
- A lot of activity is ongoing on the pixel solutions (hybrid & MAPS), more robust against background and useful in a Layer0 of 2$^{nd}$ generation.
- The boost in the performance offered by the Vertical Integration technologies has been exploited: results in few months.
- UK proposal: after a very fruitful (for all of us!) meeting in Pisa with UK group, their proposal is evolving in order to reduce the material budget for support/cooling in layers 1-5.
- The physics potential of MAPS all-pixel SVT needs to be evaluated with FastSim studies.