PID meeting

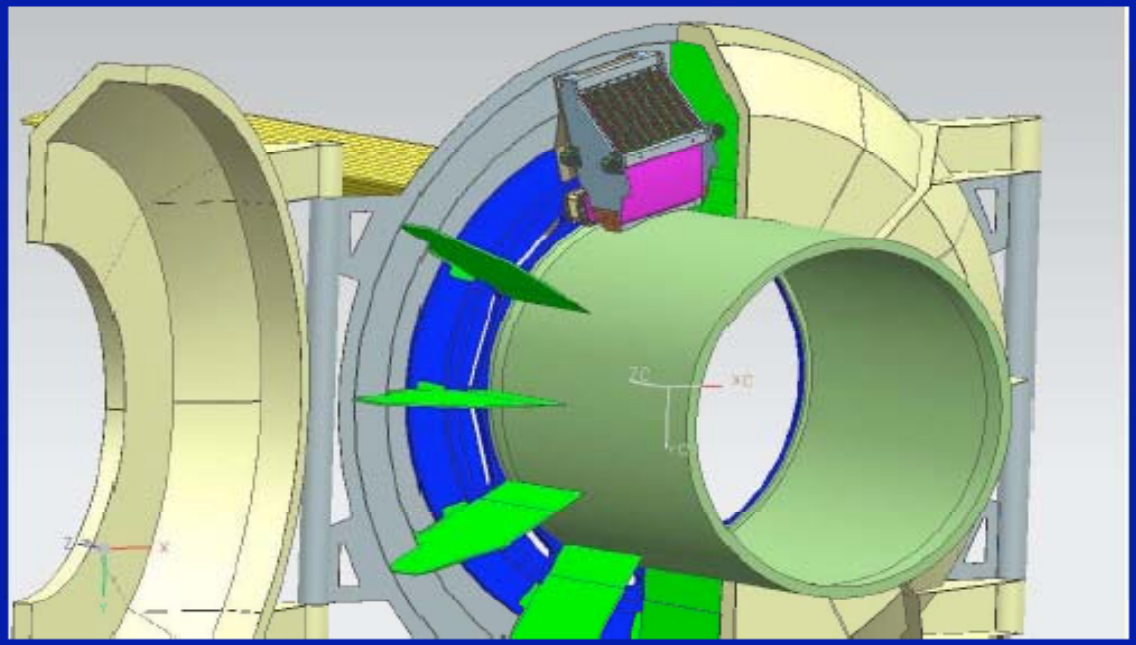
Mechanical implementation

Electronics architecture

SNATS upgrade proposal

How could FDIRC look like ?

Massimo Bennetoni, Padova



- This drawing just shows a direction we are heading.

7/28/2009 J. Va'vra, FDIRC design update 7

Electronics is split in two parts :
- one directly mounted on the PM base receiving the PM signal and processing it with TDC/ADC
- the other one concentrates and pack all the channels to send data to the DAQ

Electronics on the detector

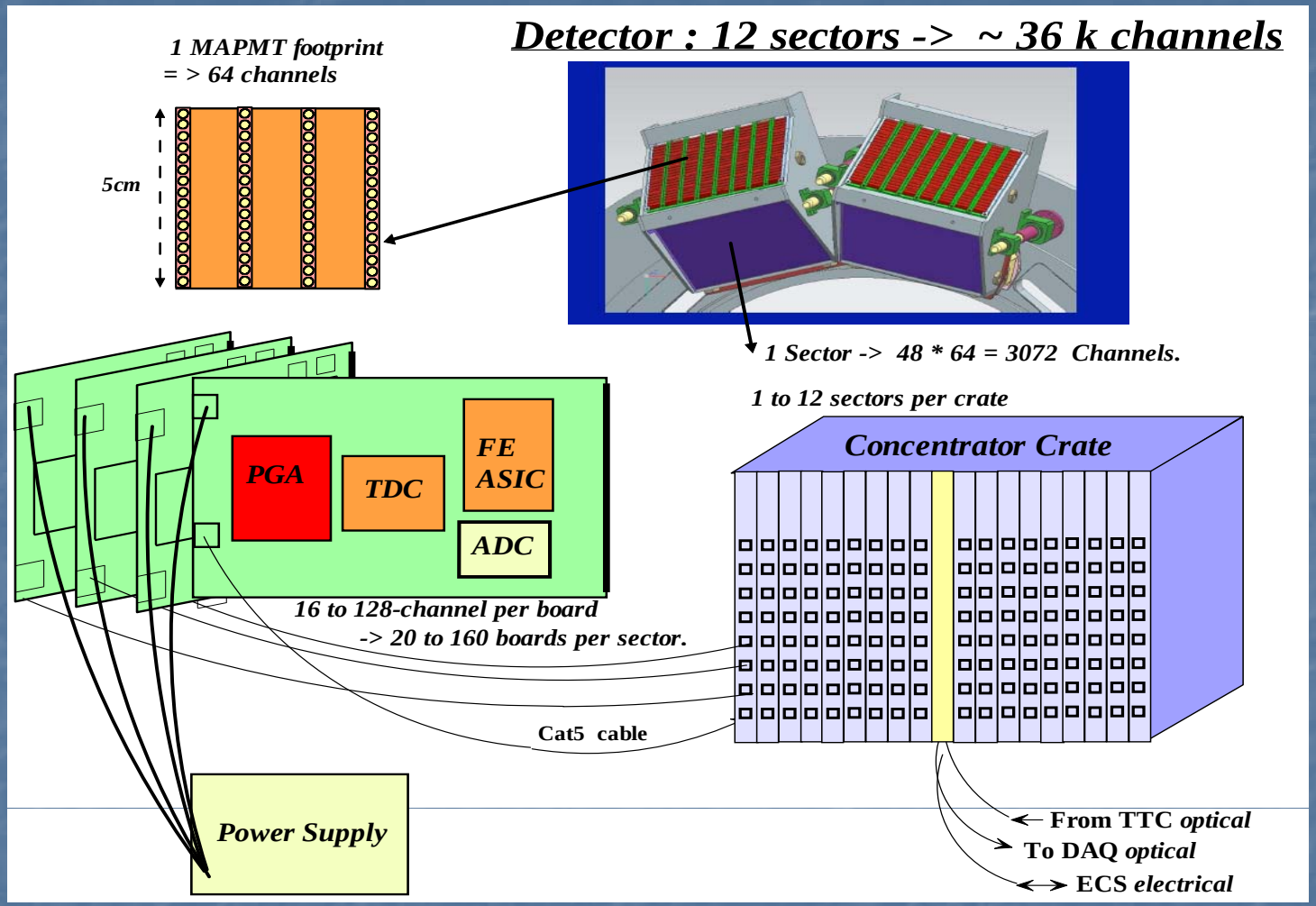
↳ Mechanical constraints: Fixing the module on the PM base.

Dismounting issues.

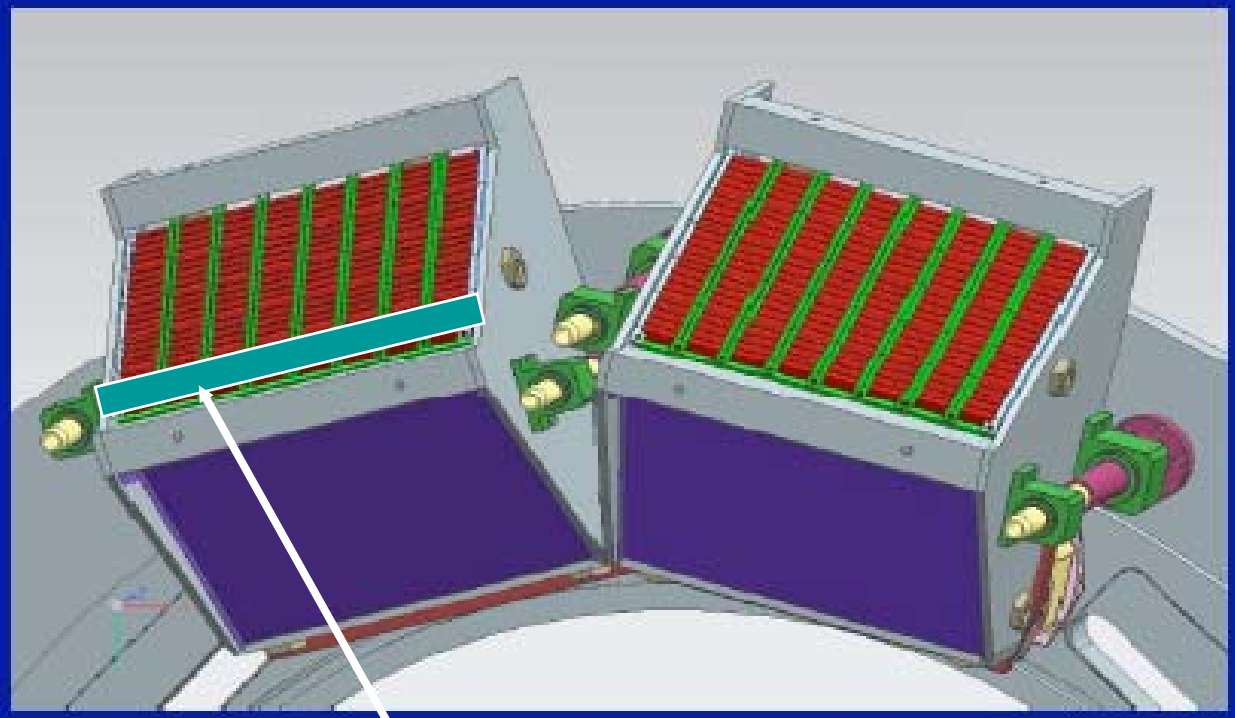
↳ Thermal constraints : Door closed gives problems of cooling.

↳ Fans on the module as G Varner's ?

↳ Global heat extraction....

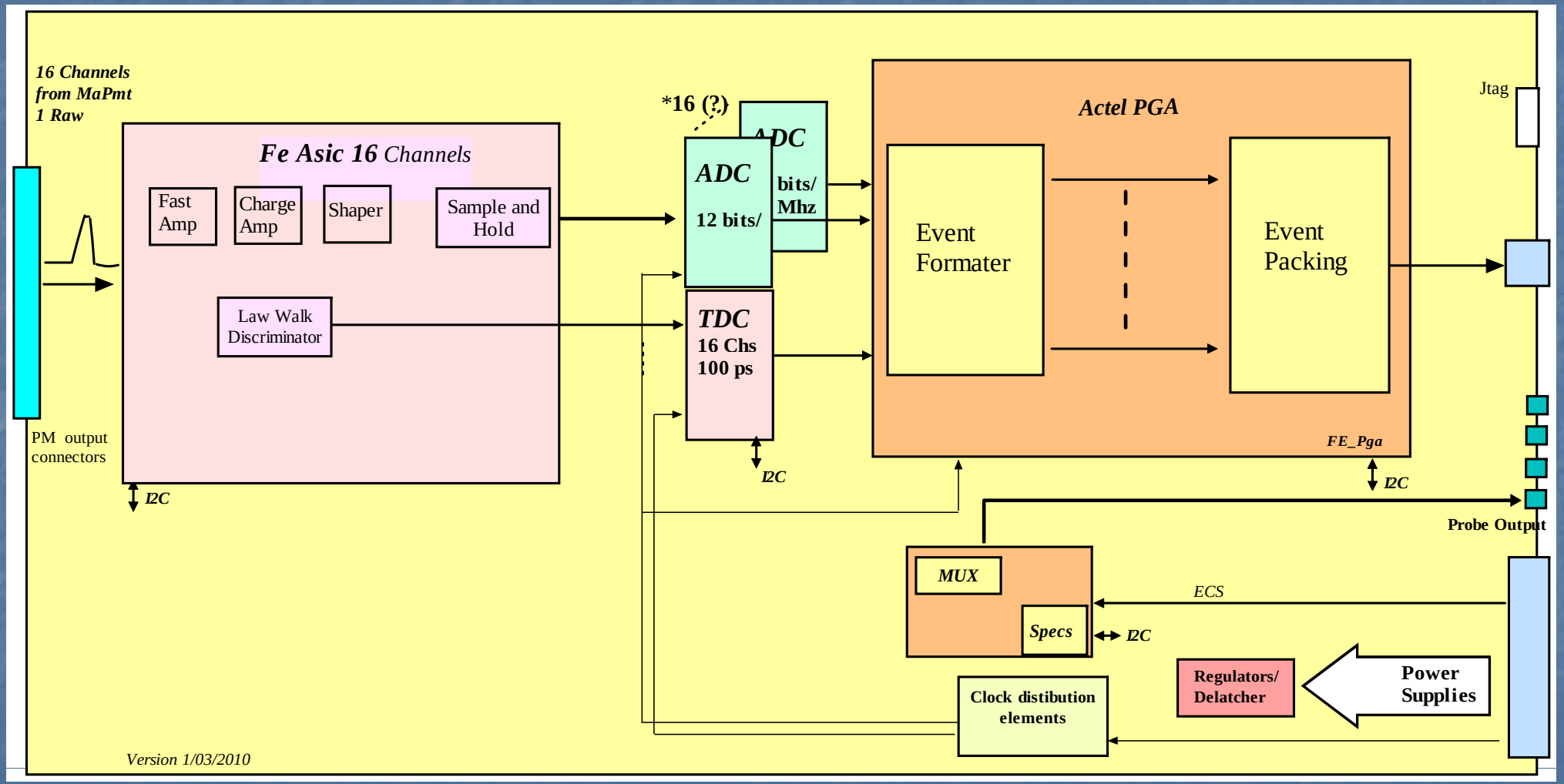

Detector : 12 sectors -> ~ 36 k channels
1 MAPMT footprint
= > 64 channels
5cm
1 Sector -> 48 * 64 = 3072 Channels.
1 to 12 sectors per crate
Concentrator Crate
PGA
TDC
FE ASIC
ADC
16 to 128-channel per board
-> 20 to 160 boards per sector.
Cat5 cable
Power Supply
From TTC optical
To DAQ optical
ECS electrical

Other possible solutions ...



Long boards : 128 channels . Mechanical issues for a precise adjustment base to base. This high granularity has a impact in case of failure. (calculation ?)

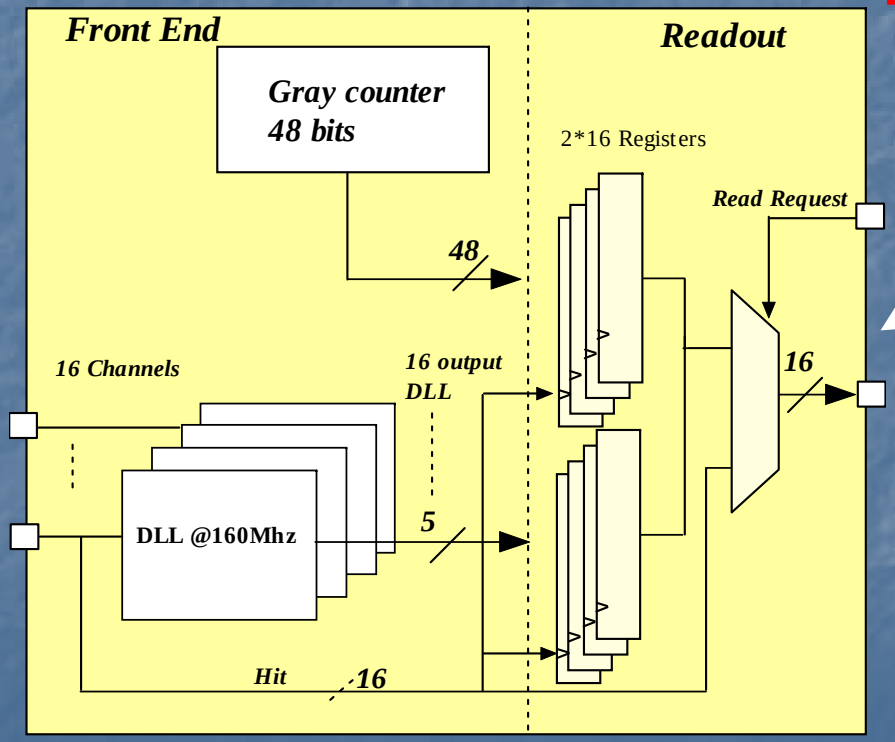
FE board synopsis



Stake: high count rate detectors

- INL, DNL, resolution … : same requirements.
- Increase the input data rate up to the Mhz level per chip.
  - SNATS: 2.5MHz per channel but ~150 kHz per chip

Need to reduce dead time due to readout protocol between ASIC and PGA = 50 ns per 16 bit word

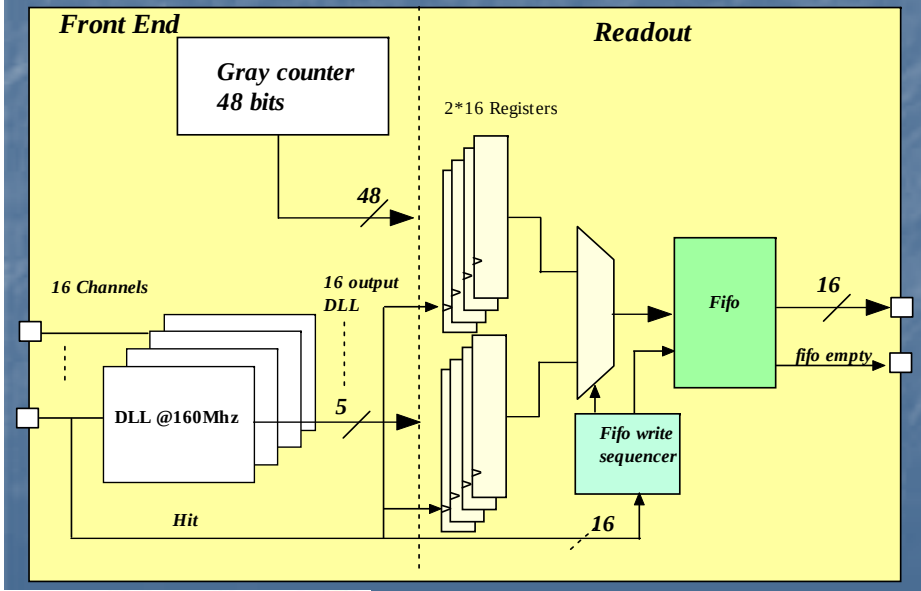


SNATS: Evolution & Perspectives

2 options (among many others …)

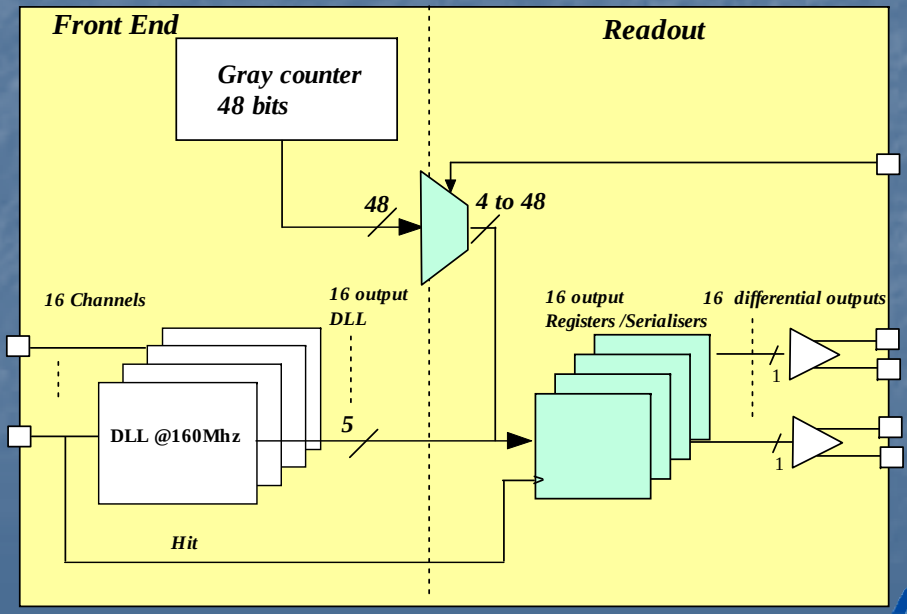
- Keeping almost the same design and just adding a FIFO at the output.
  - ➪ it increases the input channel rate in burst mode but keeps the average readout rate like the previous version.
  - ➪ The FIFO size is costly.

- Max performance :
  - ➢ Mhz/channel in burst mode but limited by the size of the FIFO.

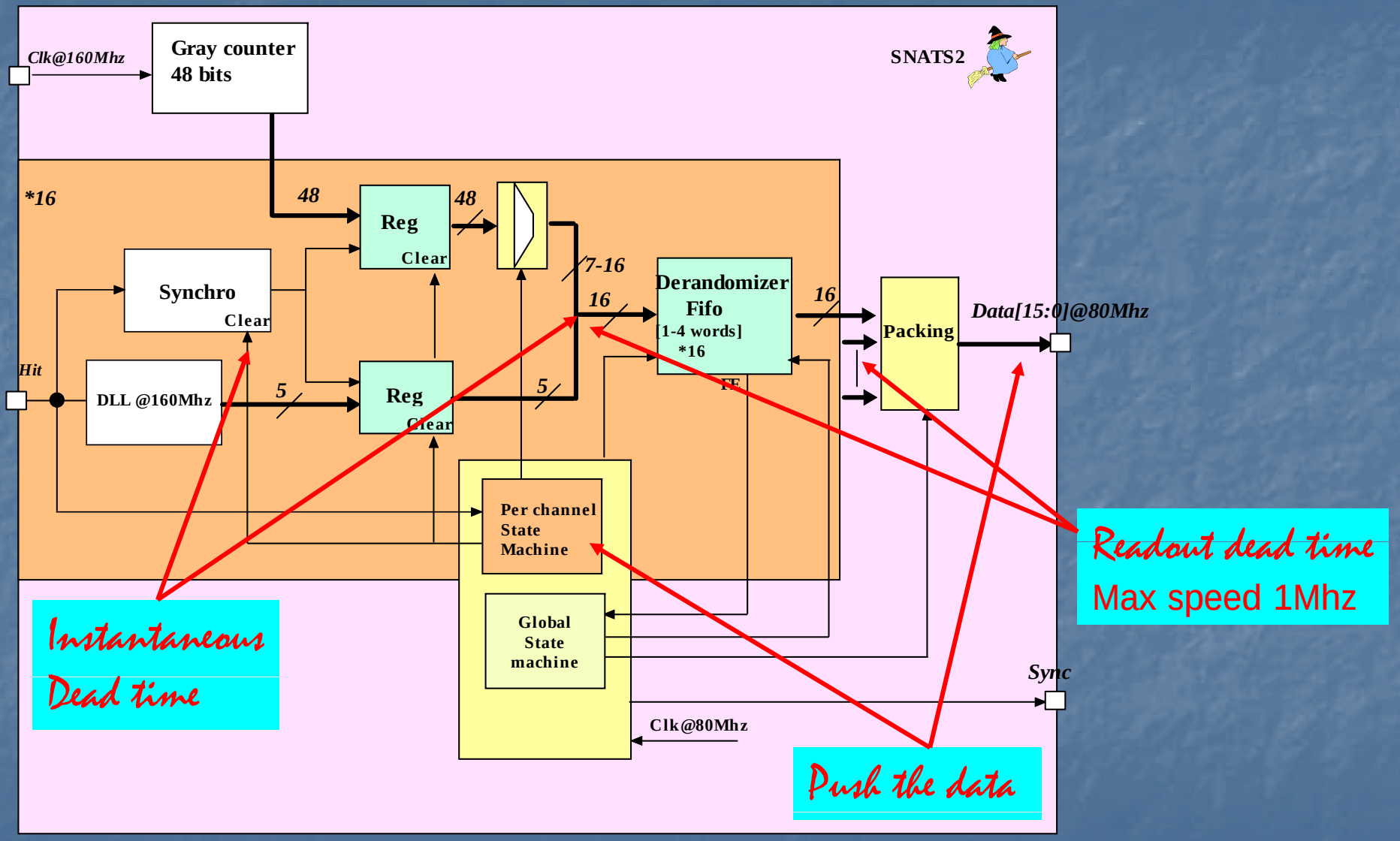


- Keeping the Gray counter inside the ASIC with an output bus width set by user in order to reduce the amount of data to be transferred. The Gray counter is duplicated inside the associated PGA.
  - ➪ The serial output is synchronous to the clock to ensure the matching between the 2 counters.
  - ➪ 16 differential output channels @ 80 Mhz (160MHz?).

- Max performance
  - ➢ 5 DLL bits + 4 Gray bits + start bit = 10b @ 80 Mhz = 8Mhz input rate !
  - ➢ Linked to performance of the readout acquisition



SNATS : new design



Summary of the SNATS evolution :

- Redesign of the readout and a few improvements on the Front end part
  - Programmable number of bits for the time counter.
  - New derandomizing FIFOs : depth of 16/32 events (each of 4 * 16-bit data word)
  - Data push at the output

Run end 2010 . AMS .35 um technology. Chip delivered first quarter of 2011

We have to think of the way to run the chip together with the FE ASIC and to match the analog pulse converted by the ADC with the hit time -> Design and simulation in the FPGA
Also have to interface the FPGA with the ***Proposal for the Electronics Trigger and DAQ architecture*** to get inside the front end buffer.

The data are output with a latency depending on the rate per channel and the occupancy of the chip.

2 Clk cycles to output the data (Derandomizer FIFO to PGA @ 84 MHz (56*1.5)) followed by 2 Clk cycles for each other fired Channel.

Latency from 2 Clk cycles to 32 Clk cycles (2.5 MHz per channel)

Costing

PID BARREL	510
Front-end electronics	**275**
FE-IC-1 prototypes + prod (qty 10 + 100 + 4000)	100
FE-IC-2 prototypes + prod (qty 10 + 100 + 4000)	100
FE boards (including FPGA) (qty 5 + 20 + 500)	125
Cables between FE and concentrator (qty 500)	25
Concentrator electronics	**55**
Concentrator boards (qty 50)	15
Concentrator control boards (qty 6)	6
Concentrator crates (qty 6)	18
Concentrator backplanes (qty 6)	6
Concentrator prototyping	10
LV supplies	44
LV Power Supplies	36
LV cables	8
HV supplies	**48**
HV Power Supplies	36
HV cables	12
Final installation	3
Electronics test Bench	10