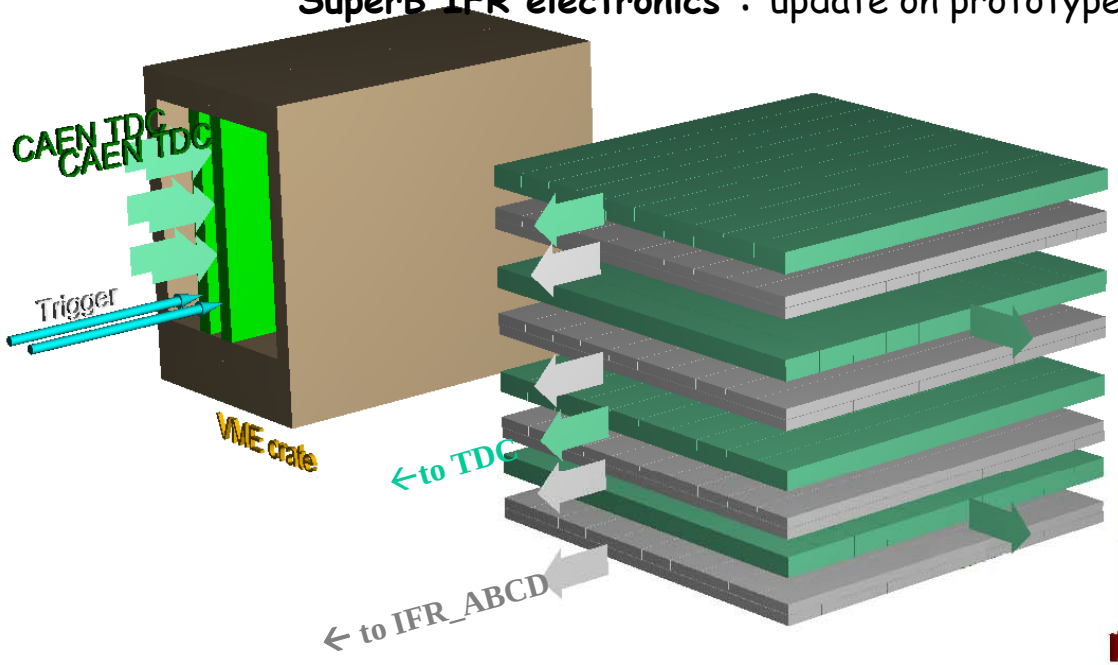
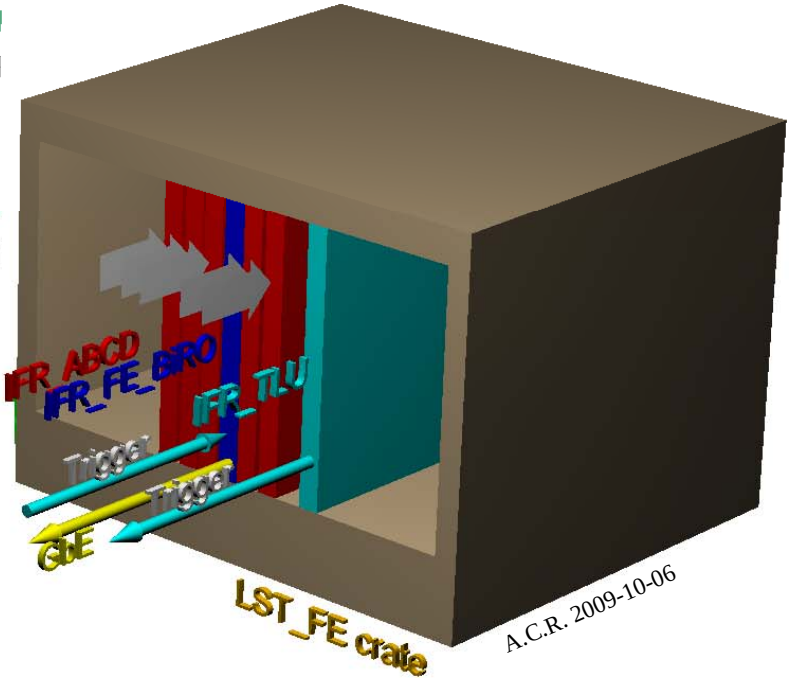
SuperB IFR electronics: update on prototype electronics and DAQ

Summary

(a) prototype detector and electronics for a proof of principle: outline
(b) description and status of the components of the IFR prototype electronics
(c) outline of the run control / daq system for the IFR prototype
(d) conclusions

SuperB IFR electronics : update on prototype electronics and DAQ – (a)



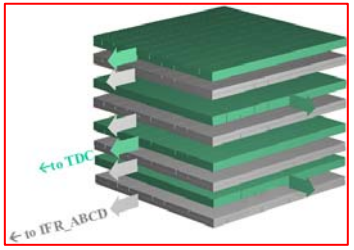


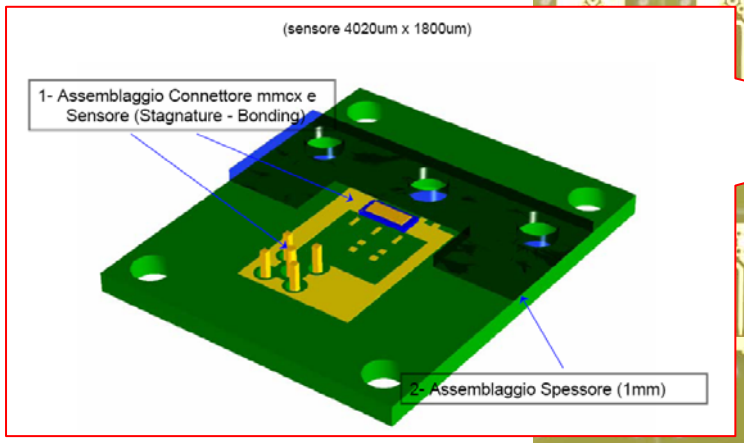
SuperB IFR prototype:
- 4 layers of x-y scintillators, 1 cm thick, read in binary mode
- 4 layers of scintillators 2 cm thick, read in timing mode

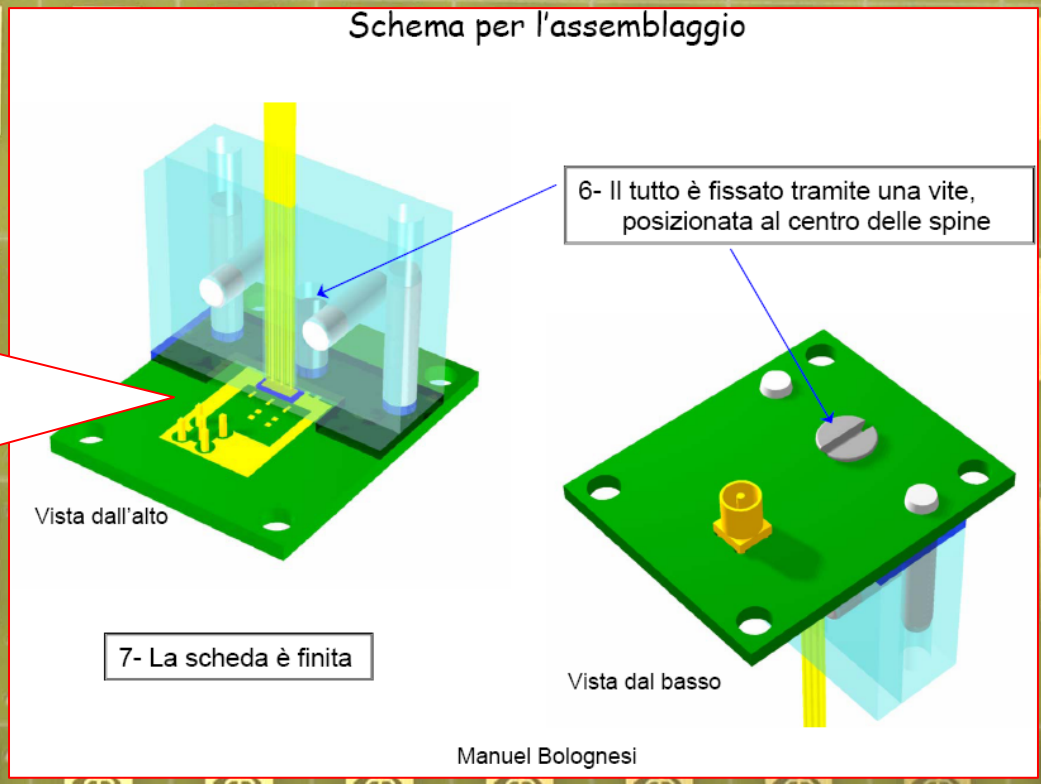
SuperB-IFR prototype readout electronics (baseline):
- "IFR_ABCD": sensor Amplification, Bias-conditioning, Comparators, (new!) Data processing: it samples the level of the comparators outputs @ >= 80MHz and stores it, pending the trigger request
- "IFR_FE_BiRO": collects data from IFR_ABCD cards upon trigger request and sends it to DAQ PC (via GbE)
- "CAEN_TDC": a multi-hit TDC design based on CERN HP-TDC; hosted in a VME crate and read out via a VME CPU or via a VME-PCI bridge to the DAQ PC
- "IFR_TLU": a module (Trigger Logic Unit) to generate a fixed latency trigger based on primitives from the IFR prototype itself or from external sources

SuperB IFR electronics : update on prototype electronics and DAQ – (b)

SiPM carrier PCB





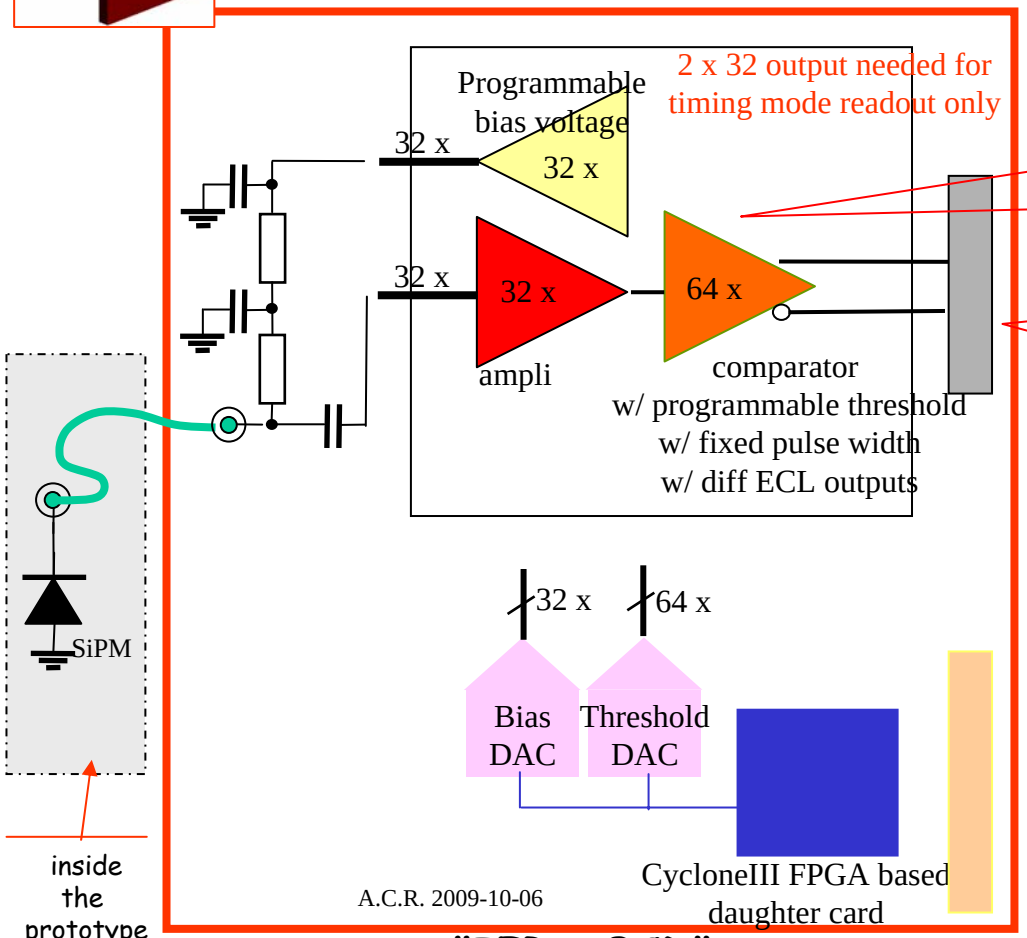


SiPM carrier PCB with NiAu plating for bonding: fits all three type of sensors being manufactured by FBK-Trento.
Sensor die glueing position is determined by a removable countermask.

Agreement exist with Dr. Giovanni Ambrosi INFN-Pg for SiPM bonding

SuperB IFR electronics : update on prototype electronics and DAQ – (b)

dimensions: VME 6U x 220mm



Outline of the "**IFR_ABCD**" card

(**A**mplifier, **B**ias, **C**omparator,**D**ataProcessing)

"**IFR_ABCD**" card features:

- ampli: two stage w/discrete components: BGA2748 + BGA2716
- discri: ADCMP562BRQ (PECL out, dual) or ADCMP563BRQ (ECL out, dual)

For the readout in timing mode of the SuperB IFR prototype it is foreseen to use two comparators at different thresholds (2.5 pe and 1.5 pe for instance) for each sensor

signal connector compatible with BaBar IFR signal cables (re-usable): KEL 8831E-034-170LD

- DAC: LTC2625CGN#PBF (I^2C, 12bit, octal)
- FPGA: Cyclone III ALTERA EP3C25Q240C8

"**IFR_ABCD**" needed for prototype readout :

1 for each of 4 BiRO planes (readout at only one end of scintillator) +

1 for each of 4 planes read with TDCs (readout at both ends of scintillator)

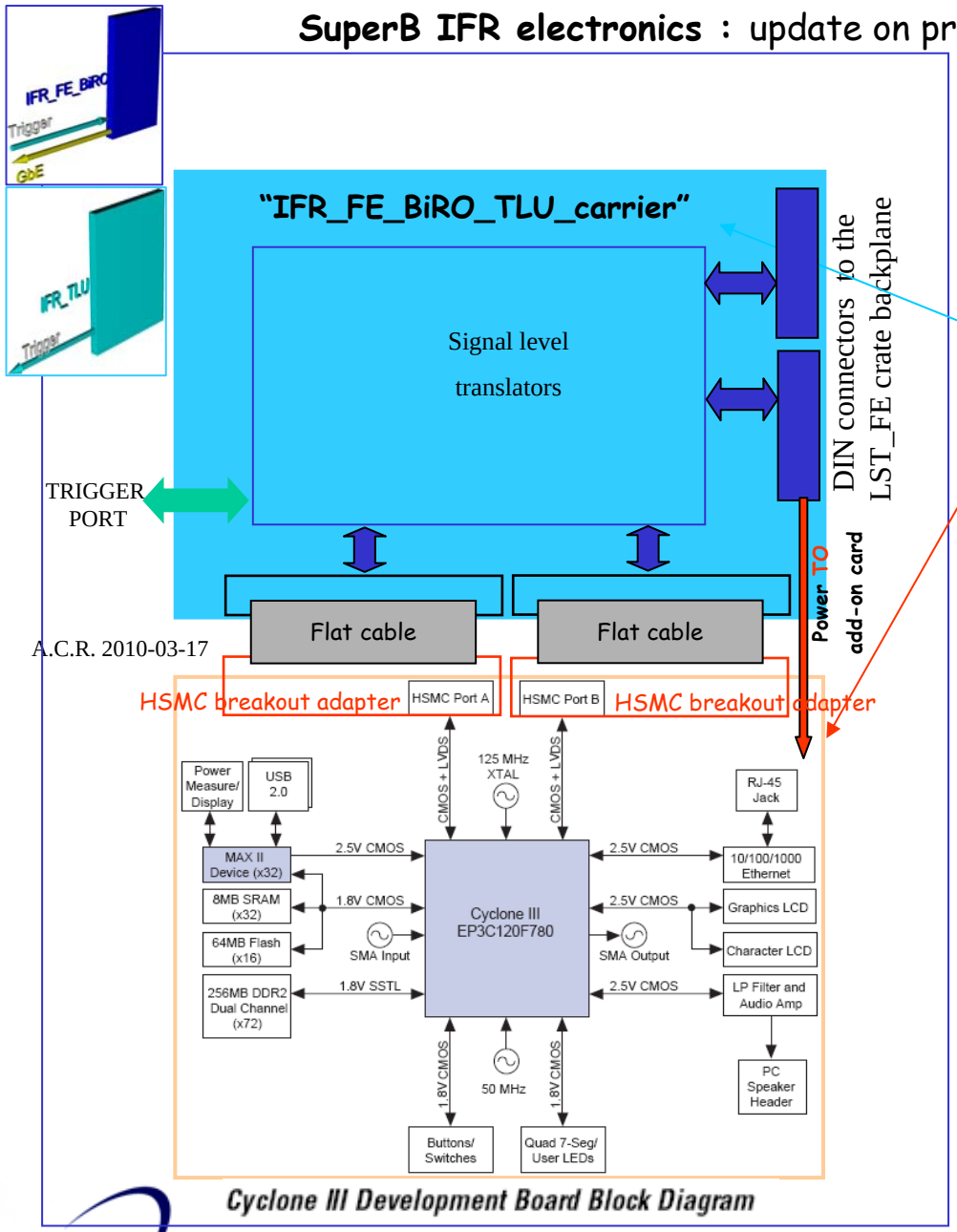
TOTAL "IFR_ABCD" cards: 8

"**IFR_ABCD**" status update :

- schematics submitted for layout; prototypes due in 6 wks
- VHDL coded firmware ready; C-language routines for the NIOS-II microcontroller being coded

IFR_ABCD card: MMIC ampli design & test, schematics, and layout pre-placement by R. Malaguti, INFN-Ferrara

SuperB IFR electronics : update on prototype electronics and DAQ – (b)



Outline of the "IFR_FE_BiRO_TLU" module

"IFR_FE_BiRO_TLU" module features (new):

The functions of the IFR_FE_BiRO and of the IFR_FE_TLU cards are combined into a single system made of

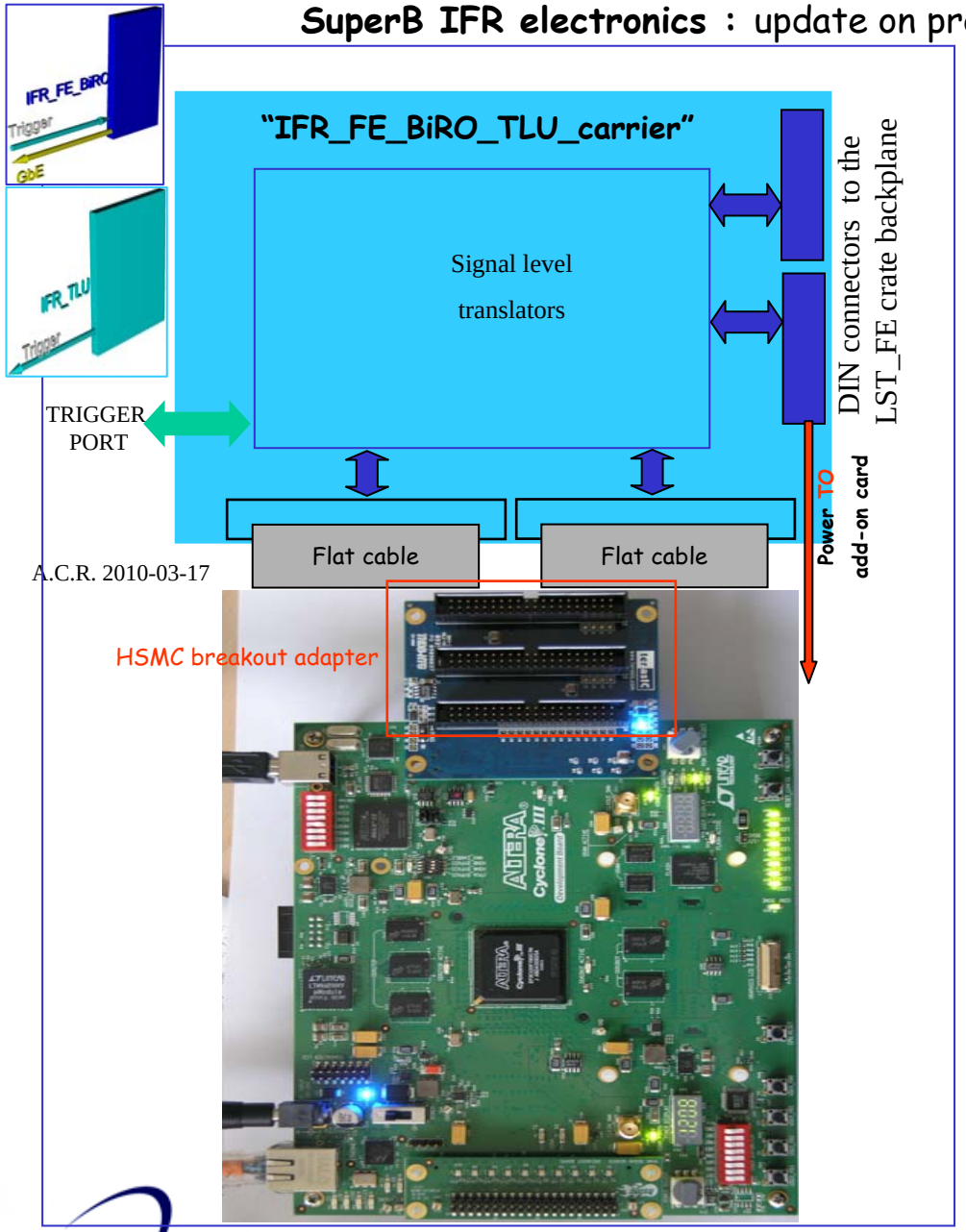
- a **carrier** card which fits in the "LST_FE" crate (6U x 220mm depth)
- an **add-on** card : it's simply the ALTERA Cyclone III development kit (**DK-DEV-3C120N**) equipped with breakout adapters for the kit's HSMC connectors

The **carrier** card hosts level adaptors and application specific I/O ports which allow the **add-on** card to:

- receive power
- receive the "fast OR" signals from the "ABCD" cards to generate triggers from
- generate and distribute triggers (also to the TDC system)
- generate and distribute clock and reset signals (also to the TDC system)
- poll data from the "ABCD" cards
- configure the programmable resources on the "ABCD" cards
- connect to the host PC running the DAQ software via ethernet (tcp/ip)

Total "IFR_FE_BiRO_TLU" needed for the prototype readout: 1

SuperB IFR electronics : update on prototype electronics and DAQ – (b)



Outline of the "IFR_FE_BiRO_TLU" module

"IFR_FE_BiRO_TLU" module features: (continues)

The FPGA on board the **add-on** card is connected to the RUN CONTROL/DAQ PC of the prototype test setup via an Ethernet port.

The FPGA features a NIOS-II microcontroller which implements the full TCP/IP stack.

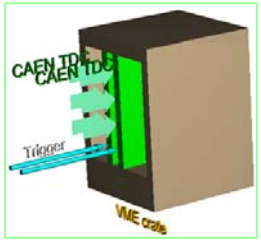
The NIOS-II receives commands (i.e. START, STOP, INIT) from the RUN CONTROL/DAQ PC on a TCP server socket and sends data to a TCP server socket on the PC. Data is collected through the LST_FE backplane from the "ABCD" cards upon a trigger request. The data collection section of the FPGA is coded in VHDL.

The FPGA of the add-on card generates the timing (clock and reset) for all the digitizers and handles the trigger distribution as well.

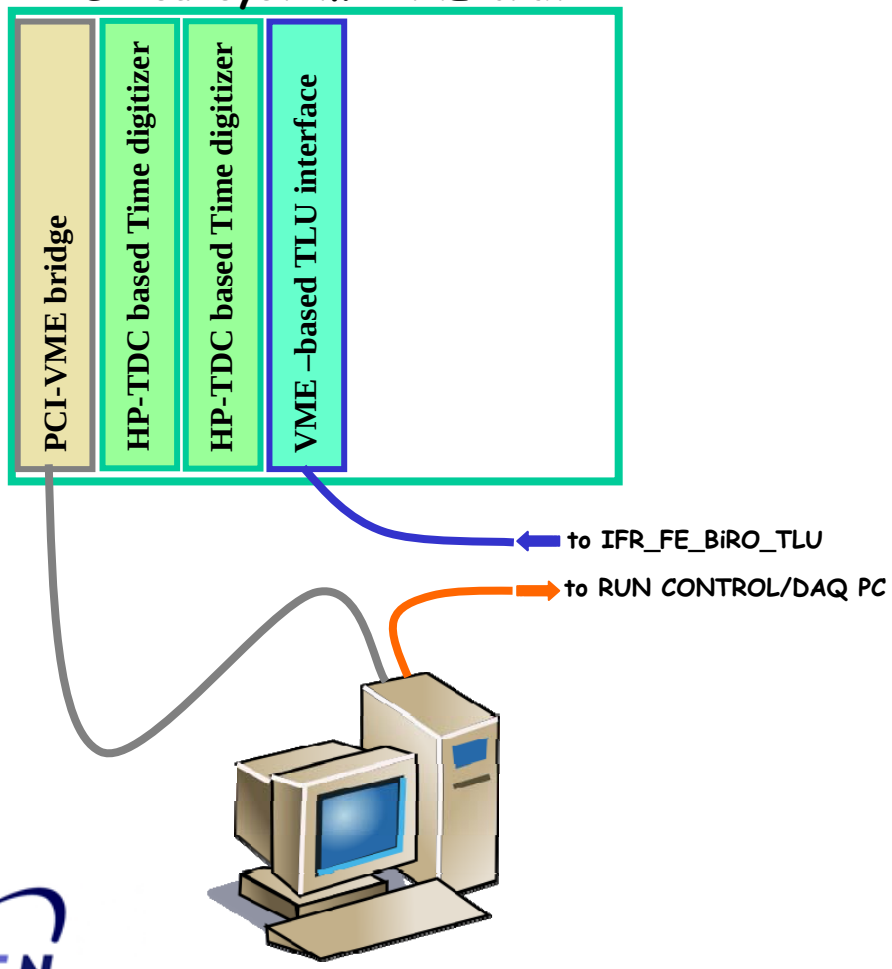
"IFR_FE_BiRO_TLU" status update :

- schematics of the "carrier card" is almost finished (pending FPGA pin assignment)
- "carrier card" layout turn around time expected to be ~3 wks
- "carrier card" PCB production and stuffing expected to be ~3 wks
- C-language routines for the NIOS-II microcontroller are coded and tested; VHDL coded firmware is being developed;

SuperB IFR electronics : update on prototype electronics and DAQ – (b)



"TDC subsystem" VME crate



"TDC subsystem" features:

The TDC subsystem uses 2 commercial TDC modules based on CERN's HP-TDC to digitze the time of arrival of the pulses from the "ABCD" boards.

The TDC subsystem will also use a VME-based module to interface to the "IFR_FE_BiRO_TLU" and receive trigger/timing signals

The TDC subsystem VME crate will be controlled and read out by the "TDC-PC" via a PCI-VME bridge.

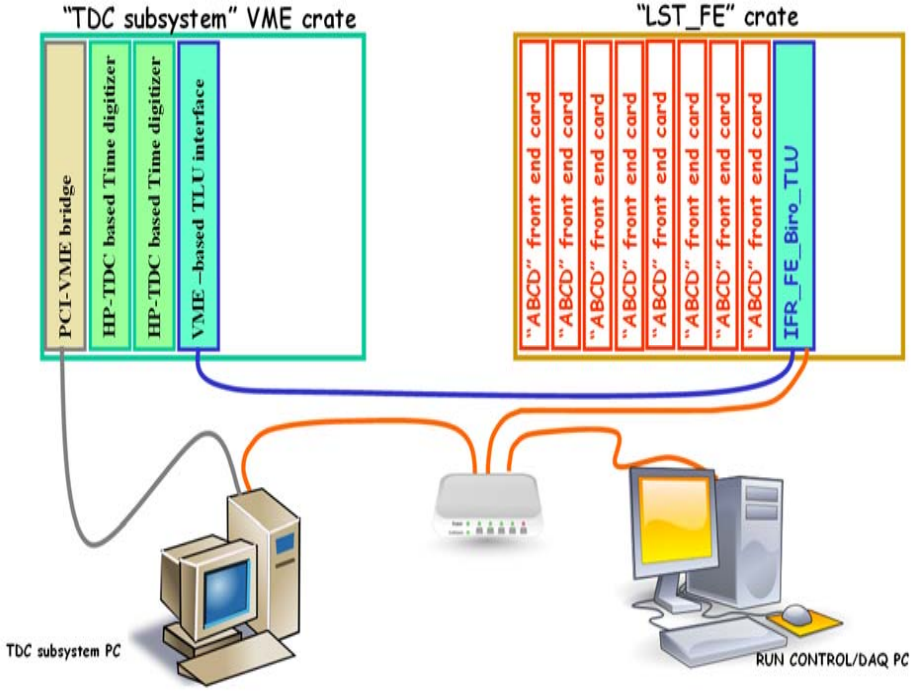
The TDC_PC will then send the triggered data to the RUN CONTROL/DAQ PC via a TCP/IP connection.

"TDC subsystem" status update :

- the readout of a VME TDC is operating
- code must be written to format the TDC measurements into formatted events
- the VME based – TLU interface module exists but needs a simple firmware upgrading

SuperB IFR electronics : update on prototype electronics and DAQ – (c)

outline of the run control / daq system for the IFR prototype



During the run initialization phase (INIT) the RUN CONTROL / DAQ PC sends commands and configuration parameters over Ethernet to the TDC-PC and the "IFR_FE_BIRO_TLU" to properly configure the programmable features of the system.

The "**IFR_ABCD**" cards generate trigger primitives which are:
• the OR of all "high threshold" channels from a plane read out in "timing" mode
• either the (OR of the X-view) OR (OR of the Y-view) or (choice made during INIT phase)
the (OR of the X-view) AND (OR of the Y-view) for the channels from a plane readout in binary mode
These primitives are collected by the "IFR_FE_BIRO_TLU" over the backplane of the "LST_FE" crate.

The "**IFR_FE_BiRO_TLU**" card generates a trigger if the primitives and the LUT loaded during the INIT phase require so. The trigger is sent also to the **VME_based TLU interface** and from that to the TDCs. A **TDC_BUSY** signal is set in the **VME_based TLU interface** and returned to the **IFR_FE_BiRO_TLU**, which uses it, together with its own **BiRO_BUSY**, to block further triggers.
When the TDC-PC and the **IFR_FE_BiRO_TLU** systems have readout the digitizers the BUSY bits are cleared and a new trigger can be generated and served as the data from the previous one is being transferred over the Ethernet port to the RUN CONTROL/DAQ PC.

Each event data block is framed by an HEADER and a TRAILER containing a local trigger count, incrementing with each new trigger served **and a trigger time-stamp locally generated; this should be sufficient**, being the whole system synchronous, **to guarantee the right matching of events from the two subsystems**. Eventually an additional **trigger_ID** tag could be distributed by the **IFR_FE_BiRO_TLU** to the **VME_based TLU interface** and from that be added to the TDC data packet

SuperB IFR electronics : update on prototype electronics and DAQ – (d)

Conclusions:

Work is in progress; the development of the readout electronics for the prototype should be completed in time for the delivery of the SiPM sensors.