First Test Results Of MIMOSA-26,
A Fast CMOS Sensor With Integrated Zero Suppression And Binary Output

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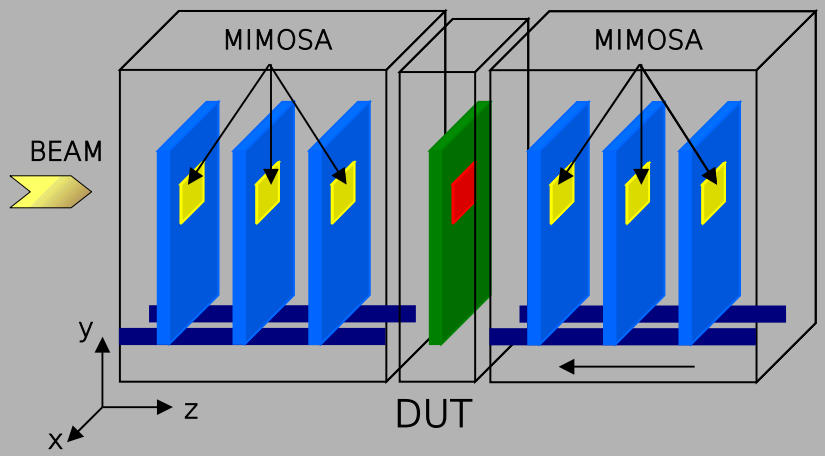
On behalf of the groups:

- IPHC, Strasbourg
- IRFU-CEA, Saclay

- Motivations for such a sensor
- MIMOSA 26 architecture
- Tests and results
- Further developments
- Integration studies

Motivations for such a sensor

- EUDET
  - ✗ 6th Framework Programme of EC
    - → Infrastructure supporting detector R&D for ILC
    - → See I.Gregor's talk on Thursday N45-2
  - ✗ High resolution pixellated beam telescope
    - → Track extrapolation @ DUT σ~2µm
    - → Sensitive area 2cm^2 with 1 dim~2cm
    - → Binary readout allowing 10 Kframes/s
    - → Up to 10^6 hits/cm^2/s
  - ✗ Final telescope for 2009



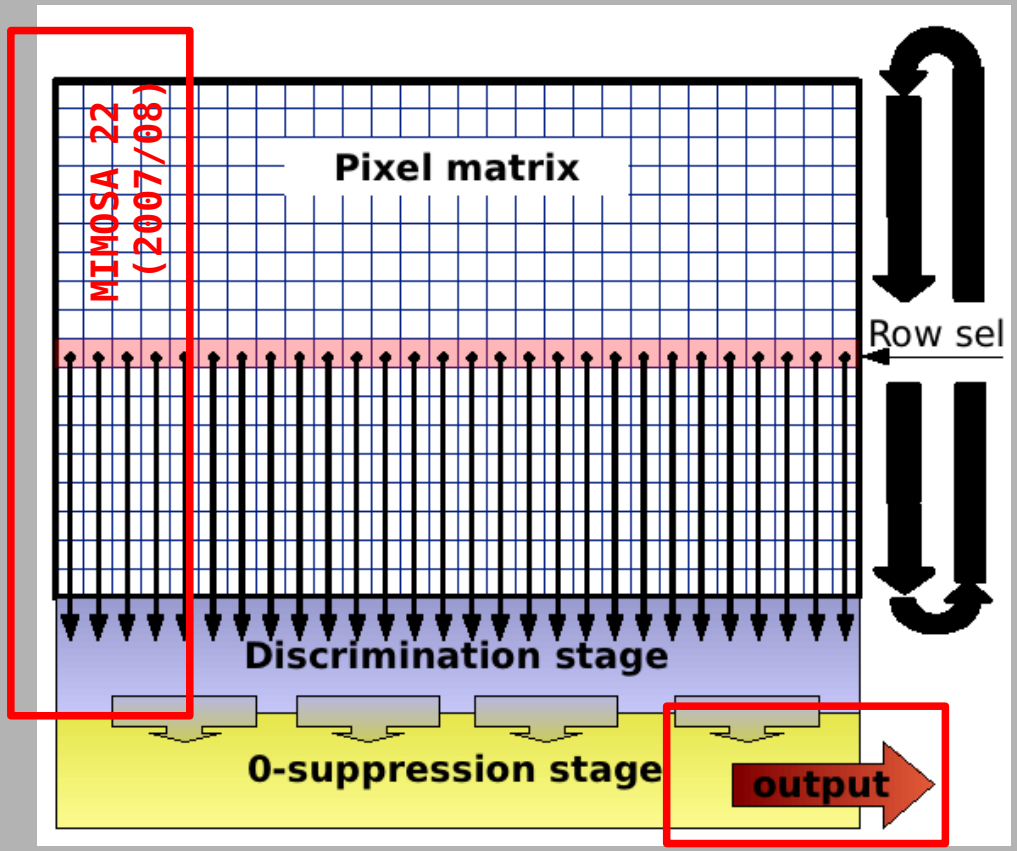
- Vertex Detectors
  - ✗ "Common" specifications
    - → High granularity: pitch < 30µm
    - → Fast: readout ~ 100-200 µs
    - → Low occupancy: few %
    - → Low material budget: $\ll 10^{-2}$ X_0
    - → Low power dissipation: 100 mW/cm^2 , ~30°C operation
    - → Mild radiation tolerance < Mrad and < 10^{12} n_{eq}/cm^2
  - ✗ STAR @ RHIC - 2010
  - ✗ CBM @ FAIR – 2012
    - → Readout < 10 µs
    - → Several Mrads and 10^{14} n_{eq}/cm^2
  - ✗ ILD @ ILC > 2012
    - → First layer readout ~ 25 µs

→ Development of a fast binary readout CMOS sensor

MIMOSA 26 architecture

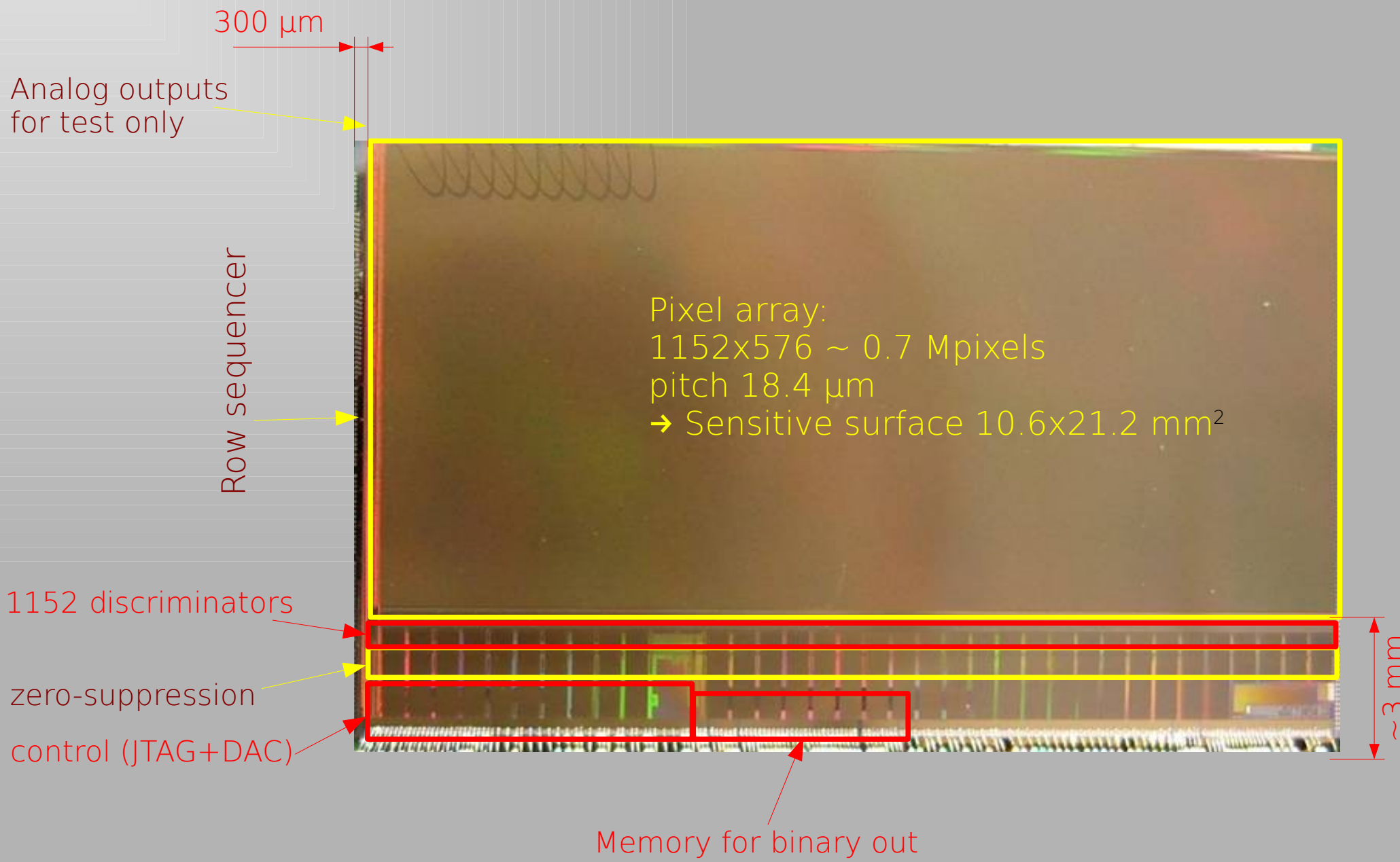
- Fabrication
  - ✗ CMOS 0.35 µm OPTO process
  - ✗ Designed in 2008, Return from foundry early 2009

- Column parallel readout
  - ✗ Rolling-shutter mode
    - ➔ 80 Mhz clock ➔ 112 µs integration
  - ✗ One pixel contains:
    - ➔ Amplification
    - ➔ Double Sampling
  - ✗ 1 discriminator per column with
    - ➔ Offset compensation
    - ➔ Correlated Double Sampling
- Zero-suppression stage
  - ✗ Parallel sparse data scan ➔ Two memories ➔ Serial readout
  - ✗ Data compression factor x10 to 1000 depending on occupancy



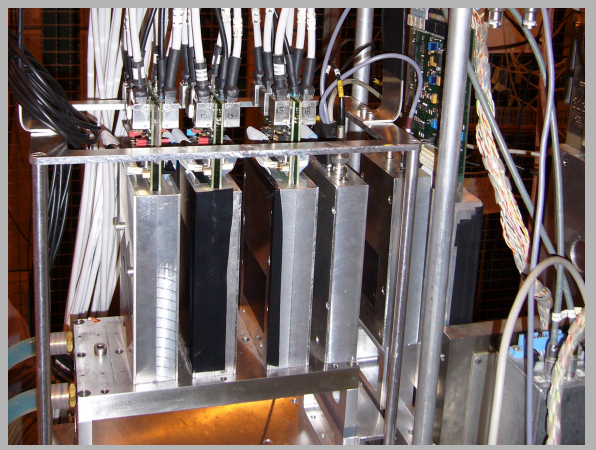
SUZE 01
(2007)

MIMOSA 26 architecture



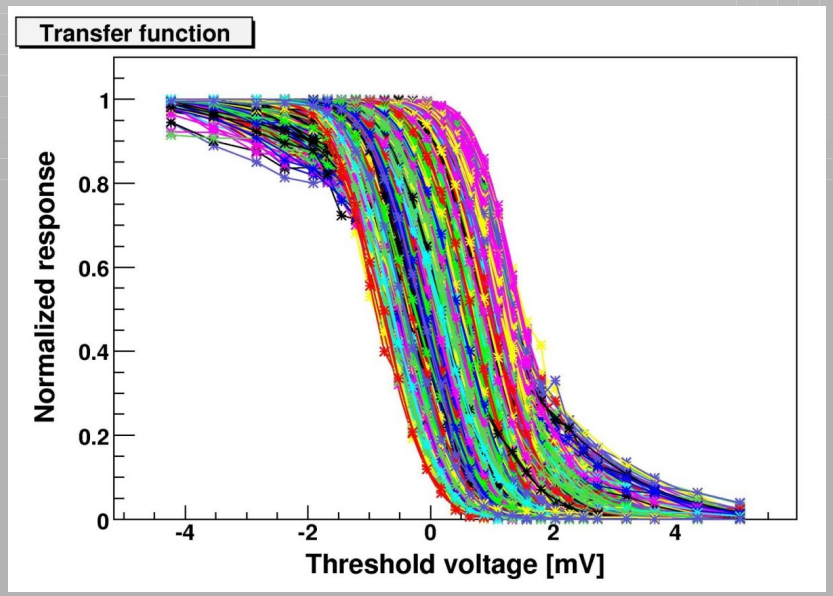
Test conditions

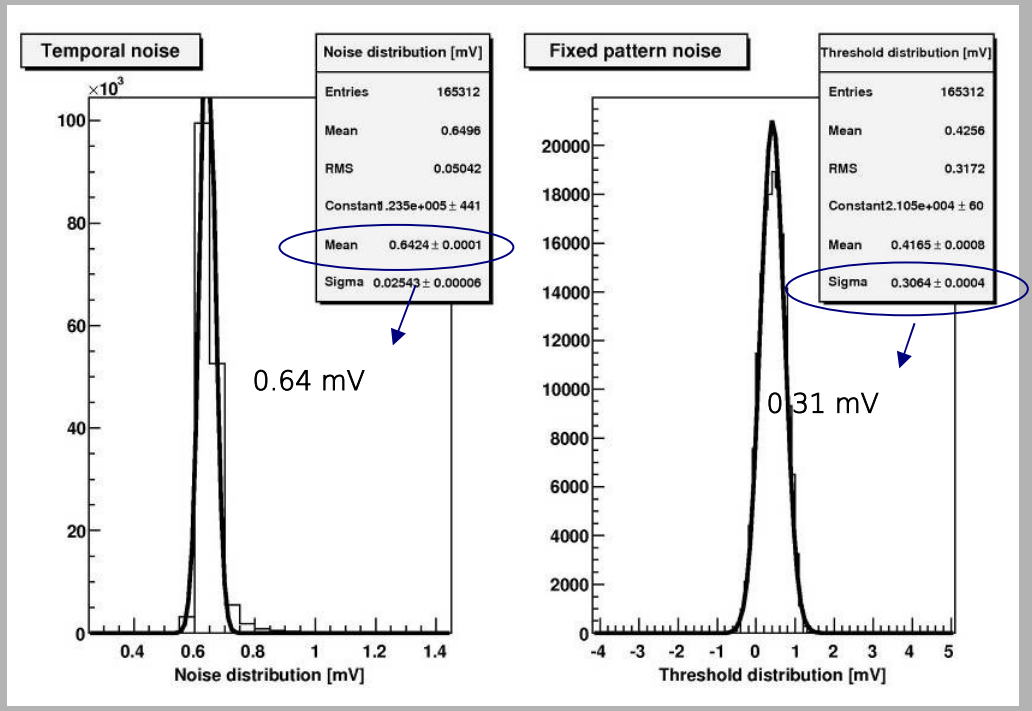
- Laboratory tests
  - ✗ Operation at 20°C
  - ✗ Clock 20 ➔ 80 Mhz
  - ✗ Noise measurements…
  - ✗ Charge collection efficiency with analog test outputs identical to MIMOSA 22
  - ✗ Validation of zero-suppression with input patterns
  - ✗ Power dissipation (static) 300 mW/cm^2 independent on #rows (dynamic ~200 mW @ 1% occupancy)
- Sensors
  - ✗ Non-irradiated
  - ✗ Over 30 sensors from 2 wafers tested in lab
    - ➔ Yield for functional sensors ~90%
  - ✗ 1 wafer thinned down to 120 µm
- Beam tests
  - ✗ SPS beam: 120 GeV π^-
  - ✗ 6 sensors used in beam test = 5 reference planes → track + 1 DUT
  - ✗ Operation at 20°C
  - ✗ Clock 20 and 80 Mhz
  - ✗ 90-20 deg incidence
  - ✗ Threshold scan 4.5 to 10 x noise
    - → Fake hit rate
      Efficiency
      spatial resolution



MIMOSA 26 - noise

- Tests in lab
  - ✗ 20 MHz to 80 Mhz
  - ✗ Temporal noise mainly due to pixels: 0.6-0.7 mV
  - ✗ Fixed pattern noise mainly due to discriminator: 0.3-0.4 mV
  - ✗ ENC ~ 13-14 e^- equivalent to MIMOSA 22 noise

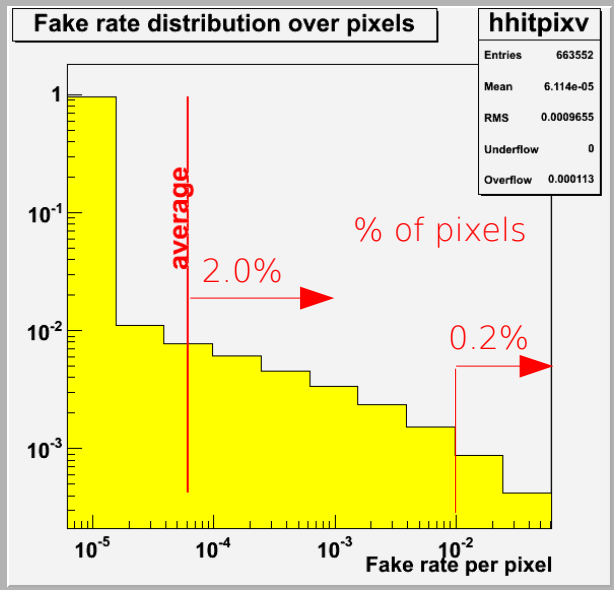




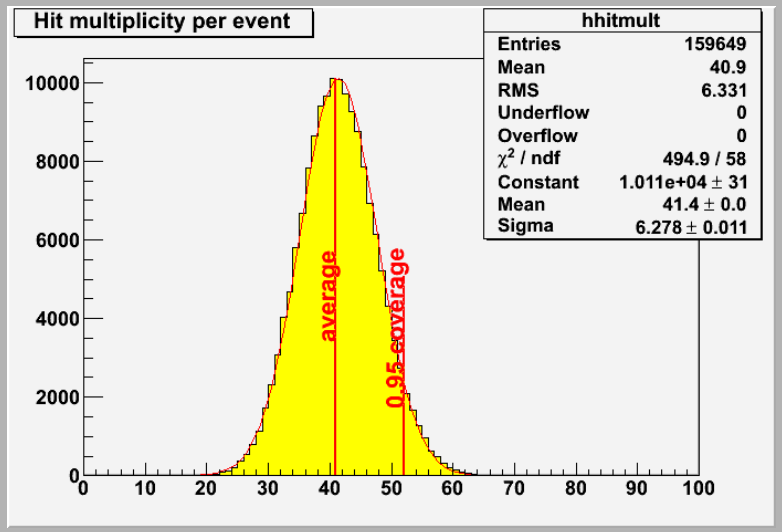
For ¼ of the full matrix

MIMOSA 26 – Fake / Efficiency

- Fake hit rate
  - ✗ Fake hit = Single pixel firing with no beam
  - ✗ Counts over the full matrix over ~150000 frames
  - ✗ Gaussian behavior per event



Threshold ~ 6xnoise



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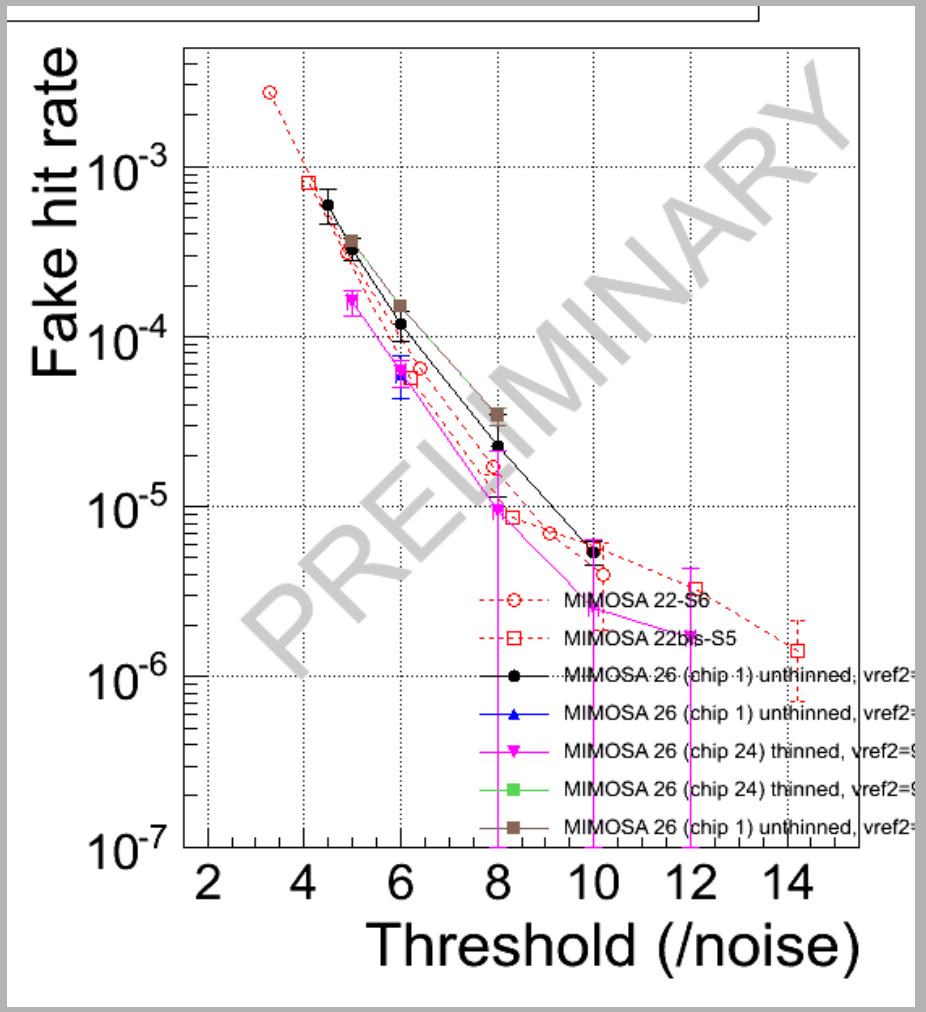

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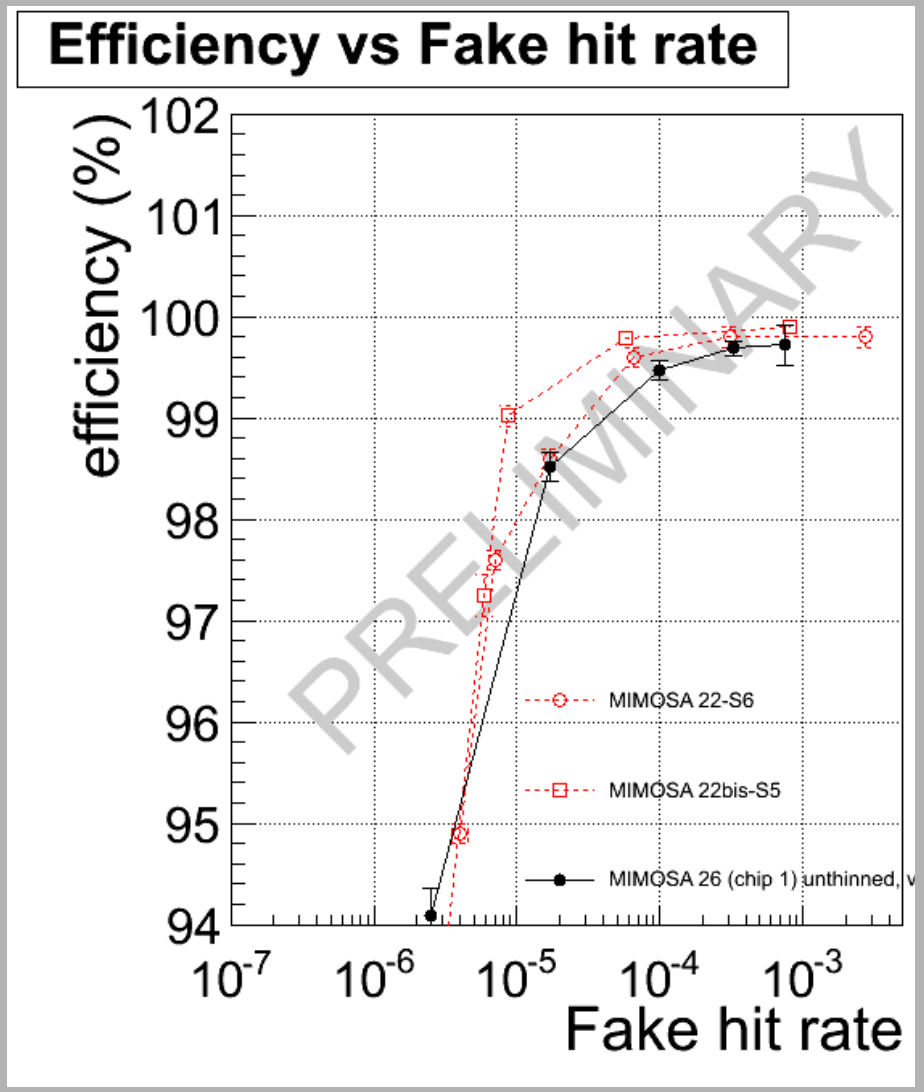
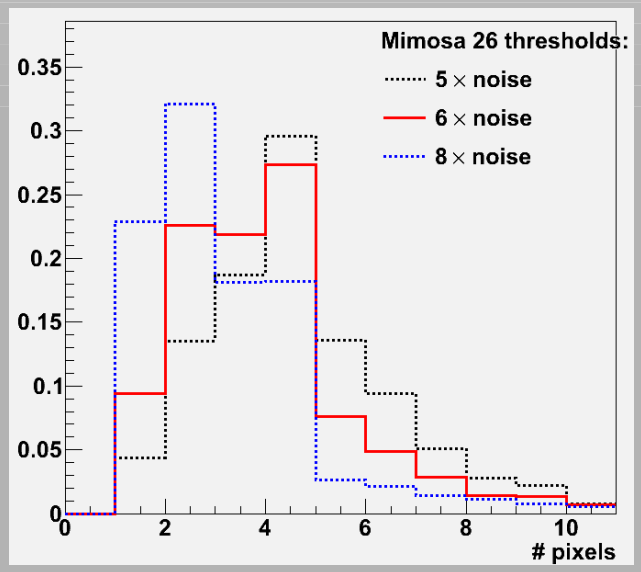
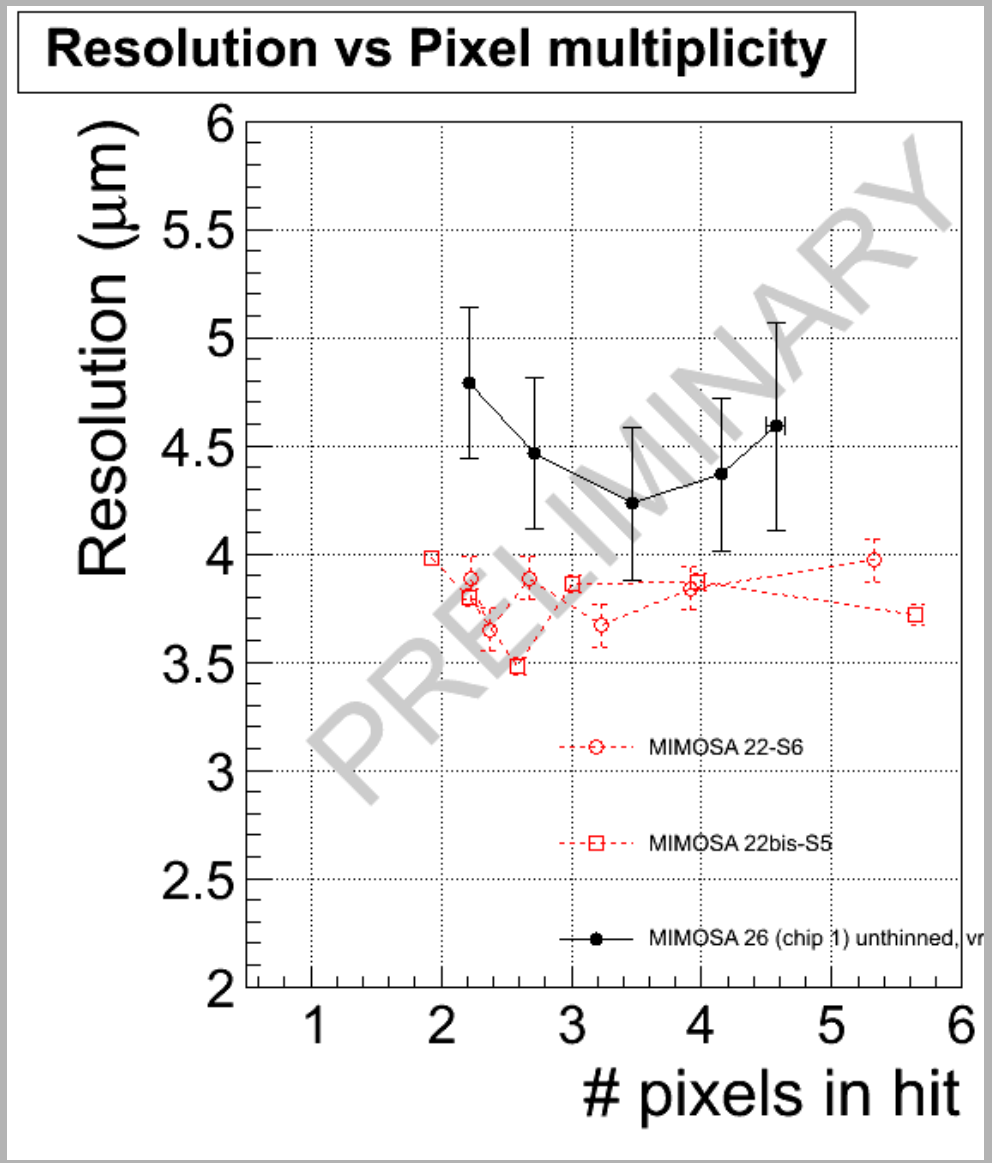
- Efficiency
  - ✗ Efficiency defined as: #tracks assoc. with a hit over total #tracks
  - ✗ Fake rate computed in the scintillator area
  - ✗ Not yet checked over the full sensor area but only 4x4 mm^2
  - ✗ Efficiency 99.5% reachable for fake rate 10^{-4}/pixel



MIMOSA 26 – spatial resolution

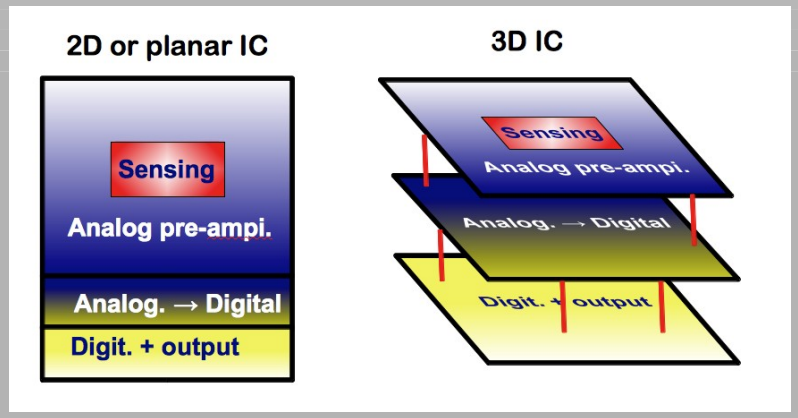
- Still very preliminary
  - ✗ Due to rough position algorithm
  - ✗ Track extrapolation @ DUT
    $\sigma = 2.1 \pm 0.4$ µm
  - ✗ Prelim. resolution of Mimosa26 worst by 0.5 µm / MIMOSA 22
    - ➔ Though average <#pixels/cluster> is the same
    - ➔ Effect of inhomogeneities in a large matrix ?

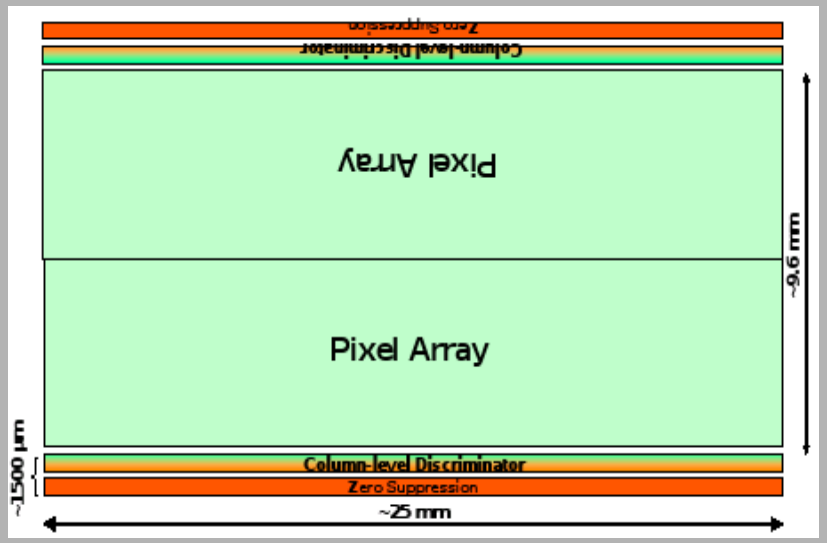




Further developments

- Sensor architecture
  - ✗ Two sided readout and/or elongated pixels
    - → Increase readout speed
  - ✗ Replace discri. with few bits ADCs
    - → Same resolution for larger pixel pitch
  - ✗ 3D integrated circuits
    - → Increase readout speed
    - → Decrease dead areas
    - → Optimization of techno. per function





- Process technology
  - ✗ Lower feature size ≤ 0.18 µm
    - → Increase readout speed
    - → Decrease dead areas
    - → Decrease power dissipation
  - ✗ High resistivity epitaxial layer
    - → Improve tolerance / non-ioniz. rad.

See Wojciech Dulinsky's talk (same session N22)
See Yavuz Degerli's poster (session N25-167)

Integration topic

- In a beam telescope
  - ✗ PCB enough for 1 or 2x2 sensors
- In a vertex detector
  - ✗ Opposite constraints
    - → Electrical connection + Mechanical support + Power dissipation
    - → Material budget
  - ✗ ILC goals
    - → Single point resolution ~ 3µm
    - → Double sided ladder
    - → Material budget < 0.3% X_0

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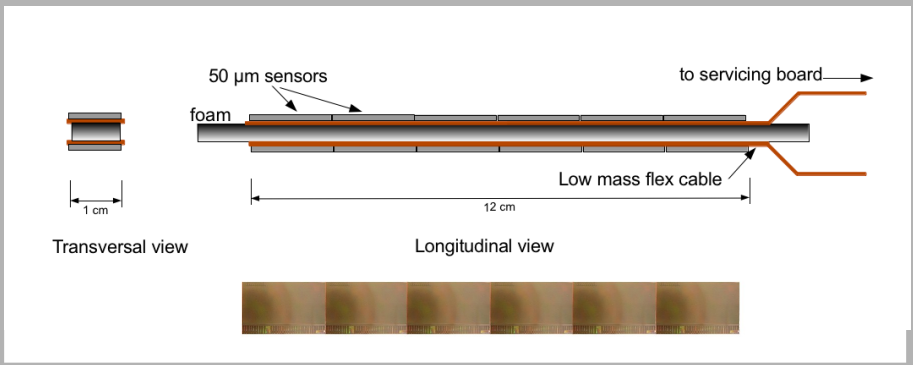
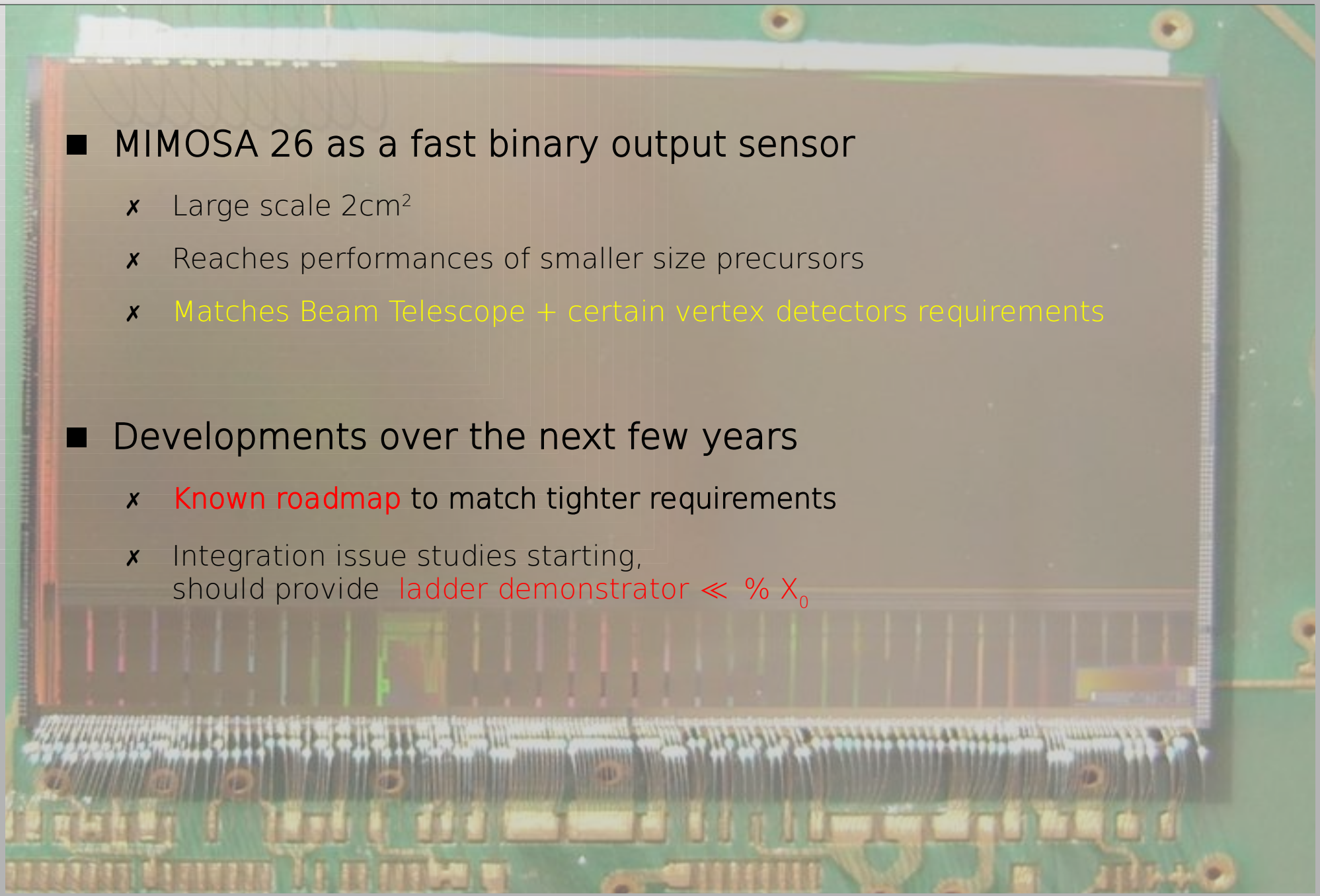


- PLUME project

Strasbourg, DESY, Oxford, Bristol, …

  - ✗ Assume
    - → air flow cooling
    - → Double sided ladders
    - → Power cycling operation
    - → Ladder = 2 modules on SiC
    - → Sensors thinned down to 50 µm
  - ✗ 2009:
    - → Module = 2 MIMOSA 20, 2x1cm^2 (analog sensors)
    - → Ladder = 0.6 % X_0
    - → Test beam for pointing accuracy study (start next week!)
  - ✗ 2010 - 2012
    - → Module = 6 large MIMOSA
    - → Decrease material budget
    - → Many tests ahead
      - Mechanical stability
      - Thermal distribution
      - Alignment

Conclusion



- MIMOSA 26 as a fast binary output sensor
  - ✗ Large scale 2cm^2
  - ✗ Reaches performances of smaller size precursors
  - ✗ Matches Beam Telescope + certain vertex detectors requirements
- Developments over the next few years
  - ✗ Known roadmap to match tighter requirements
  - ✗ Integration issue studies starting, should provide ladder demonstrator $\ll$ % X_0

ADDITIONAL SLIDES