Silicon/Vertex Detector

RD_FA Referee Meeting
23 settembre 2019

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Per il work-package on silicon detectors

Istituto Nazionale di Fisica Nucleare
Sezione di Milano

UNIVERSITÀ DEGLI STUDI DI MILANO
DIPARTIMENTO DI FISICA

Goal of the WP

- Till now the silicon/vertex detector work-package was mainly concerned with the exploration of technologies suitable for the high-precision requirement of an e^+e^- collider
- For example, from CepC CDR:
  - Impact parameter resolution

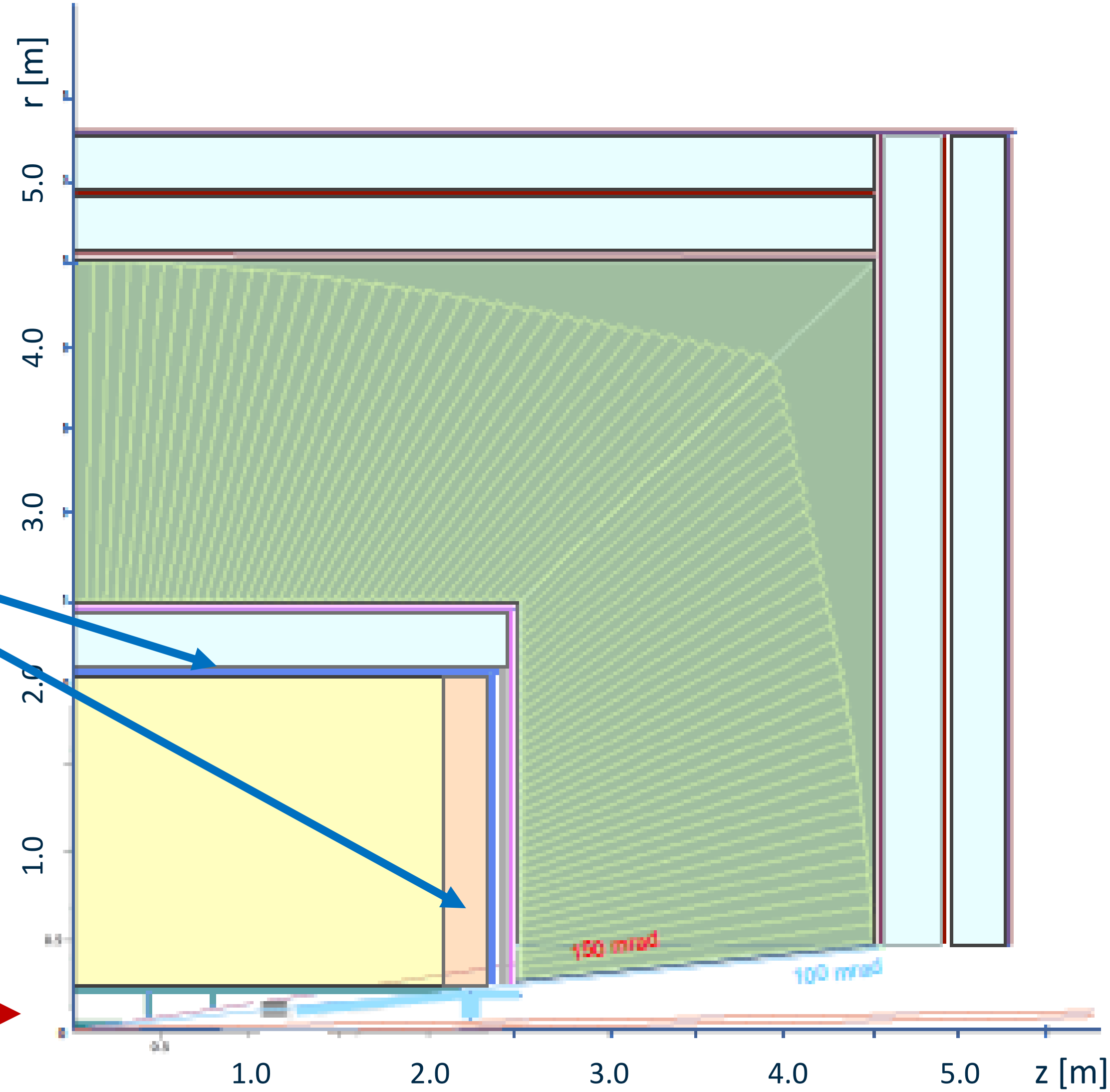
$$\sigma_{R\varphi} = 5\mu\text{m} \oplus \frac{10\mu\text{m} \cdot \text{GeV}}{p \sin^{3/2} \vartheta}.$$

    - Intrinsic resolution of first point **<3 µm**
    - Innermost layer radius **16 mm**
    - Material **<0.15% X_0/layer**
    - Time resolution **<25 ns** (run at the *Z*)
    - Power dissipation **< 50 mW/cm^2**
  - Momentum resolution

$$\sigma\left(\frac{1}{p_T}\right) = 2 \times 10^{-5}\text{GeV}^{-1} \oplus \frac{0.001}{p \sin^{3/2} \vartheta}.$$

The IDEA Detector layout

- Beam pipe (R~1.5 cm)
- **VTX:**
  - 4-7 Depleted MAPS layers
  - **Acceptance: θ>150 mrad**
- DCH: 4 m long, R 35-200 cm
- **Outer Silicon Layer**
- SC Coil : 2 T, R ~2.1 m
- Preshower: ~1 X_0
- Dual Readout calorimeter: 2 m/7 λ_{int}
  - **Acceptance: θ>100 mrad**
- Yoke + muon chamber



Technologies under investigation

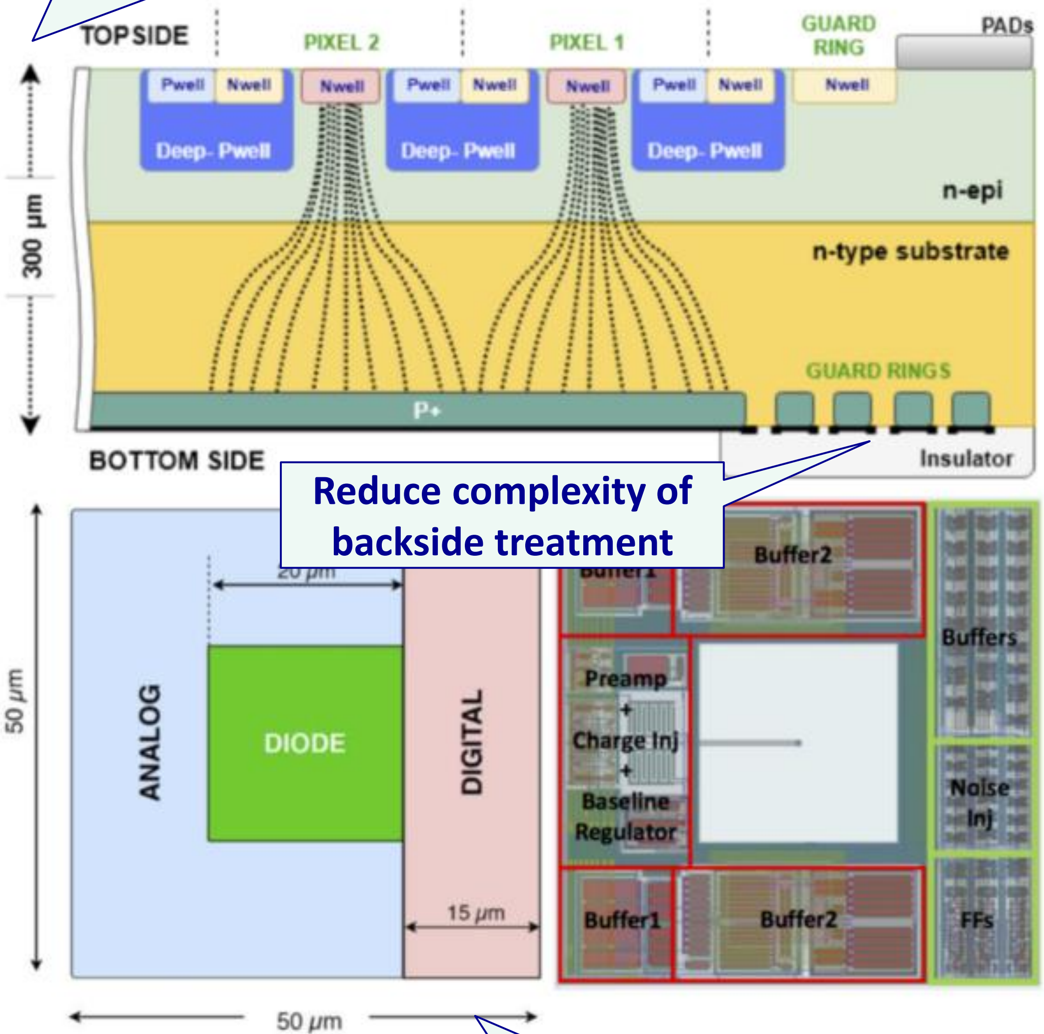
- Exploring CMOS technologies, since they have the potential for low cost/high throughput
- VTX: Depleted Monolithic Active Pixels
  - Fast signal
  - Possibility for very thin detectors (low material)
  - Small pitches already realized
  - CSN5 developments: SEED-ARCADIA
    - One AIDA++ EoI submitted
  - CSN5+CSN1 developments: HVR_CCPD-ATLAS
    - One(+) AIDA++ EoI submitted
- Outer tracker:
  - Proposing passive CMOS sensor (productions by ATLAS/CMS on going, part of the ATLAS pixel detector market surveys)
    - One AIDA++ EoI submitted

Currently funded by CSN5

Small requests this year

SEED⟶ARCADIA Sensors

Thinning of sensor



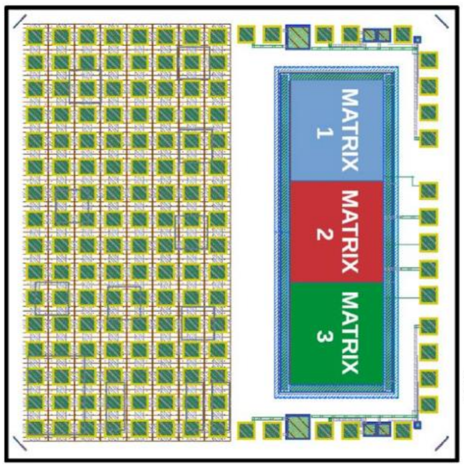
Reduce complexity of backside treatment

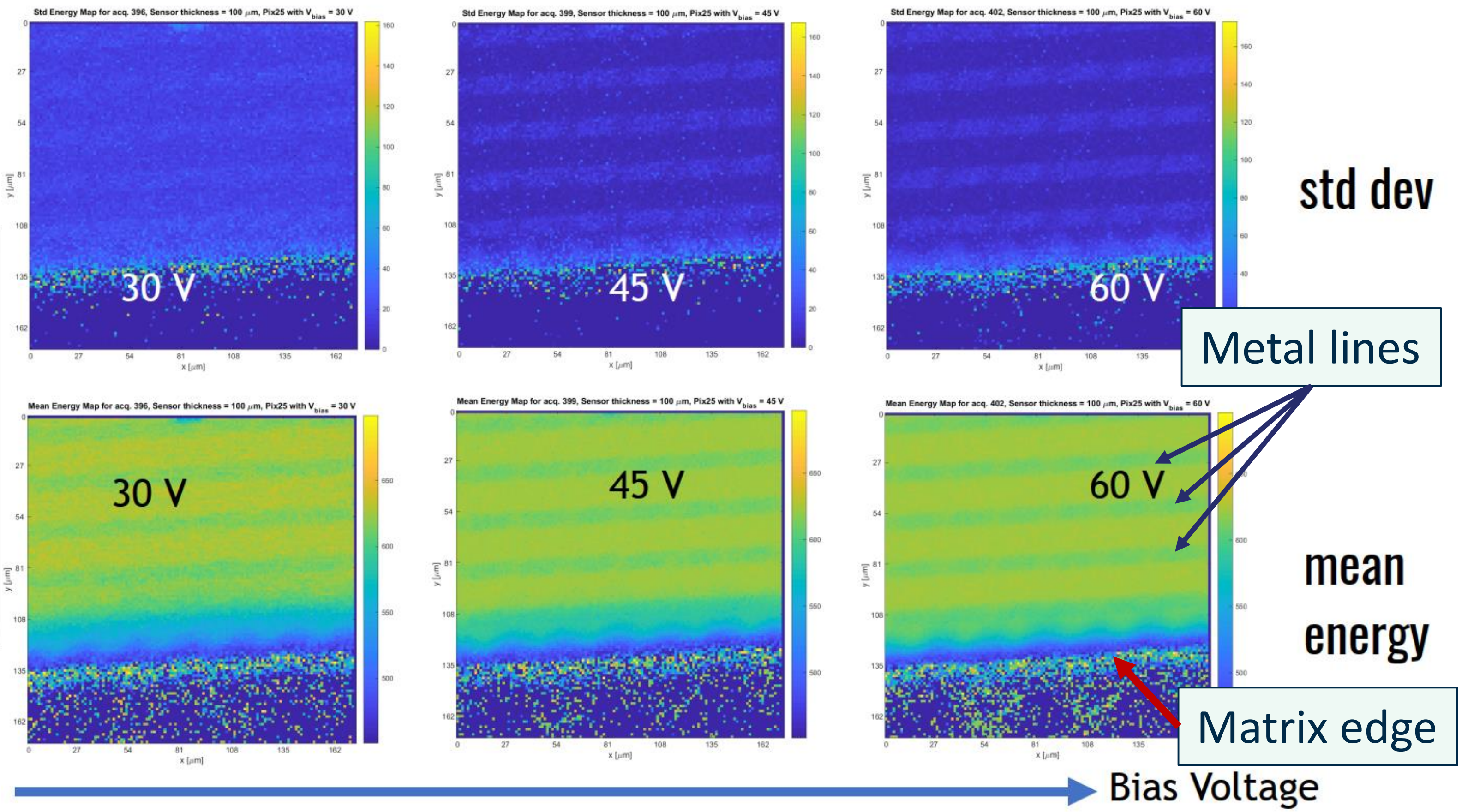
Smaller size

MAIN REQUIREMENTS OF MATISSE	
Technology	CMOS BSI 0.11 μm
Voltage supply	1.2 V
Measurements	Hit position Energy Loss
Number of channels	24×24
Input dynamic range	up to 24 ke$^-$
Sensor capacitance	$\sim$ 40 fF
CSA input common mode voltage	$>$ 600 mV
Local memories	2 ($\sim$70 fF each)
Noise	$<$ 100 e$^-$
Shutter type	Snapshot shutter
Readout type	Correlated Double Sampling Double Sampling
Readout speed	up to 5 MHz
Other features	Internal test pulse Mask mode Baseline regulation

SEED detector characterization

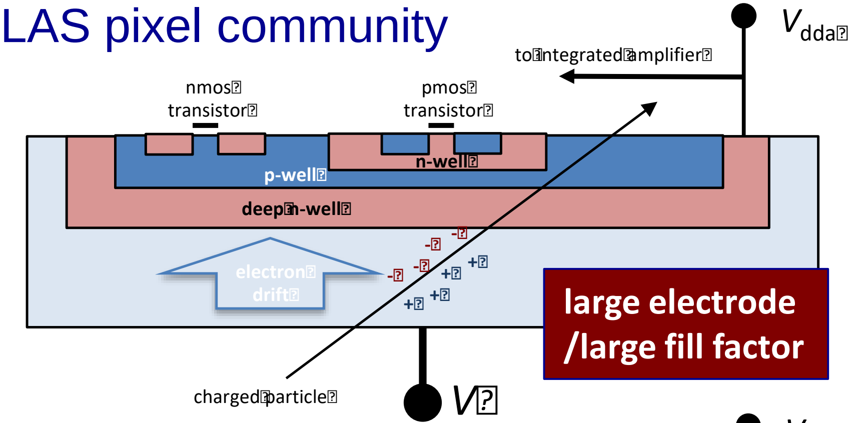
- Microbeam scans at RBI – Zagreb
  - Study charge collection of SEED sensors
  - 2 MeV protons → good charge collection uniformity
  - Pseudomatrices of 10 µm – 50 µm pitch, 100 µm – 400 µm sensor thickness



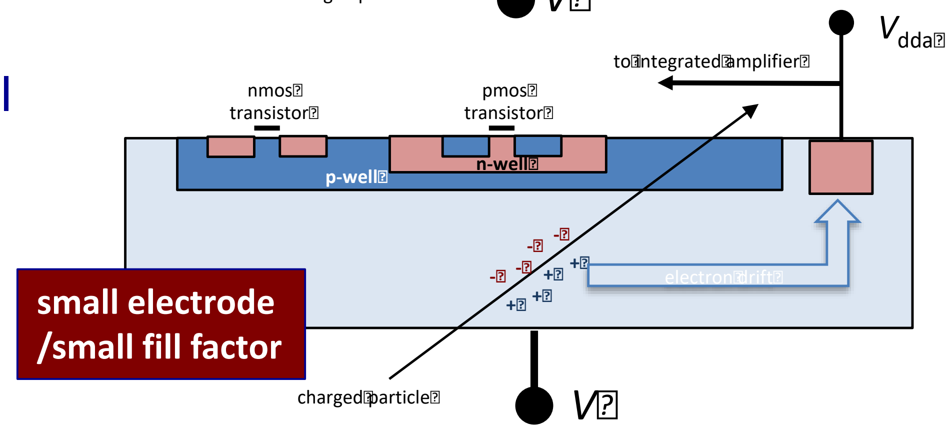


ATLAS developements

- Different monolithic devices developed within the ATLAS pixel community
- Front-end electronics **inside** the collecting well
  - **uniform charge collection**
  - **short drift path → less trapping**
  - **large electrode capacitance** ~100 fF, due to parasitic capacitance between the deep wells
  - LFoundry, AMS/TSI technologies



- Front-end electronics **outside** the collecting well
  - **non uniform drift field**
  - **long drift path → more sensitive to trapping**
  - **small electrode capacitance** <10 fF
  - TowerJazz



- CMOS option reviewed in February 2019, in view of the overall ATLAS ITk schedule

From the review report:

- Excellent R&D being done on the monolithic CMOS sensors
  - will be important for the field in the longer term
  - but available evidence suggests it will not converge in time for this iteration of the Pixel Upgrade

Moving developments to RD_FA

Completing ATLAS R&D: ATLASPIX3

- **AMS 180 nm HV** technology **now moved to TSI** (USA) compatible process
- Sensor radiation hardness verified on several prototypes till 2×10^{15} n/cm^2

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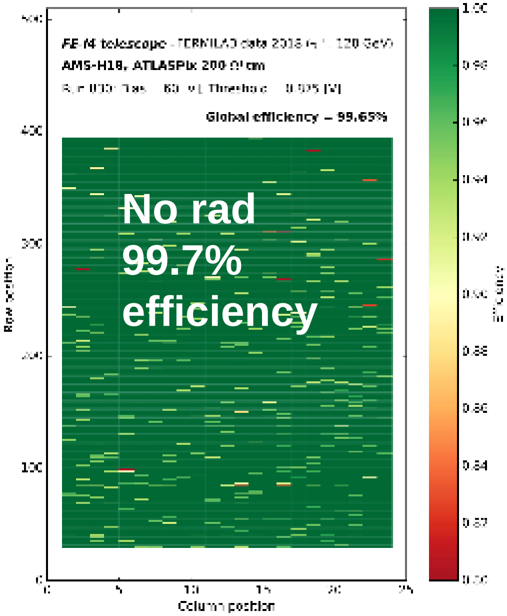
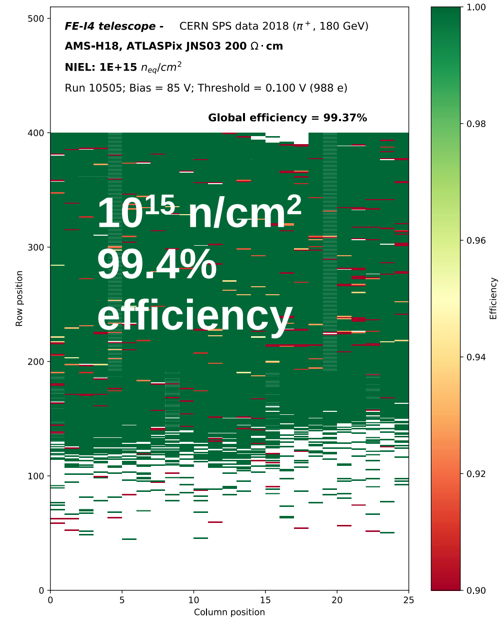
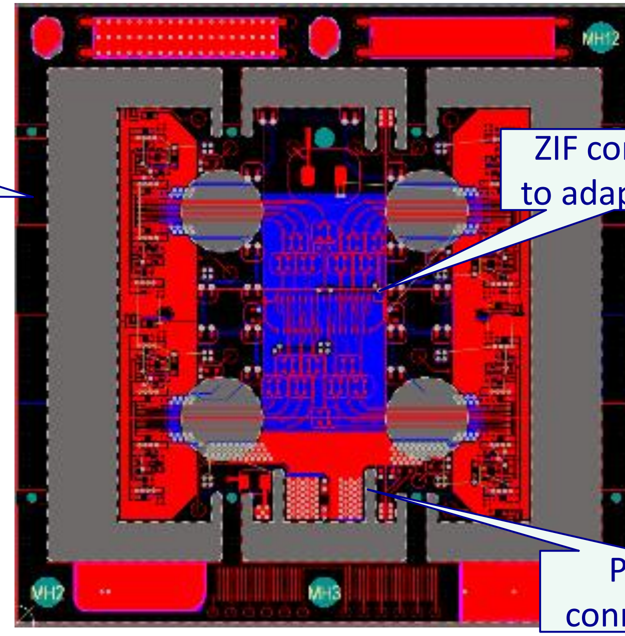


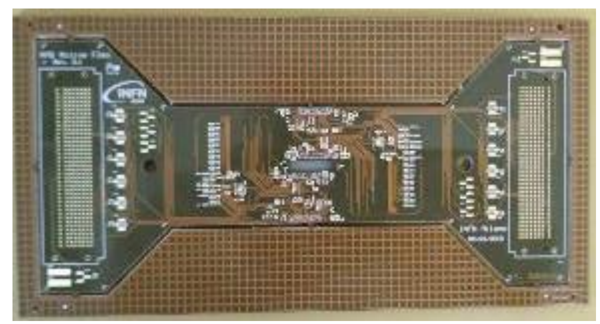


- Full size matrix: 20.2mm x 21mm
- Compatible with most ATLAS requirements:
  - 50×150 µm^2 pixel size, **large fill factor**
  - Column drain readout (FE-I3 like)
  - Compatible with RD53A serial powering schema and readout protocols
- **Submitted to TSI in April, first chips available now**

ATLASPIX3 Modules



- Interest of this new prototype:
  - Readout on full scale matrix
  - **System aspects:**
    - **Serial powering**
    - **Multi-chip module**
- Develop a multichip hybrid following a layout similar to the ones for the hybrid ATLAS quad modules
  - Challenges: accurate chip placement + flexibility
  - General agreement: hybrid by Milano, adapter+readout firmware by Lancaster
  - If successful, considering a similar development for the TowerJazz Monopix prototype (small fill factor) to be submitted at the end of the year (see backup).



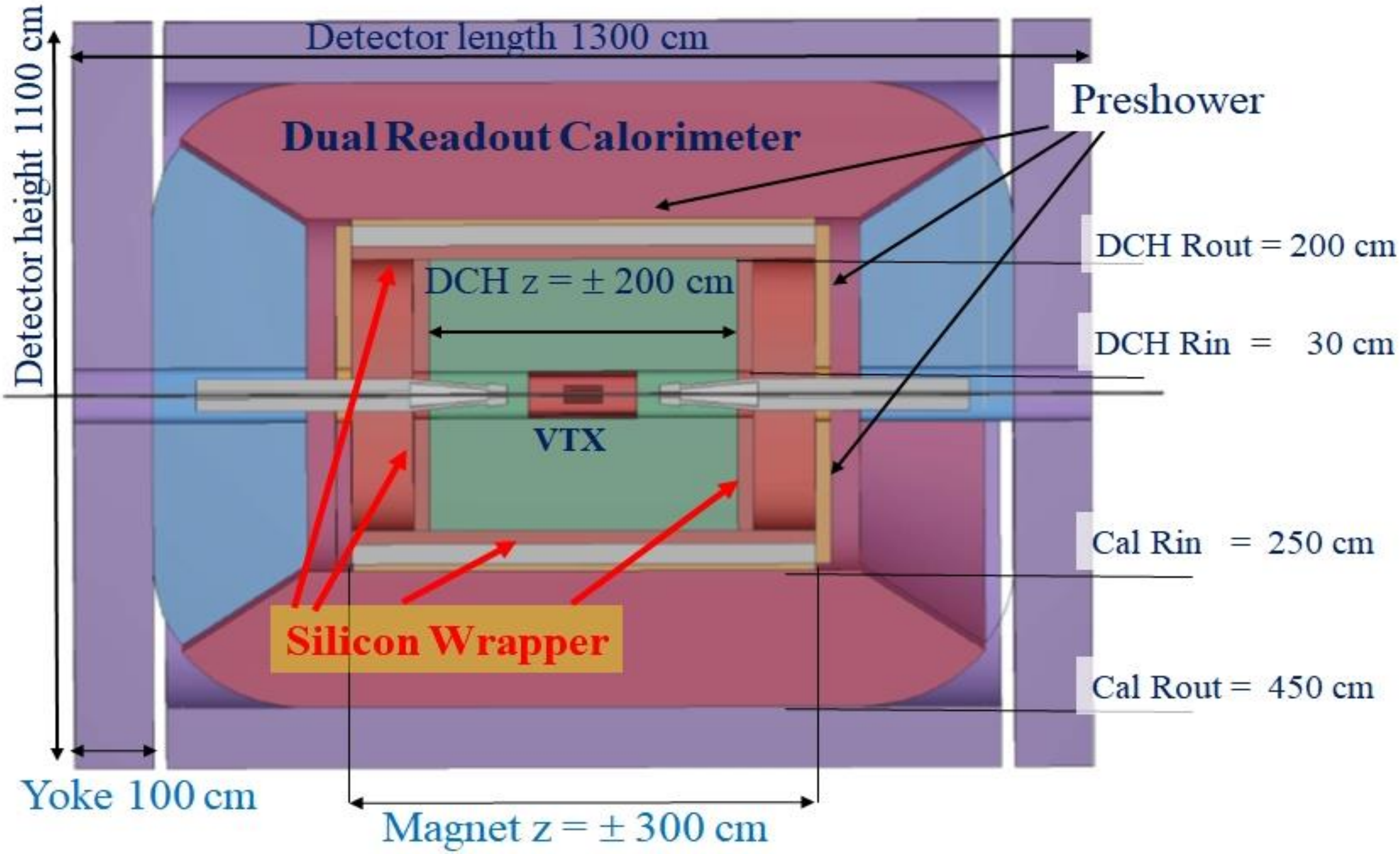
- Costs depends a lot on geometry and complexity.
  - Our last pseudo-quad from ATLASPIX1 costed 6k + IVA: smaller chip, but more complex layout, integrating also adapters to readout system
  - With symplifications available in ATLASPIX3 and splitting between hybrid and adapter expect to go down to 4k+IVA: **funding request of 5k**

Plans

- Silicon package till now mainly concentrate on application of CMOS technologies and developed without RD_FA funds
  - Small request this year to assess multi-chip performance of the detectors developed for ATLAS
- The technology if of great interest, in total INFN submitted 5 AIDA++ EoI on CMOS related technologies
- Three of them involve RD_FA members
  - Future requests probably based on the development of the IDEA detector concept and of the final AIDA++ project

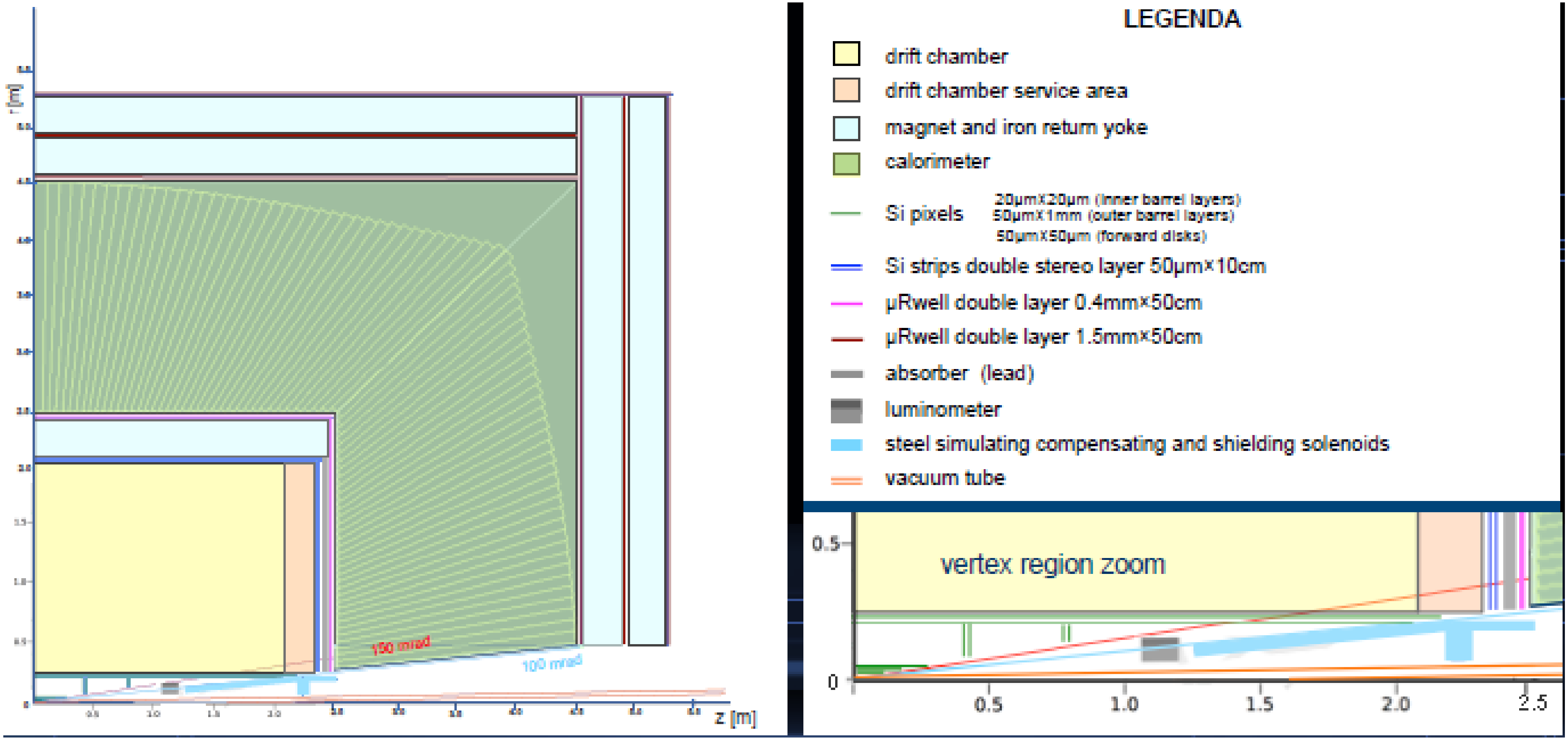
BACKUP

IDEA Layout



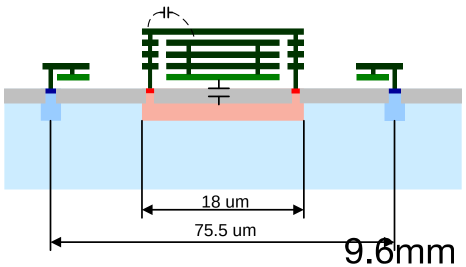
Detector length 1300 cm
Detector height 1100 cm
Preshower
Dual Readout Calorimeter
DCH Rout = 200 cm
DCH z = ± 200 cm
DCH Rin = 30 cm
VTX
Cal Rin = 250 cm
Silicon Wrapper
Cal Rout = 450 cm
Yoke 100 cm
Magnet z = ± 300 cm

IDEA Layout


r [m]
z [m]
150 mrad
100 mrad
LEGENDA
drift chamber
drift chamber service area
magnet and iron return yoke
calorimeter
Si pixels
20μmX20μm (inner barrel layers)
50μmX1mm (outer barrel layers)
50μmX50μm (forward disks)
Si strips double stereo layer 50μm×10cm
μRwell double layer 0.4mm×50cm
μRwell double layer 1.5mm×50cm
absorber (lead)
luminometer
steel simulating compensating and shielding solenoids
vacuum tube
vertex region zoom
0.5
0
0.5
1.0
1.5
2.0
2.5

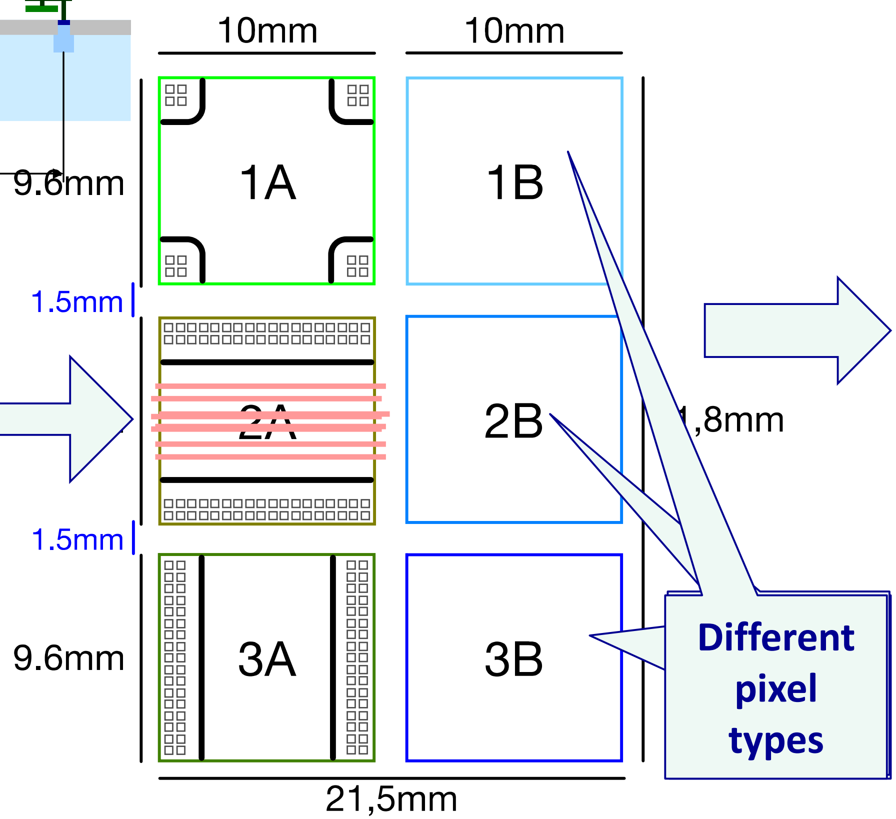
Passive CMOS

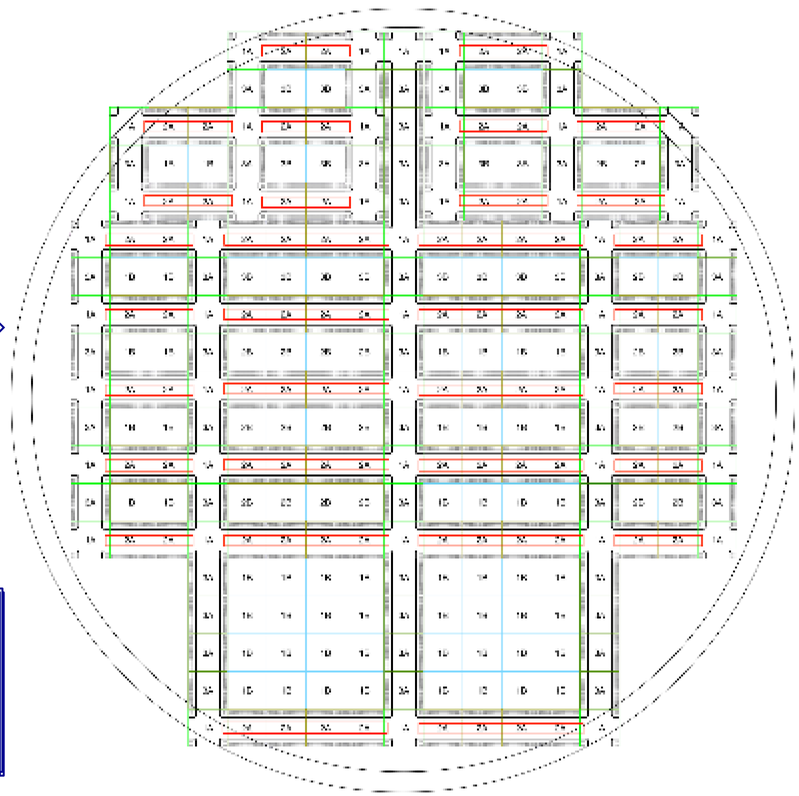
- Implement passive structures in standard CMOS processes on high resistivity substrate
  - Alternative fabrication process for standard strip and pixel sensors: **“fast and cheap”**
  - **Stitching** to build large area sensors: **submitted this week in Lfoundry 150 nm**



Strip layout

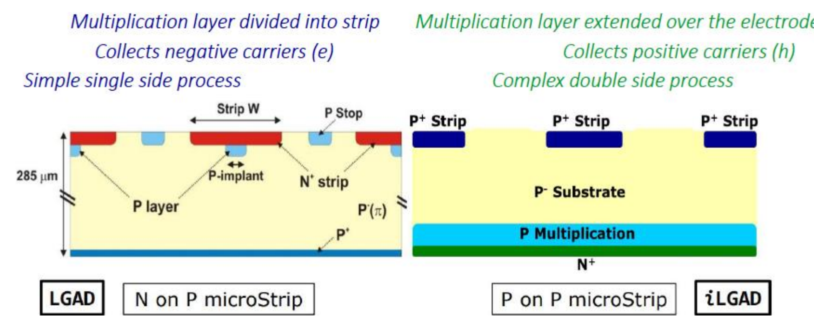
2 × 3 cm^2 reticle





Can one use passive CMOS Strips?

- The Outer Silicon Layer as an area of 100 m^2: use of pixels is impractical
- Hamamatsu is the only supplier for the ATLAS and CMS strip trackers:
  - Both O(100 m^2) size
- CMOS detector production consideration are valid for strips too:
  - Fast (foundries capabilities 10000 wafer/month)
    8" wafers ~100 cm^2 (considering yield):
    100 m^2 detector is 10000 wafers
  - Cheap (~1000 Eur/wafer)
  - Stitching yield and cost?

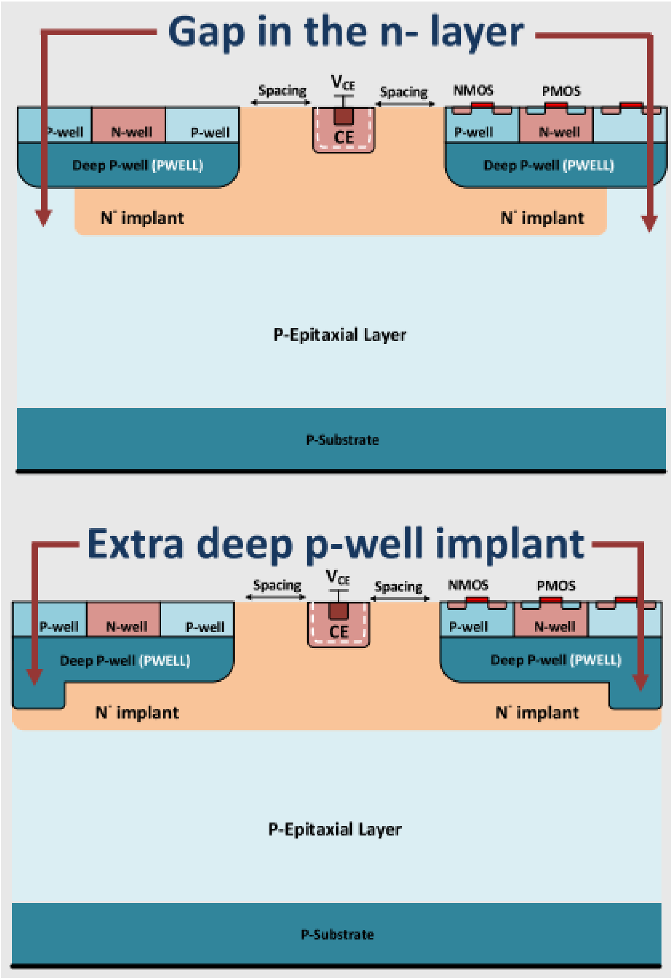


https://indico.cern.ch/event/666427/contributions/2881813/attachments/1603622/2544525/20180219_iLGAD_IvanVila.pdf

- A dream: can we implement charge multiplication in CMOS sensors:
  - Mechanism similar to LGAD
  - Reduce timing requirement of the rest of central tracking
    Slower detector → Less power → Less material (?)
  - ToF Detector:
    Assuming 30 ps time resolution and 2 m tracking volume, 3σ π/K separation till 3 GeV/c

TowerJazz: MALTA-MONOPIX

- **TowerJazz 180 nm** CMOS CIS
  - Deep Pwell allows full CMOS in pixel
  - Derived from ALICE development (CERN)
  - Epitaxial-layer thickness: 18 – 40 μm
  - High resistivity: 1 – 8 kΩ·cm
  - Modified process to improve lateral depletion
- **MALTA** (asynchronous) and **TJ-Monopix** (column drain) implementing **small fill factor** designs
  - 36 × 40 μm^2 pixel size
  - Very low noise (10-15 e^-) and threshold dispersion (30-40 e^-)
  - Pixel design submitted in 2017 had charge losses due to low field region at pixel corners
- New cell design submitted in 2018, being tested now on small size prototype
- **Large scale arrays probably submitted end of 2019**



Offerta per ATLASPIX1

Prime S.r.l. Unipersonale – Assemblaggi elettronici – Prime Elettronica

Offerta

Revisione offerta n°1 del 20/02/2019

Richiesta di Offerta N°	Numero	Data
CIG : Z4826F106A	A 000027	20/02/2019

Spett.le
I.N.F.N. Sez. di Milano
Via Celoria, 16
20133 Milano MI Italia

Pagina 1 — Alla Cortese attenzione di

Codice Fiscale: 84001850589

Pagamento: Bonifico Bancario 30 GG DF

Banca: BANCA INTESA SANPAOLO SPA
IBAN: IT 11 N 03069 60816 100000030115
BIC: BCITITMM

Codice	Descrizione	U.M.	Q.tà	Prezzo Un.	Sconto %	Importo	C.IVA
	CIG: Z4826F106A						
	Assemblaggio completo SMT della Vostra scheda mod. "AMS Active Flex 3.1" completo di ispezione ottica, gestione di tutta la componentistica elettronica da parte nostra compreso il FLEX PCB multistrato	NR	5	685,00		3.425,00	22SP
	Fornitura pcb flex NON assemblati	NR	5	360,00		1.800,00	22SP
00010CM100FIC	Spese da affrontare al primo assemblaggio: Contributo spese per esec.attrez.lamina deposito pasta saldante lato top	NR	1	155,00		155,00	22SP
	Contributo spese esecuzione attrezzature complete PCB FLEX	NR	1	590,00		590,00	22SP
PROGRAMMA	Contributo spese per esecuzione programm a macchina e set-up P&P	NR	1	190,00		190,00	22SP

Il Nostro Valore Aggiunto:
- Serigrafia a centraggio ottico, completa di ispezione ottica automatica post serigrafia SPI (Solder Paste Inspection)
- Saldatura con tecnologia a rifusione 9+0 zone e/o dove necessario anche in Vapor phase. (Possibilità di profilare e certificare ogni produzione)
- Ispezione X-RAY ove necessaria con la possibilità di ricevere un report completo di immagini
- Gestione dei componenti sensibili all'umidità secondo lo standard J-STD 033, anche a mezzo di armadi ad umidità controllata.
- Produzione secondo lo standard di qualità ISO 9001:2015 e operatori certificati IPC-A610 CIS

Note / Vettore / Totale Articoli / % Sconto / Importo Sconto / Acconto / Spese Trasporto / Spese Bancarie / Spese Varie / Spese Bolli / Causale Trasporto / Modalità di consegna / Cod. IVA / Imponibile / Aliquota / Imposta / Totale Imponibile / Data richiesta consegna / Totale IVA / Totale Documento

Nell'attesa di un vostro cortese riscontro, vogliate nel frattempo gradire

Distinti Saluti
PRIME SRL

Ufficio Commerciale
Verifica e approvazione

Prime S.r.l. Unipersonale – Assemblaggi elettronici – Prime Elettronica

Offerta

Revisione offerta n°1 del 20/02/2019

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CIG : Z4826F106A	A 000027	20/02/2019

Spett.le
I.N.F.N. Sez. di Milano
Via Celoria, 16
20133 Milano MI Italia

Pagina 2 — Alla Cortese attenzione di

Codice Fiscale: 84001850589

Pagamento: Bonifico Bancario 30 GG DF

Banca: BANCA INTESA SANPAOLO SPA
IBAN: IT 11 N 03069 60816 100000030115
BIC: BCITITMM

Codice	Descrizione	U.M.	Q.tà	Prezzo Un.	Sconto %	Importo	C.IVA
	Termine di consegna: 6/7 settimane da ricevimento ordine ed eventuale Vs materiale Validità offerta: 60 gg						

Note: CIG: Z4826F106A AMS Active Flex 3.1

Vettore: EXECUTIVE 6316, VIA LAGO DI MOLVENA 35, 36015 SCHIO VI

Totale Articoli: 6.160,00

Causale Trasporto: Vendita — Modalità di consegna: FRANCO

Cod. IVA	Imponibile	Aliquota	Imposta
22SP	6.160,00	22 %	1.355,20

Totale Imponibile: 6.160,00
Totale IVA: 1.355,20
Totale Documento: EUR 7.515,20

Nell'attesa di un vostro cortese riscontro, vogliate nel frattempo gradire

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