Firmware at the Mu2e Test Stand

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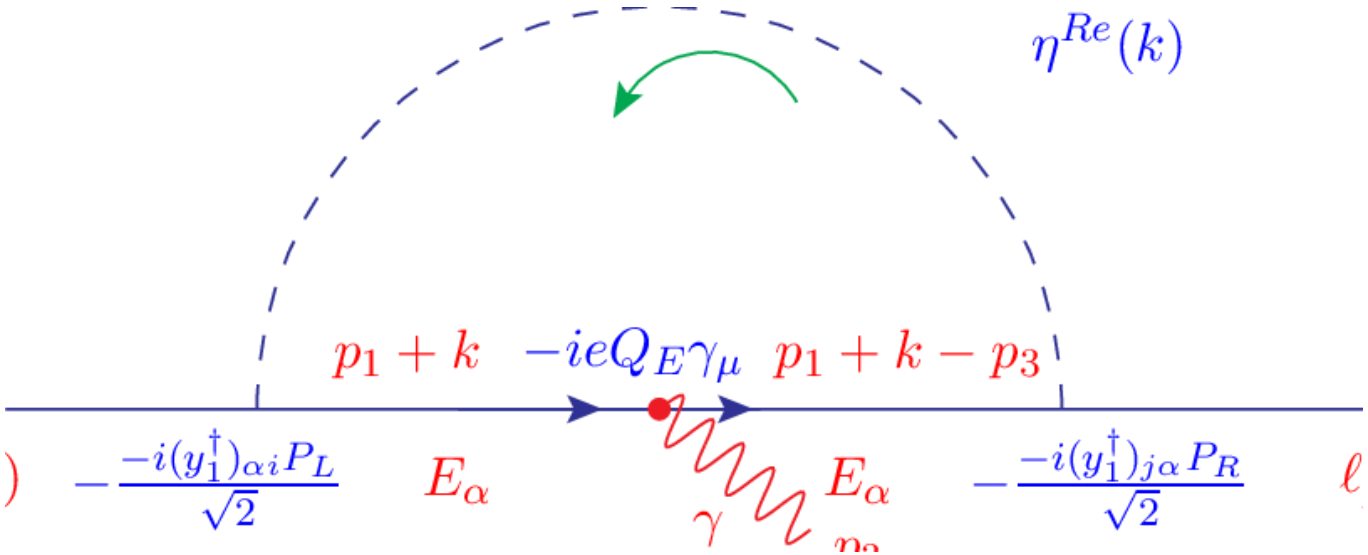
Final Report

25/09/2019

Mu2e Experiment

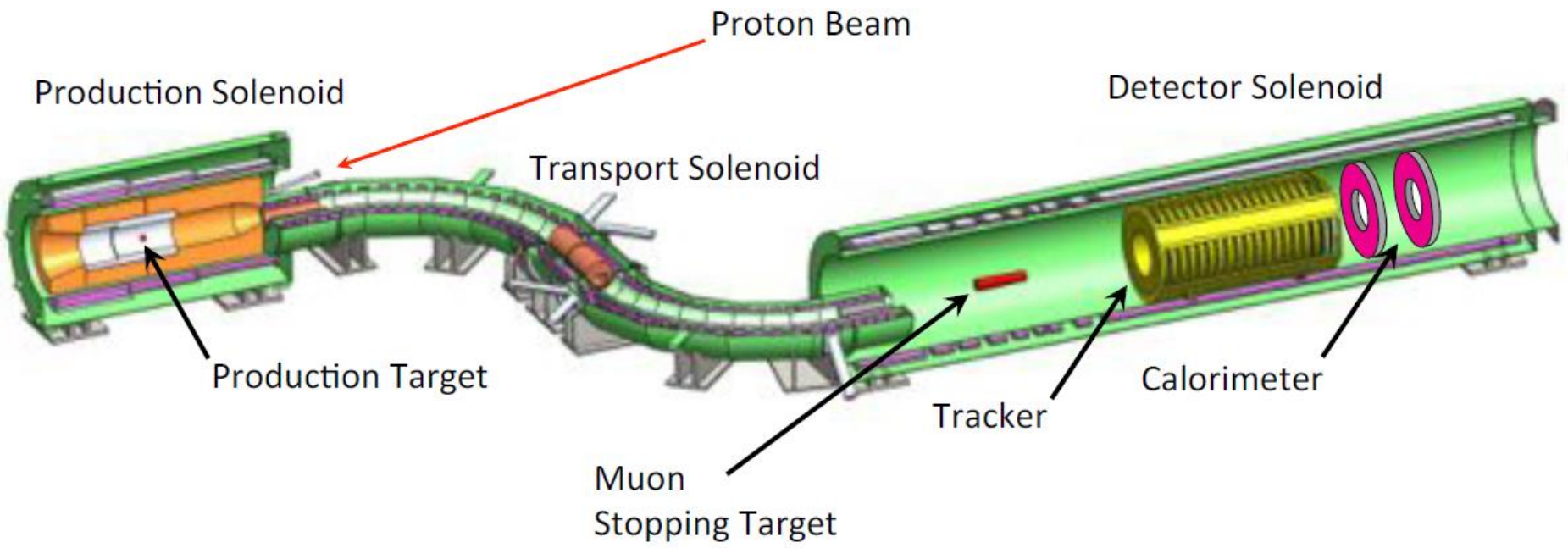
A search for Charged-Lepton Flavor Violation



neutrino-less coherent conversion of the muon in electron

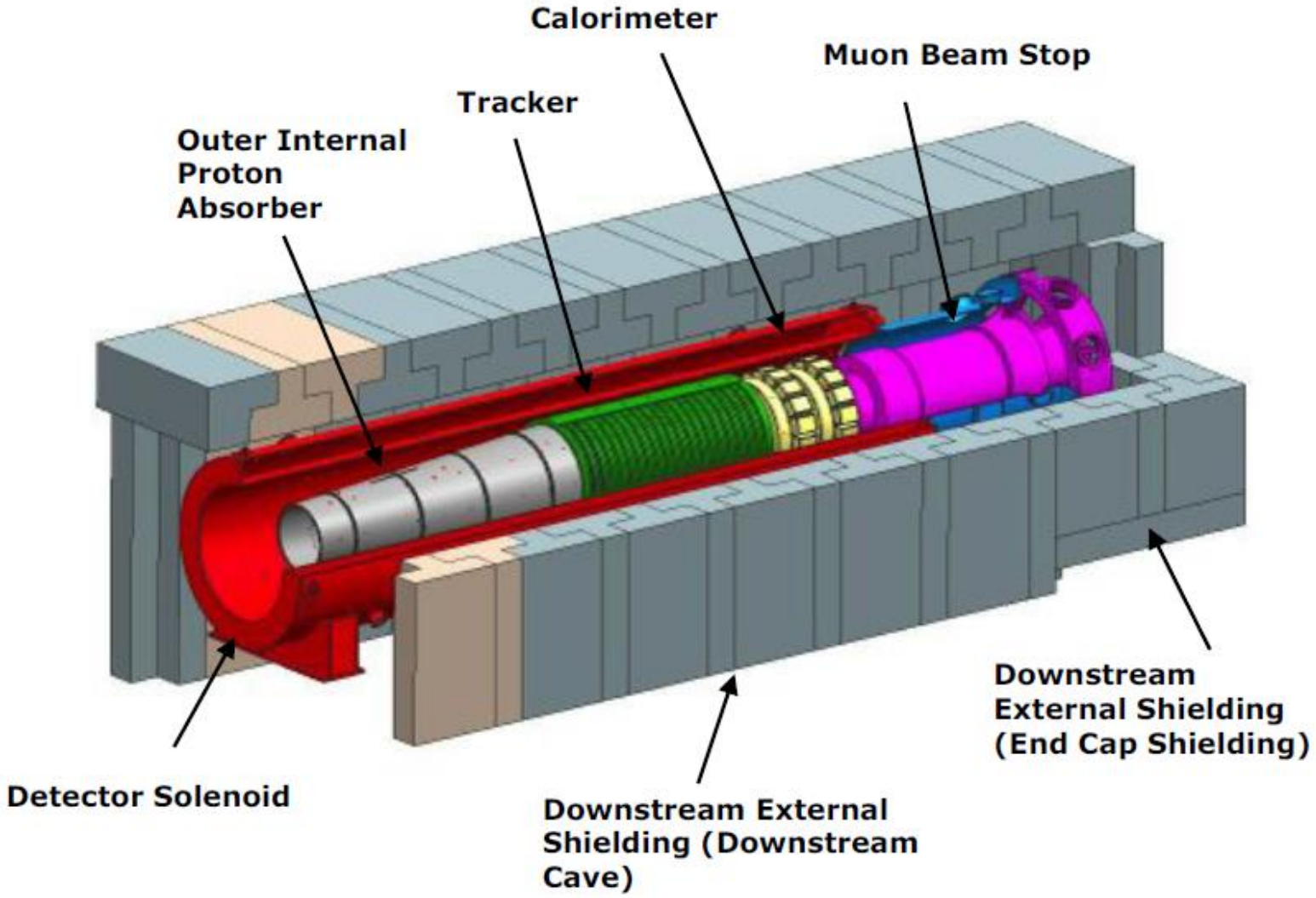
The observation of this physics process would demonstrate the existence of physics beyond the standard model

Mu2e Concept



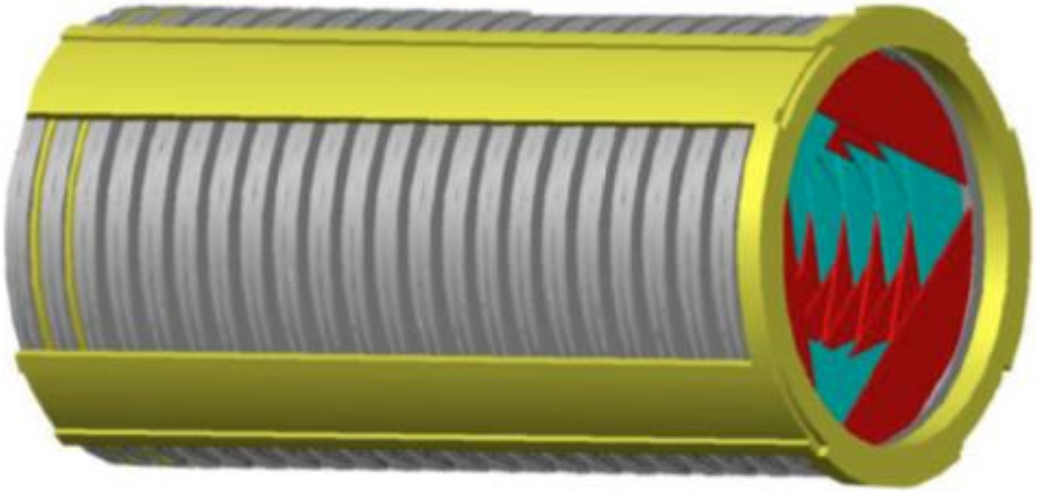
- Generate a beam of low momentum muons (μ^-)
- Stop the muon in a target (aluminum)
- The stopped muons are trapped in orbit around the nucleus
- Look for events consistent with $\mu N \rightarrow eN$

The Mu2e Detector



Tracker

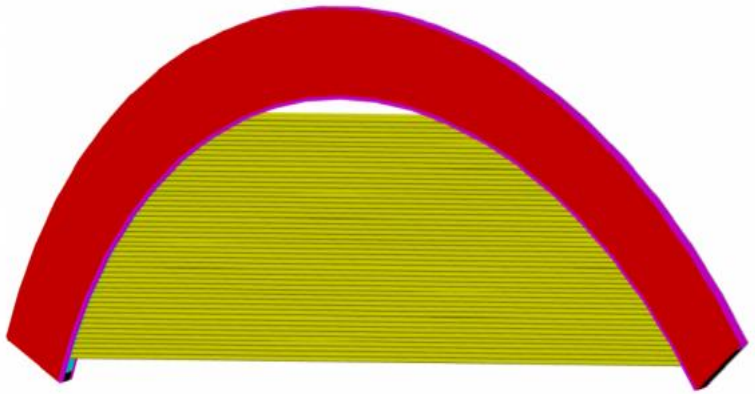
Identify and measure 105 MeV/c electrons

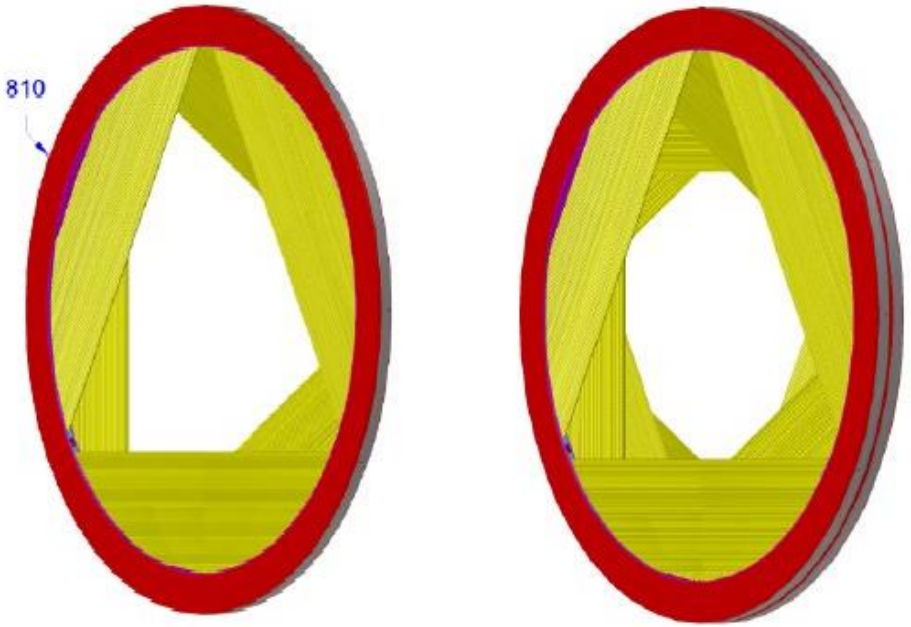


18 stations are assembled into the completed tracker

A station is 1 plane of 6 panels

A panel is a group of 96 straws





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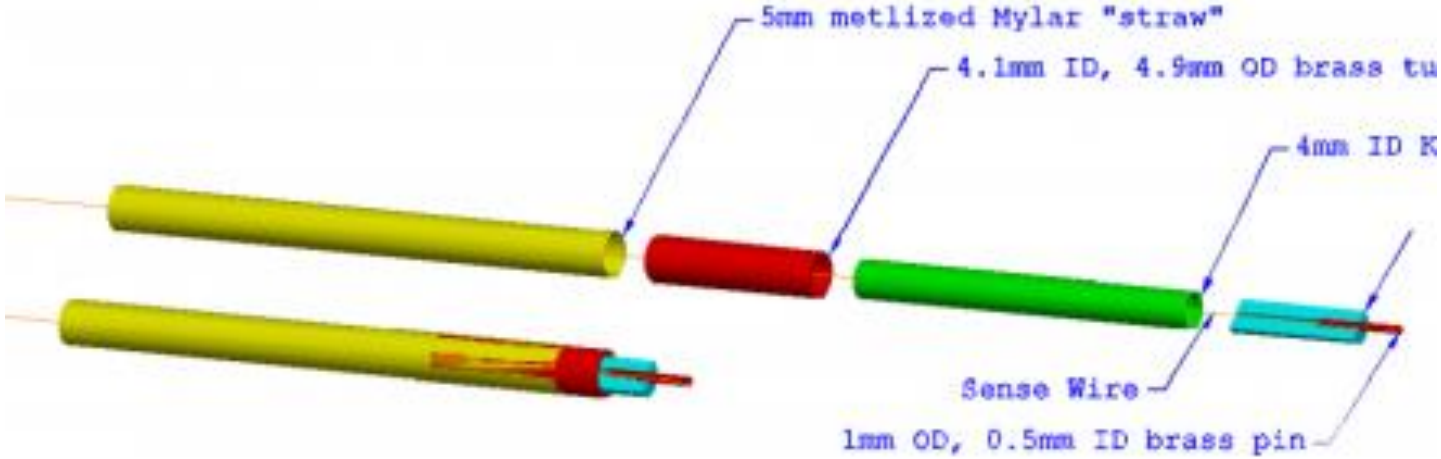
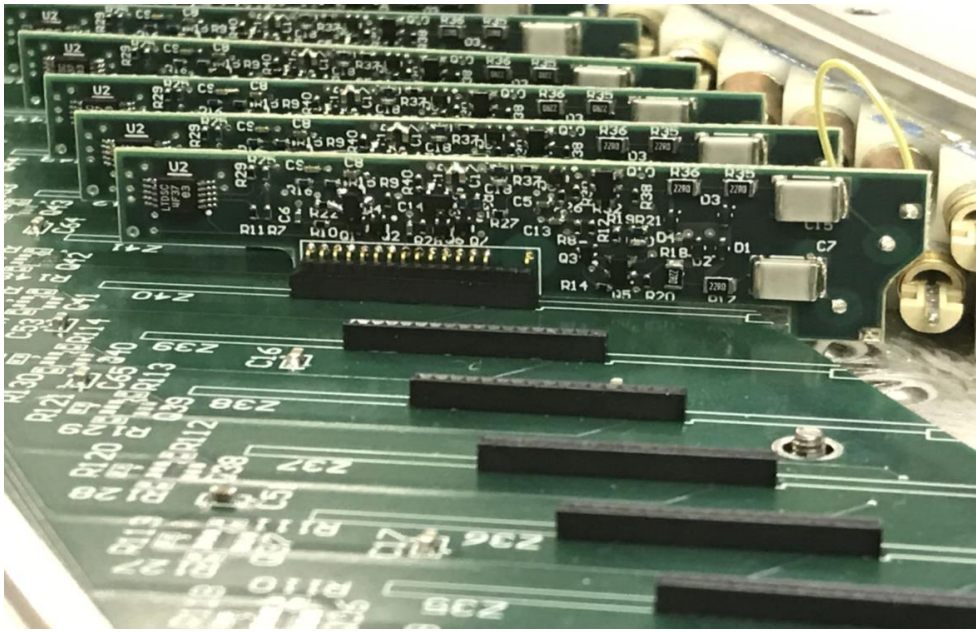


The detector has 23,000 straws distributed into 20 measurement stations across a 3 m length.

Each straw is instrumented on both sides with preamps and TDCs.

Signal from the straws need to be amplified, digitized and trasmitted to the DAQ.



DRAC

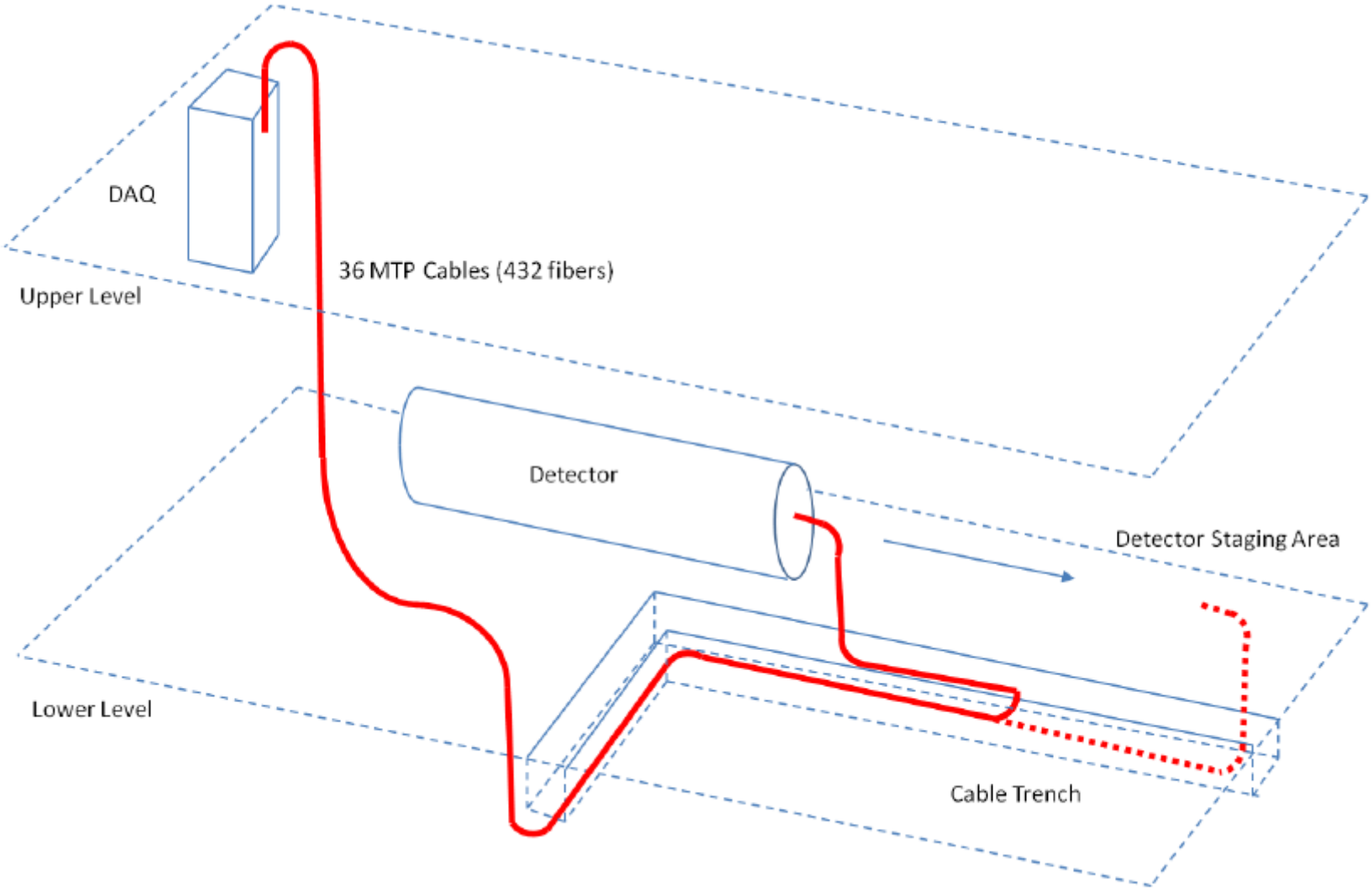
Mu2e tracker digitizer and readout controller board

It sits on the outer edge of each Mu2e tracker panel and services the entire panel via 12-bit 50 Mbps ADCs (MAX19527) digitizing the hit energy from each of the 96 straws.

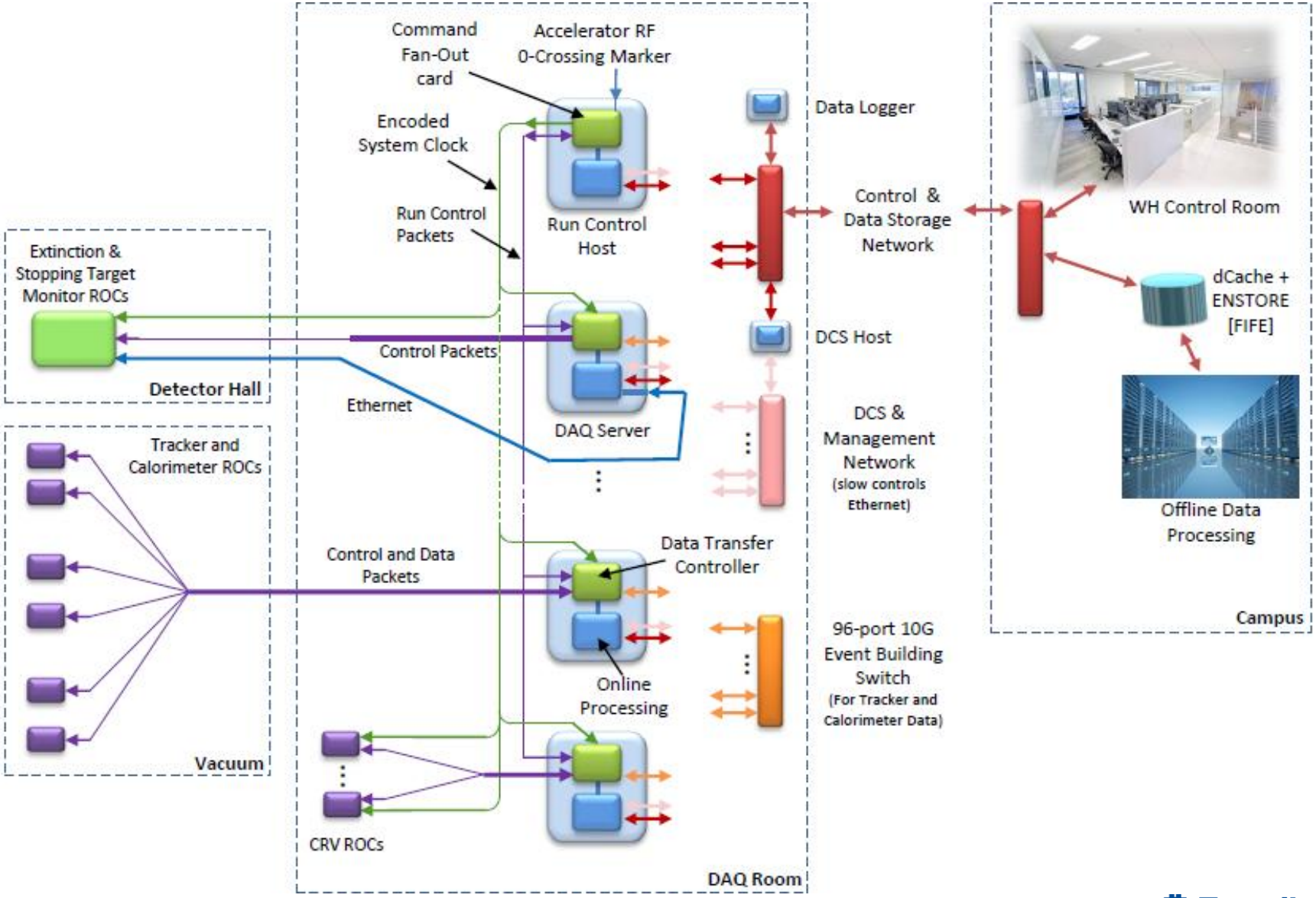
The time of the hits from the two ends of the straws is digitized inside two Microsemi PolarFire FPGAs (MPF300TS-1FG1152), called DIGI HV and DIGI CAL.

A third Microsemi PolarFire FPGA, called ROC, is connected to each DIGI via four 5 Gbps SERDES lanes and to the TDAQ via a two 2.5 Gpbs fibers connected to a Data Transfer Controller.

Optical Fibers



TDAQ - Mu2e Trigger and Data Acquisition



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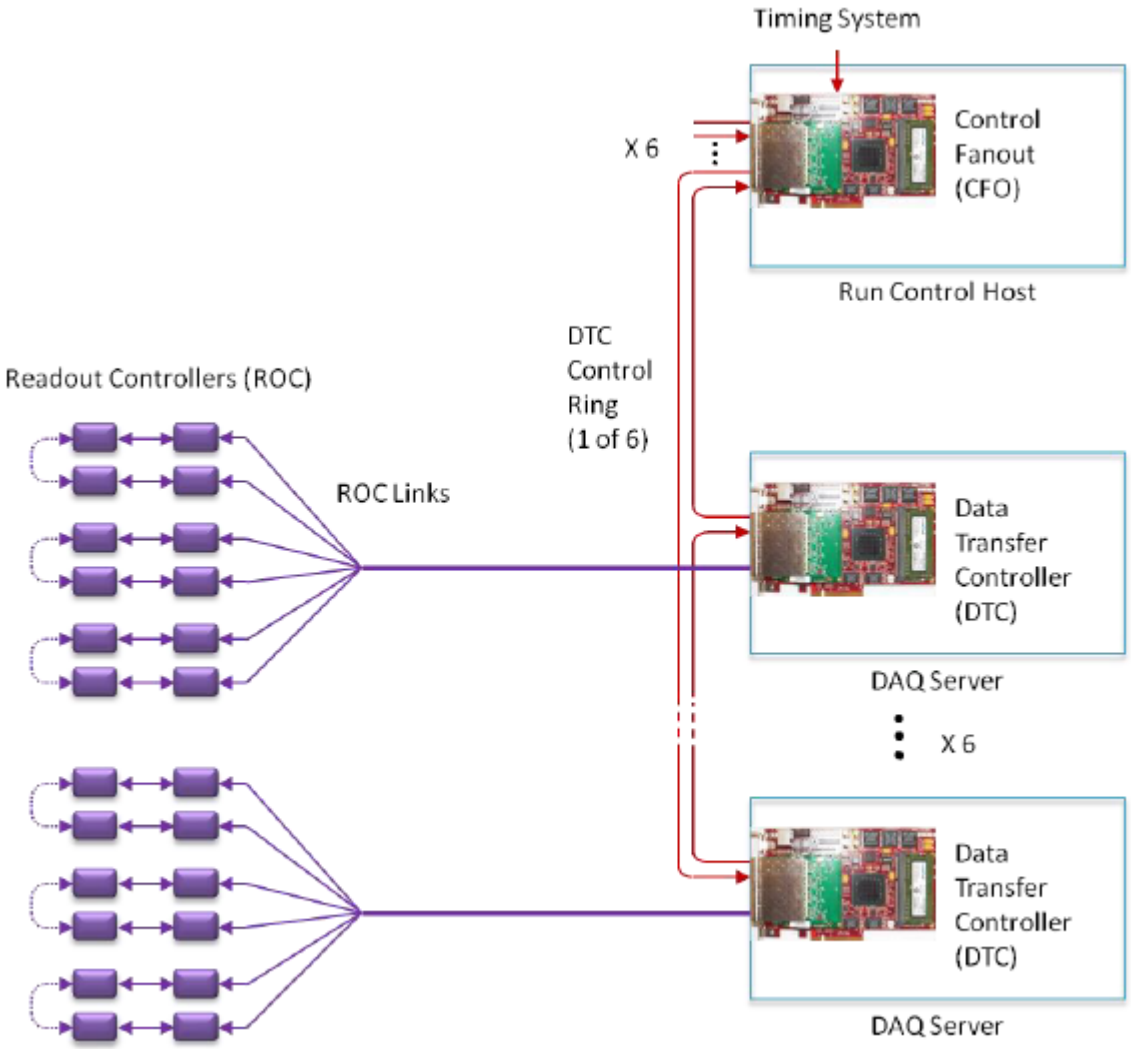
TDAQ - DTC



The Data Transfer Controller (DTC) collects data from multiple detector Readout Controllers.

The DTC is implemented using a commercial PCIe card located in the DAQ Server.

There are a total of 36 DAQ servers, occupying four racks in the electronics room.

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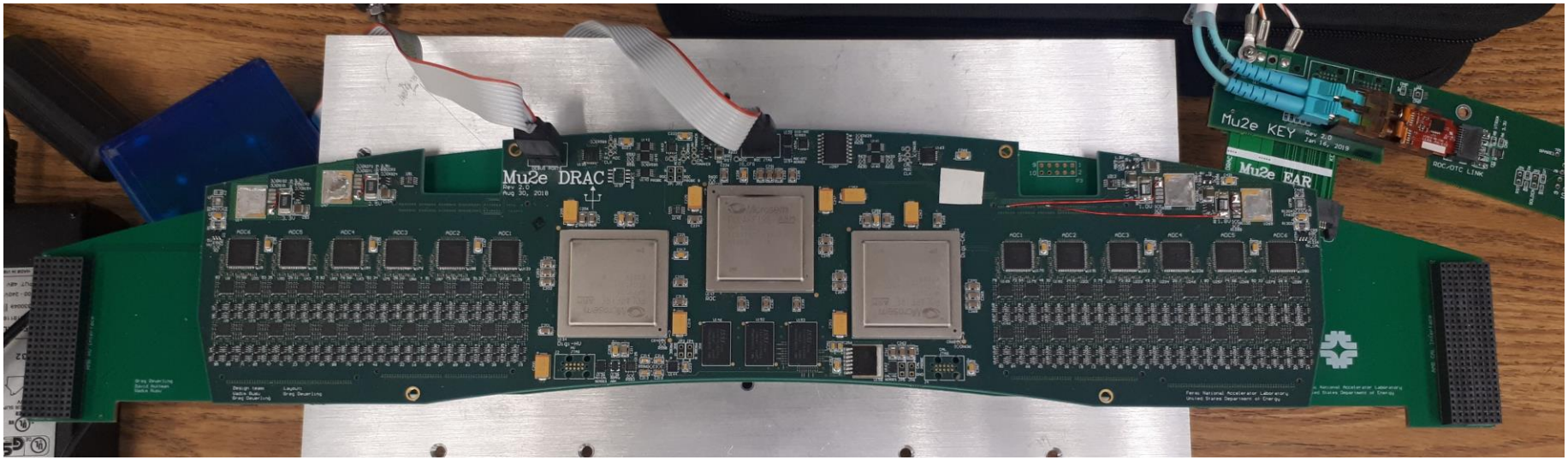
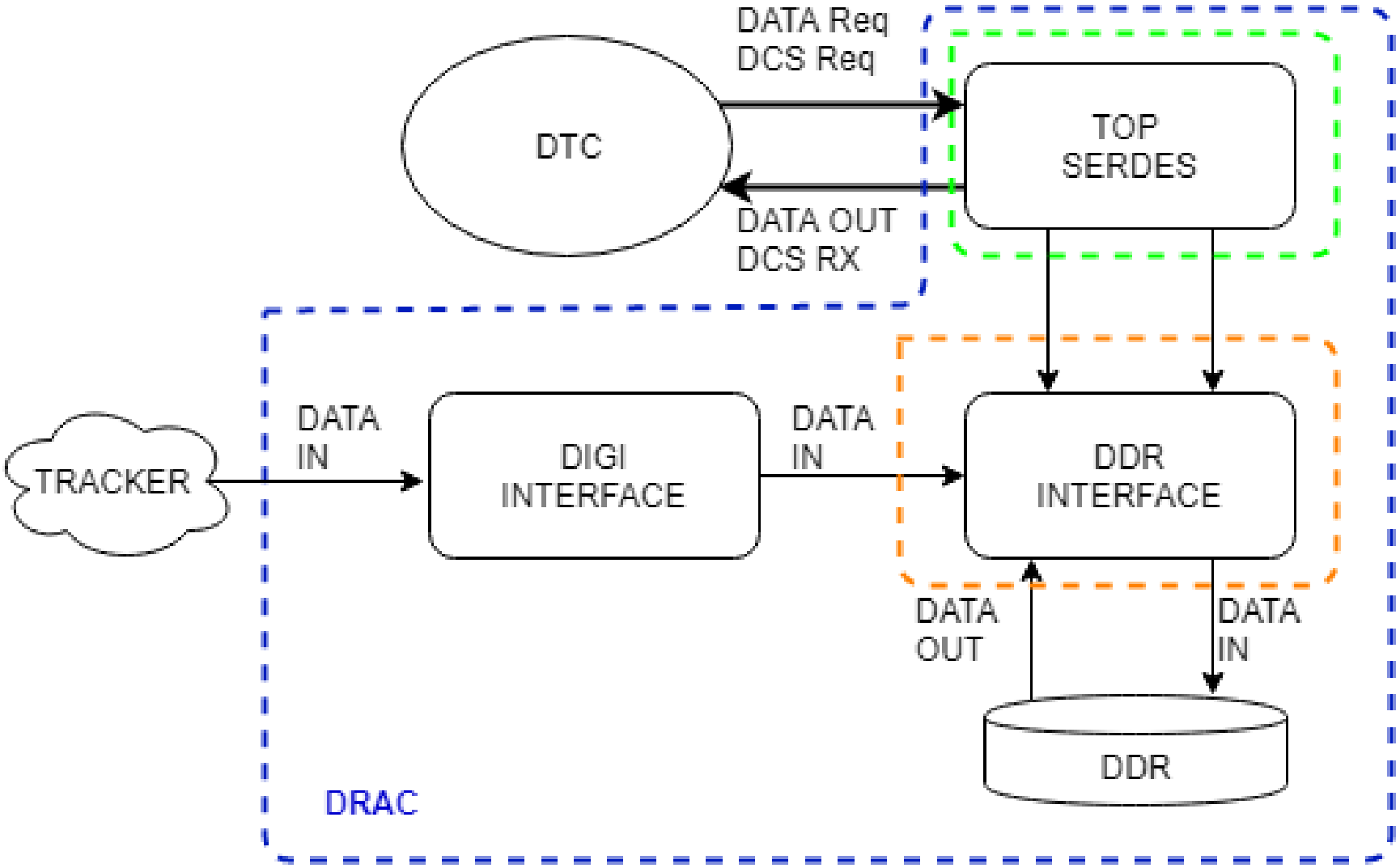
TDAQ - Run Control Host

The Command Fanout (CFO) module in the Run Control Host is responsible for generating and synchronizing packets by sending Heartbeat control packet for each event window.

ROCs – Readout Controllers



Firmware concept on DRAC



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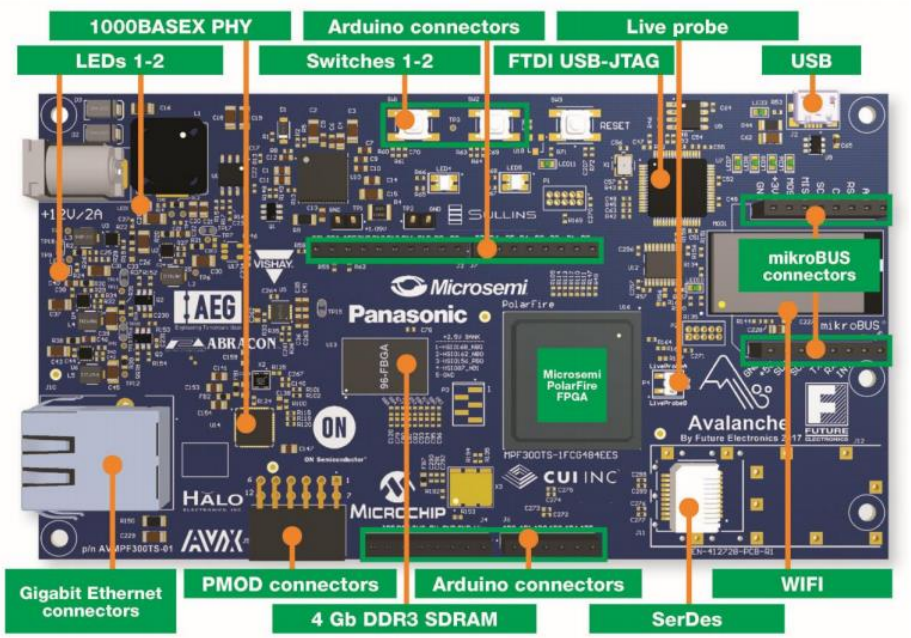

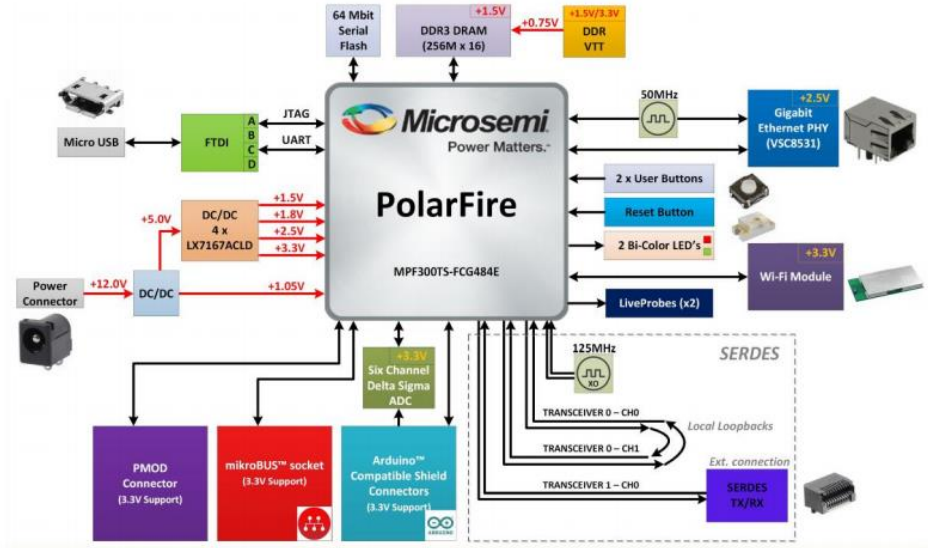

TOP SERDES

The main purpose of the firmware developed on the evaluation board is to manage communication between the Trigger and Data Acquisition (TDAQ) and the Mu2e detector subsystem Readout Controllers (ROCs).

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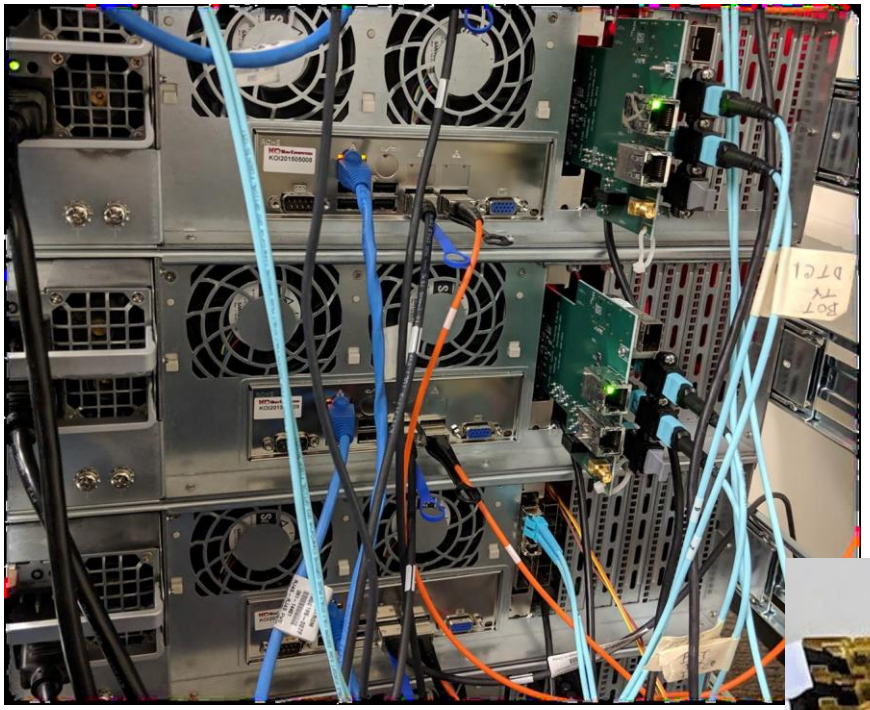
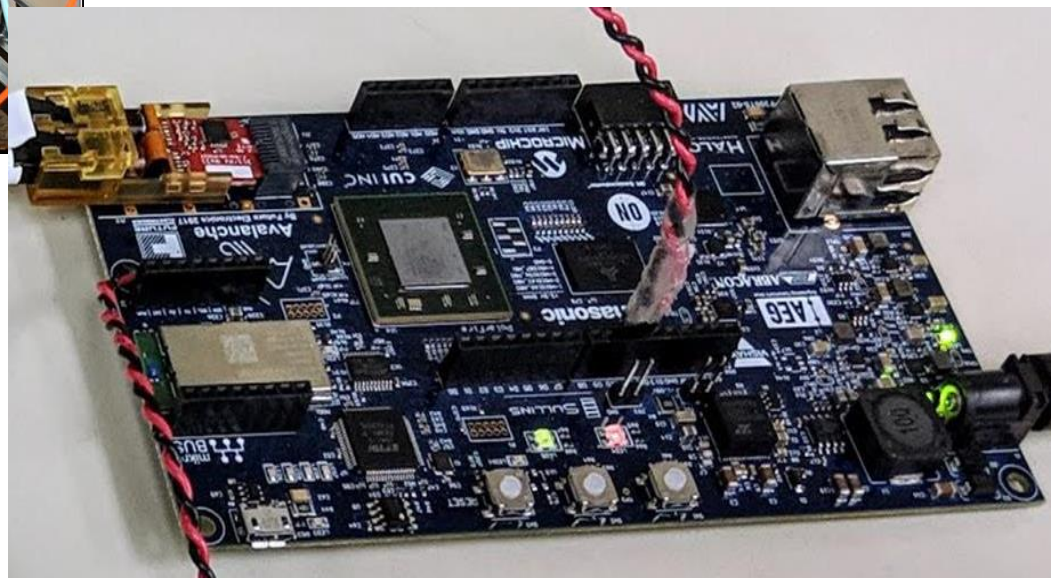
Testing link between ROC and DTC



Data Transfer Controller

Optical Fiber

Evaluation board with TOP SERDES



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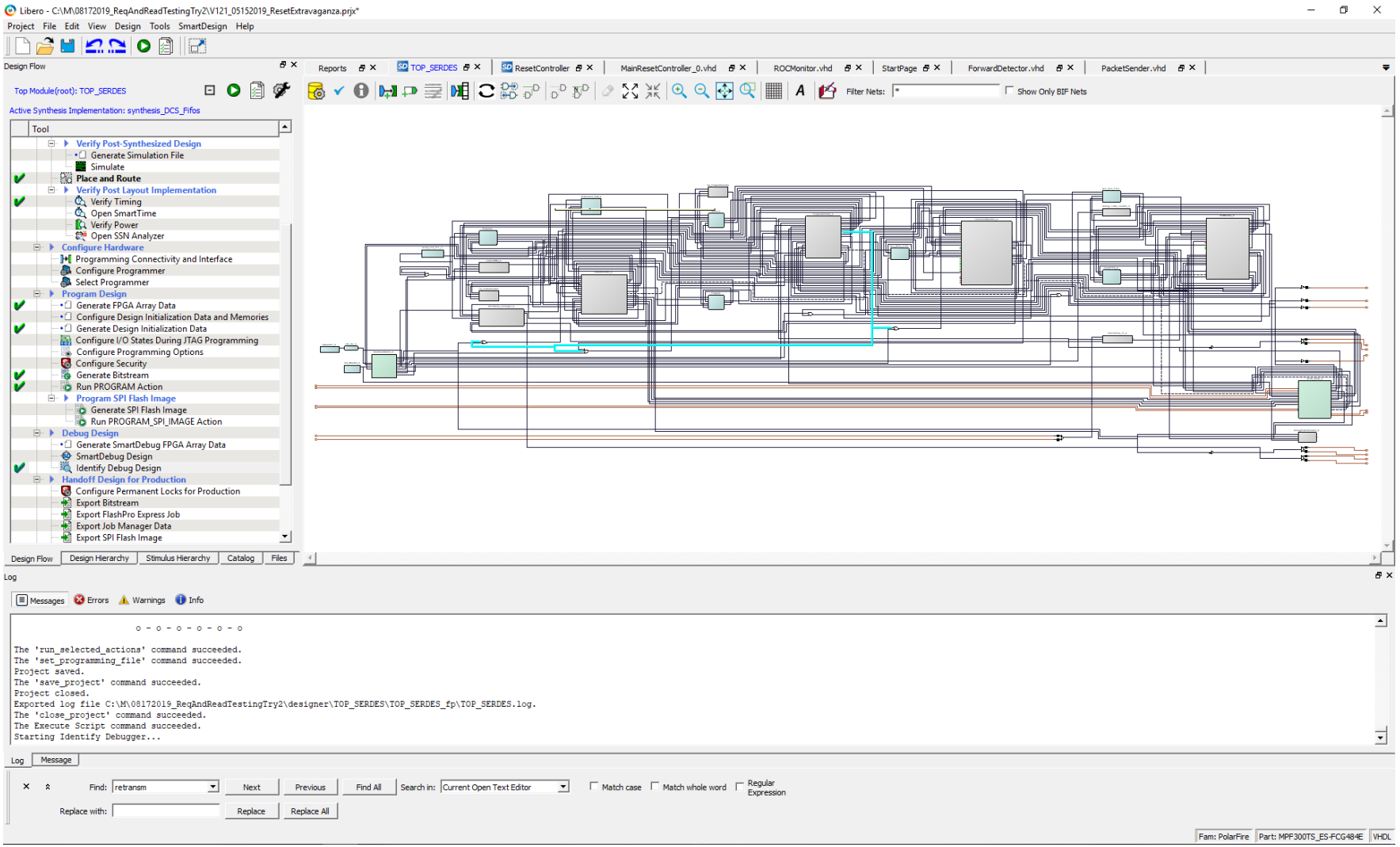
Libero SoC



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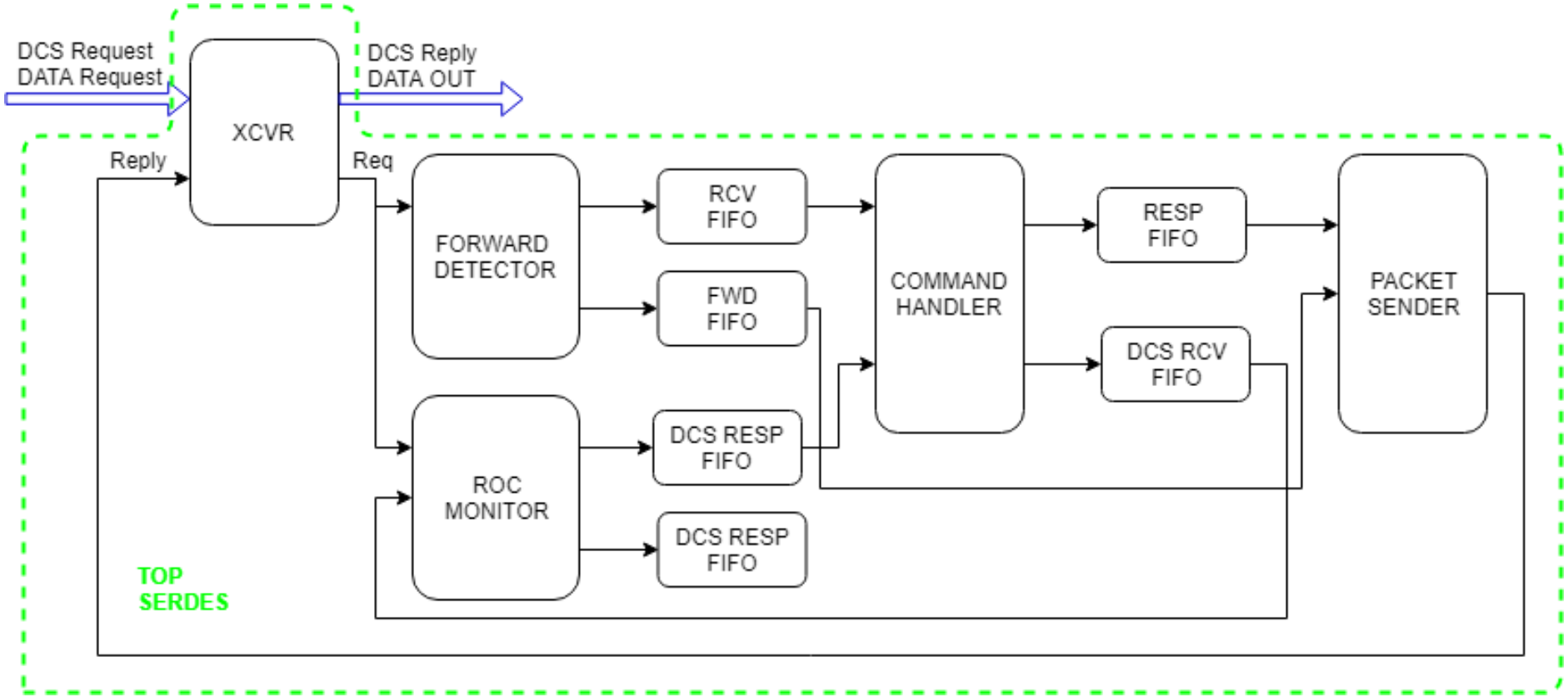
TOP SERDES


DCS Request
DATA Request
XCVR
DCS Reply
DATA OUT
Reply
Req
FORWARD
DETECTOR
RCV
FIFO
FWD
FIFO
COMMAND
HANDLER
RESP
FIFO
DCS RCV
FIFO
PACKET
SENDER
ROC
MONITOR
DCS RESP
FIFO
DCS RESP
FIFO
TOP
SERDES

otsDAQ - off-the-shelf data acquisition

otsdaq is an online DAQ software framework.

It is a web interface to configure, control, and monitor the online DAQ software entities from Chrome.

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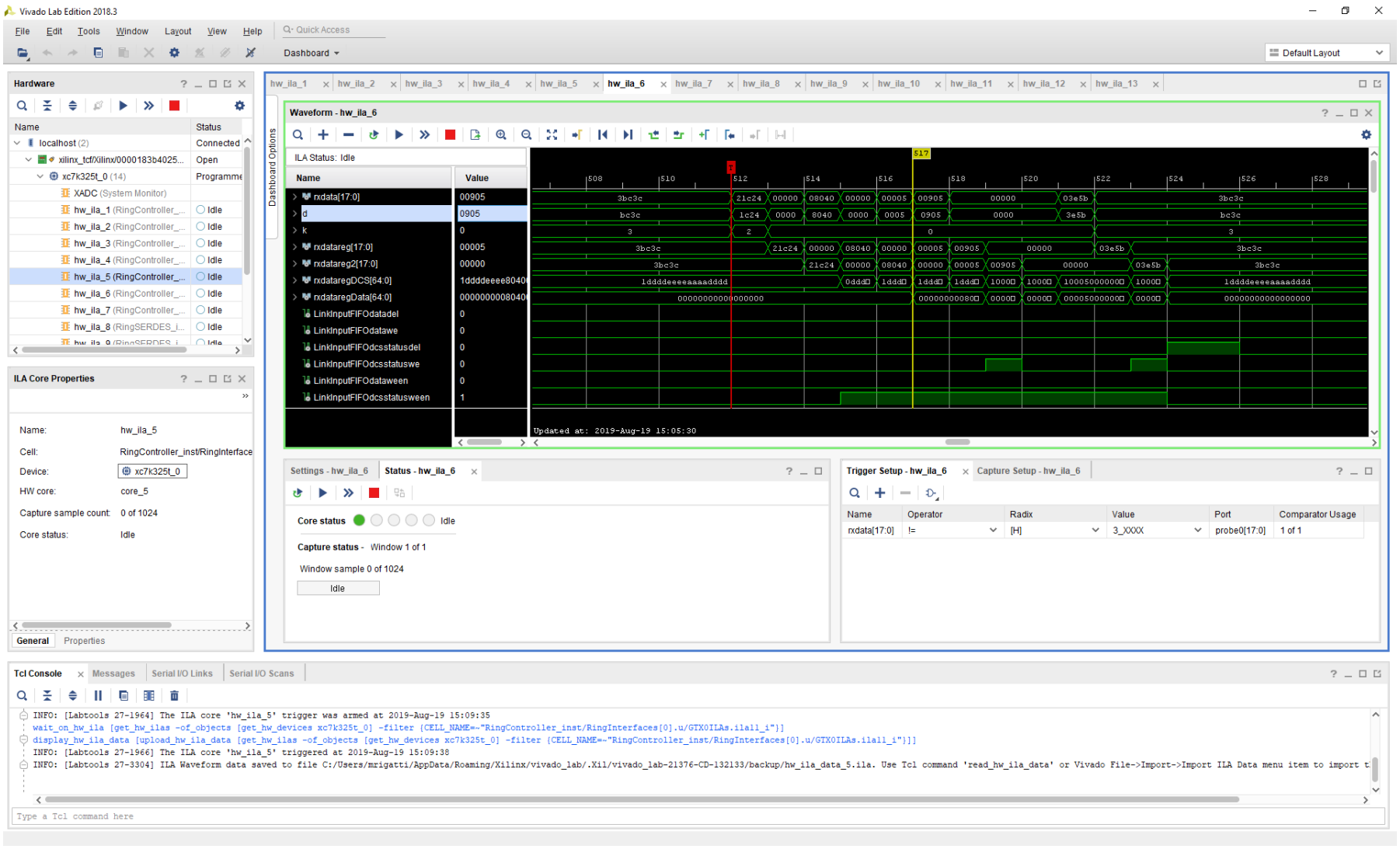
Vivado – signals from DTC



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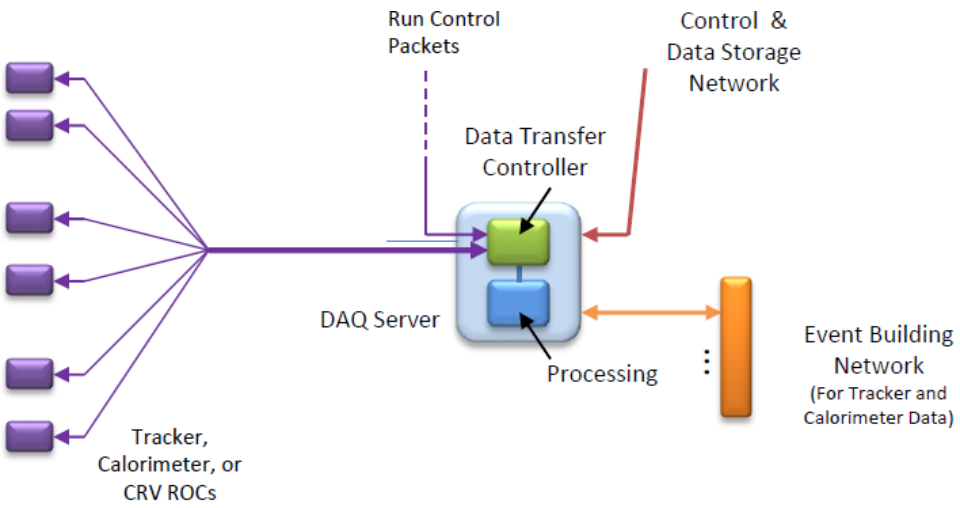
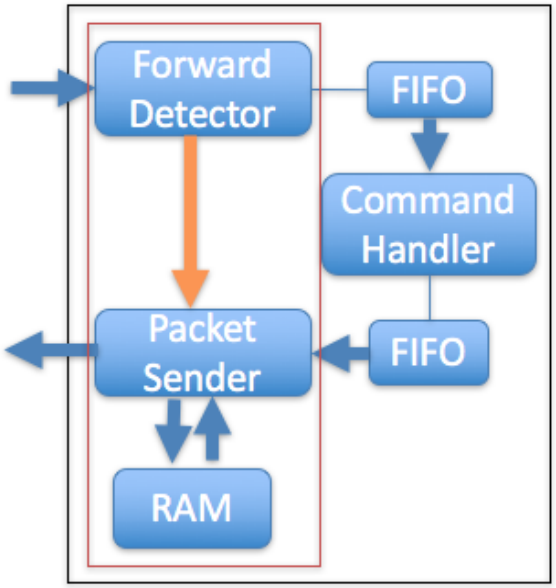
What so far?

PROBLEMS SOLVED:

- Bad synchronization on latches
- RESET bug
- Wrong calculation on the CRC
- Bad handling of the RESET on the retransmission

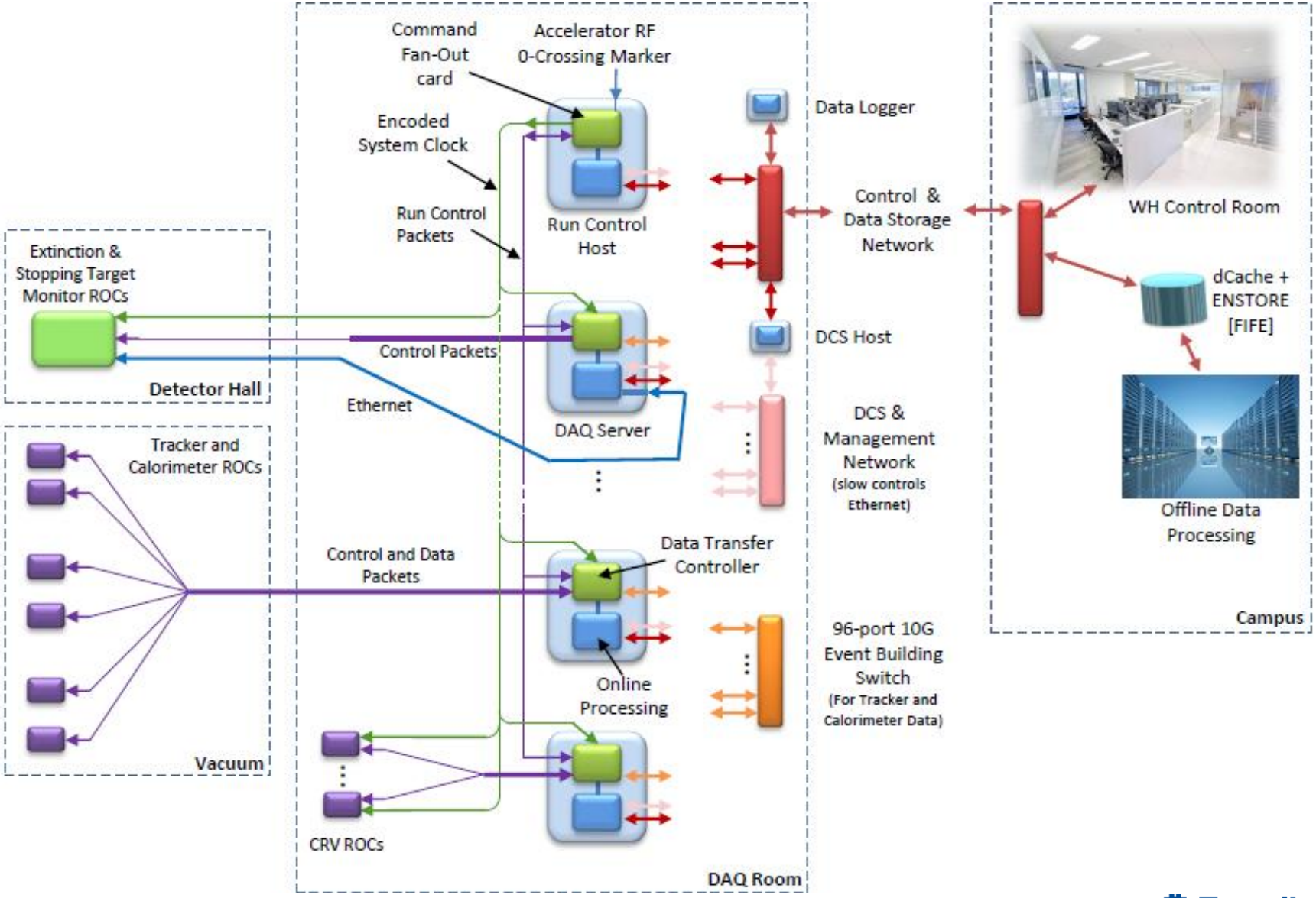




TASK ACCOMPLISHED:

- Debugging, testing and fixing retransmission of corrupted data
- Changed marker detection
- Testing of Read, Block Read, Write, Block Write Request
- Testing of Heartbeat and Data Request
- Stress Test

What now…?



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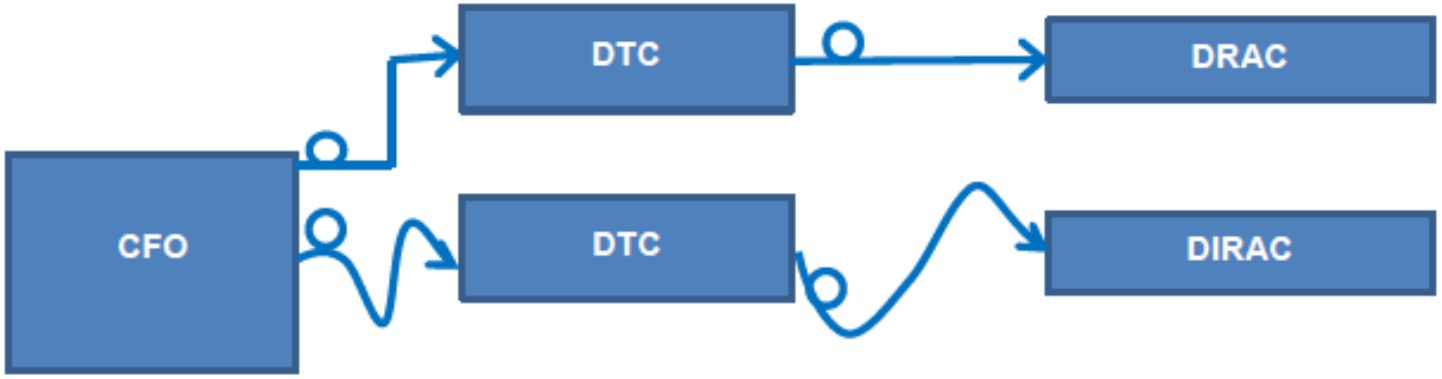
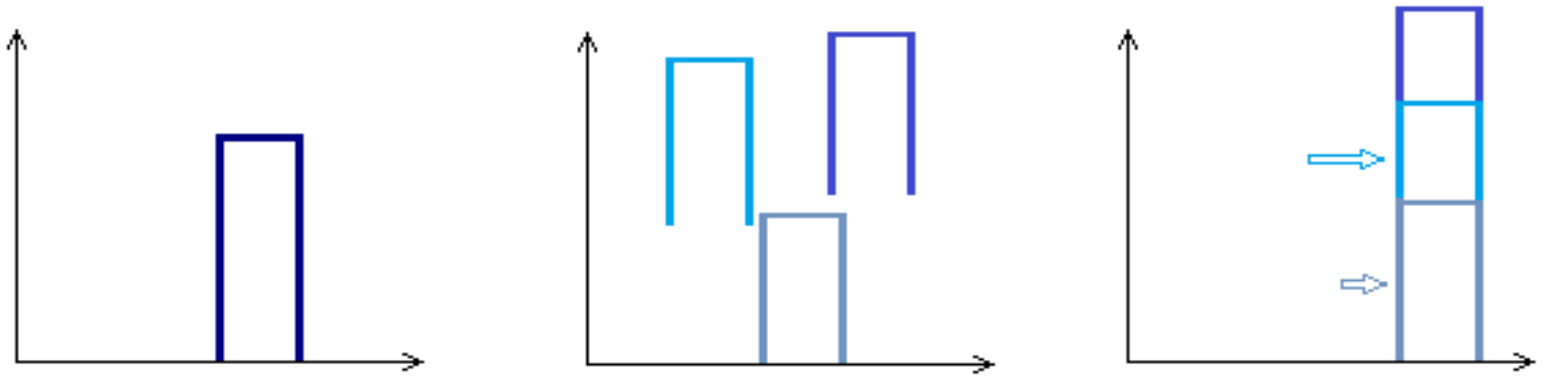
Pictorially: Event Window synchronization



Event Window defined at CFO

Step 1. Measure travel time through different boards and through fibers of different lengths

Step 2: after delays applied at ROC: Event Windows synchronized at timestamping front-ends



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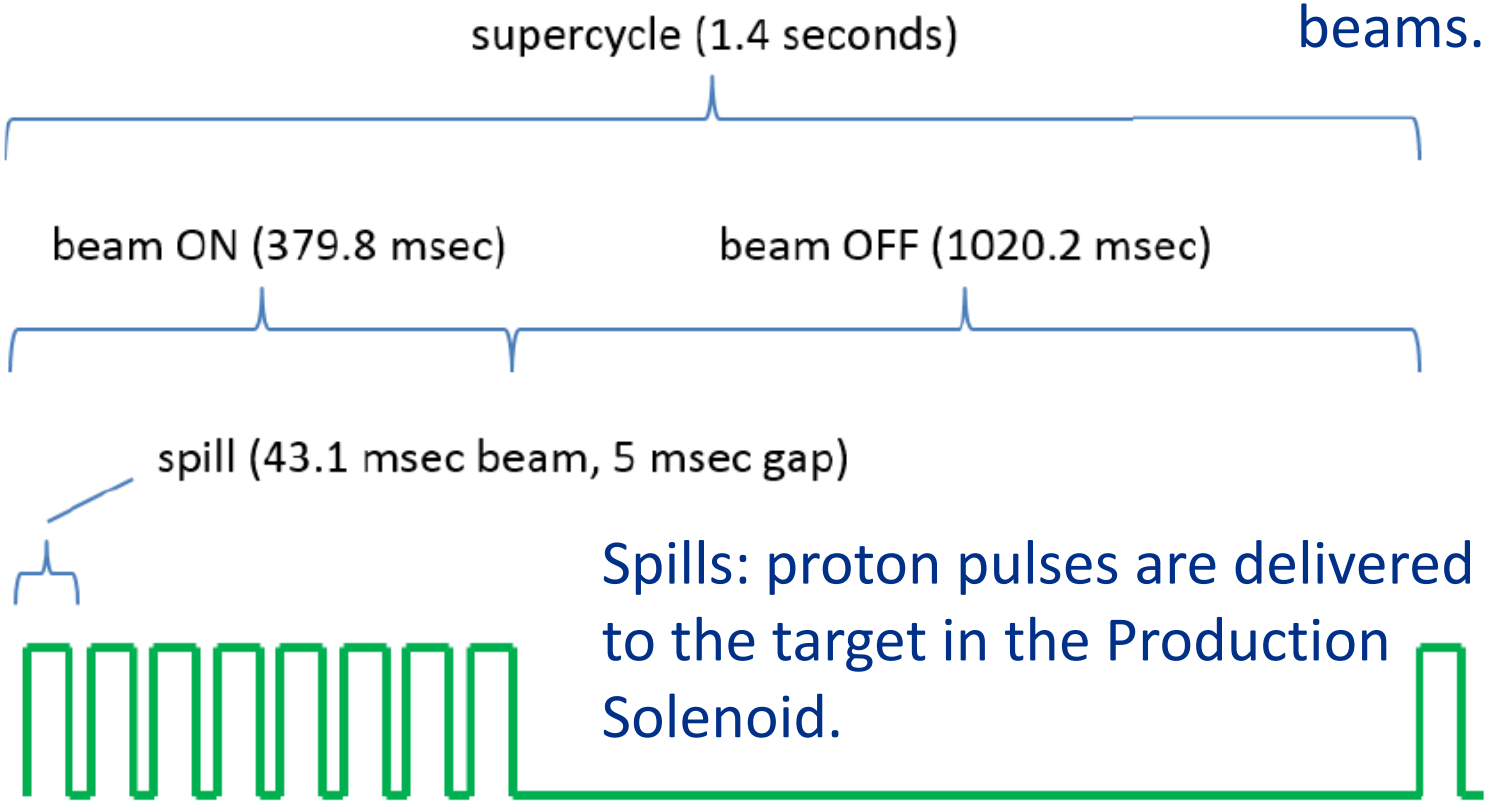
Timing

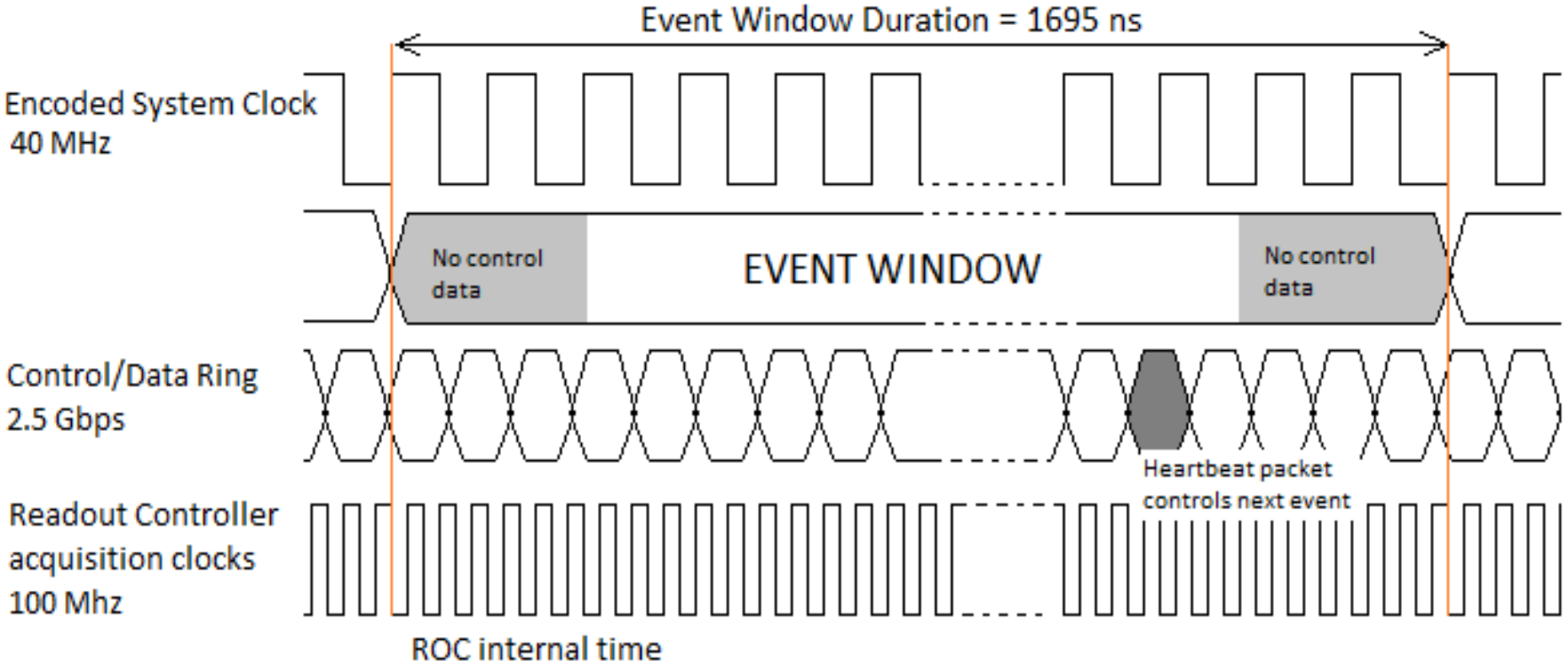
Supercycle: the temporal window between two proton beams.



Spills: proton pulses are delivered to the target in the Production Solenoid.

Each spill contains approximately 32 000 uBunches, for a total of 256 000 Bunches in a 1.4 second supercycle. A Bunch is 1695 ns.

Timing



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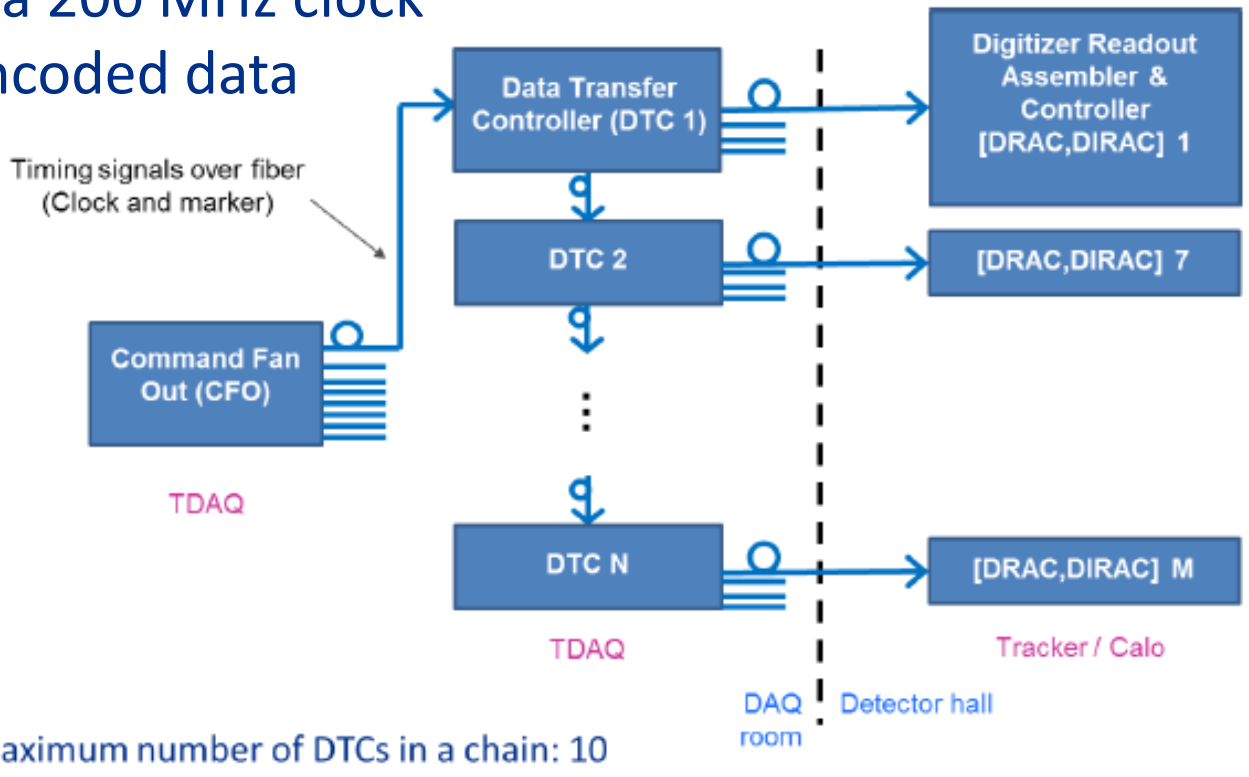
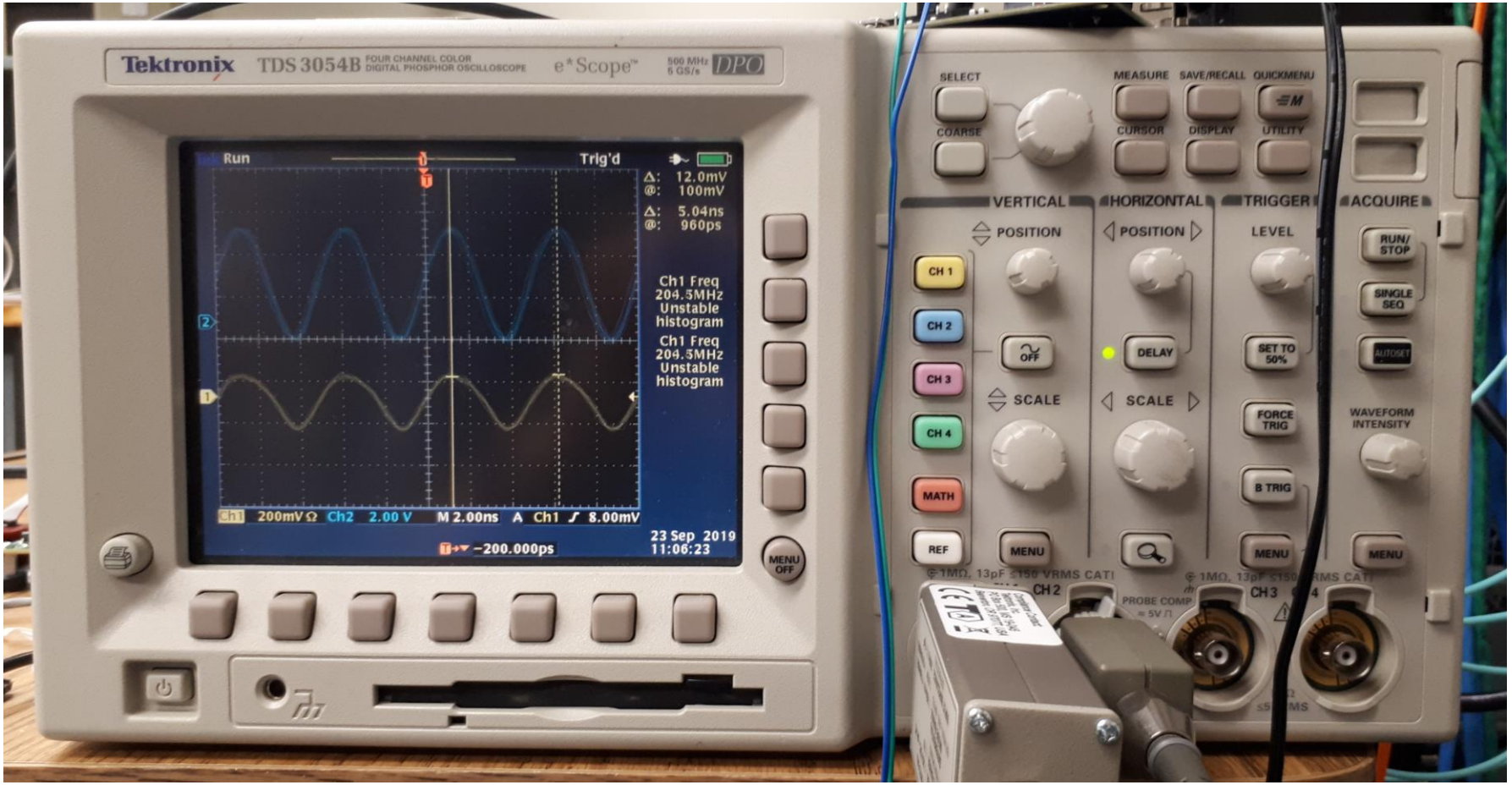
Loopback

1. The Command Fan Out (CFO) is the 40 MHz single clock source and fans out clock to N Data Transfer Control (DTC) units
2. Transmission to the front-end ROCs will be done using optical fiber employing clock-encoded data at 4.0 Gbps
3. ROCs will extract a 200 MHz clock from the clock-encoded data bitstream, which will be used by the ROCs as the Reference Clock for timestamping data.

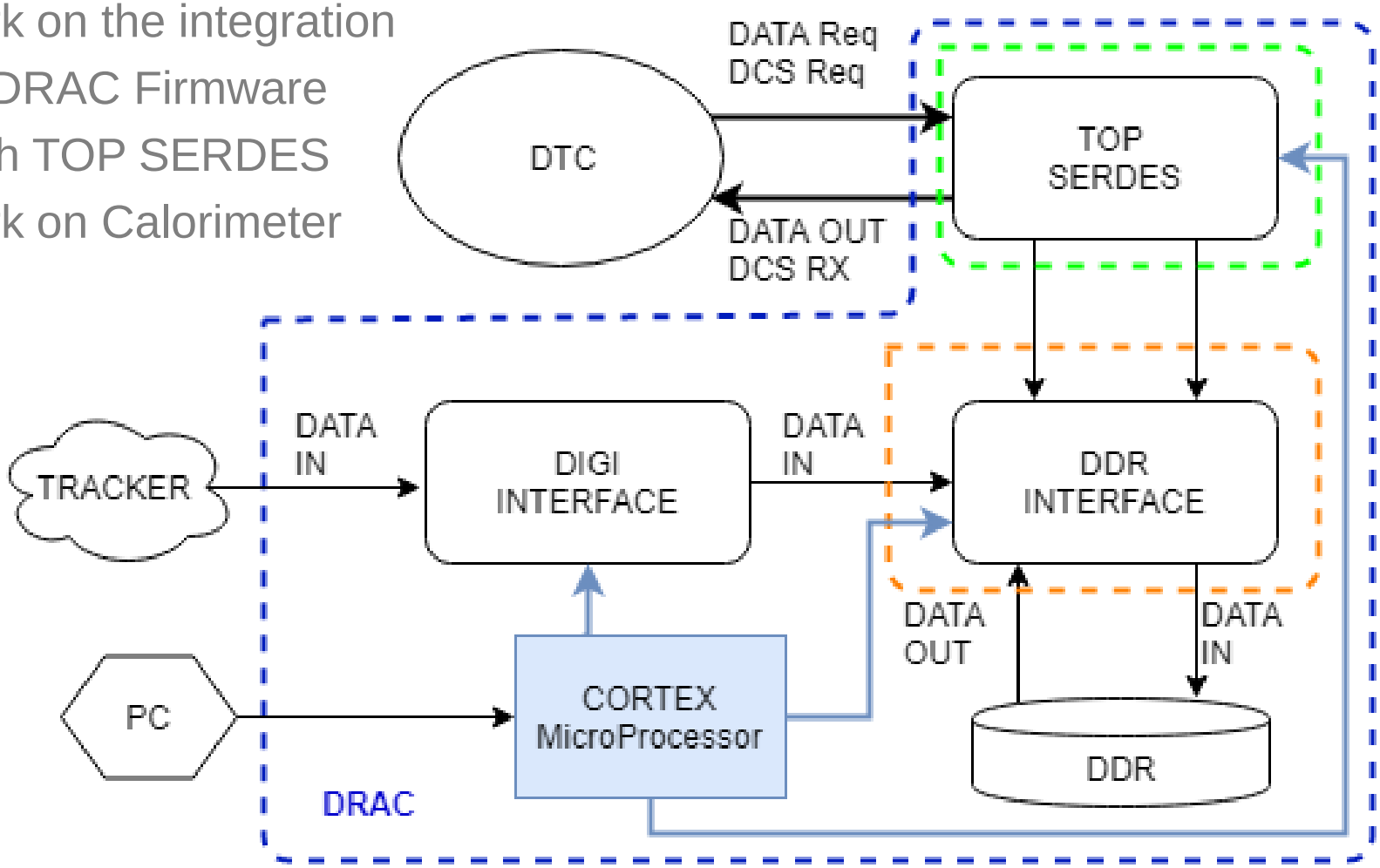


Clock test


Tektronix
TDS 3054B
e*Scope
DPO
Run
Trig'd
Ch1 Freq
204.5MHz
Unstable
histogram
Ch1 Freq
204.5MHz
Unstable
histogram
Ch1 200mV Ω Ch2 2.00 V M 2.00ns A Ch1 8.00mV
−200.000ps
23 Sep 2019
11:06:23
VERTICAL
HORIZONTAL
TRIGGER
ACQUIRE
POSITION
SCALE
LEVEL
CH 1
CH 2
CH 3
CH 4
MATH
REF
MENU
DELAY
SET TO 50%
FORCE TRIG
B TRIG
RUN/STOP
SINGLE SEQ
WAVEFORM INTENSITY

Next goals

- Understand why clock is not recovering and solve that
- Work on the integration
  of DRAC Firmware
  with TOP SERDES
- Work on Calorimeter



Thank you!

DDR INTERFACE

Part of the firmware that handles storage of data and integrity of the DDR memory.