Mu2e Calorimeter electronics

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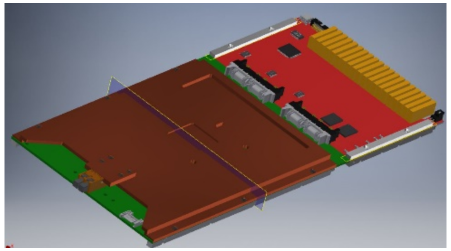
INFN Pisa

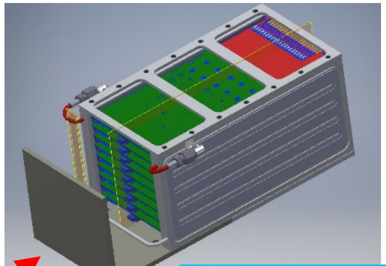
NEWS General Meeting
November 4-5 2019

Talk overview

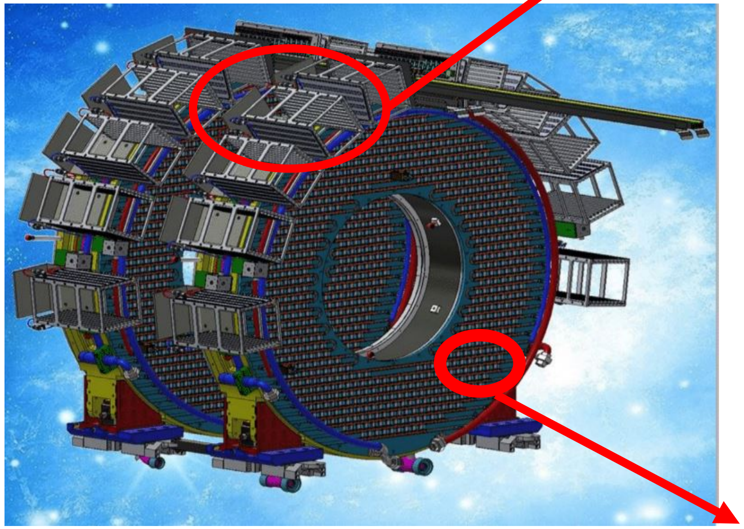
- Calorimeter electronics scheme
- Front End electronics
- DIRAC spec, architecture and design
- DIRAC qualification tests
- Dirac cooling
- Module 0
- Slice test
- Dirac V2

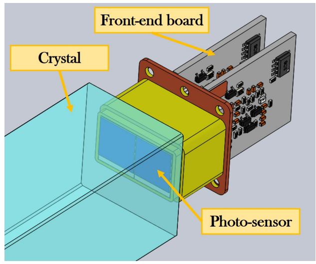
Calorimeter design


DIRAC + Mezzanine


CRATE

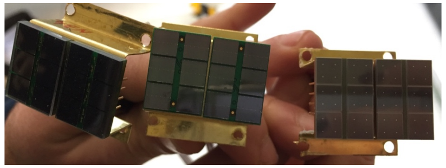

CsI + SiPM + Holder + FEE


Calorimeter disks



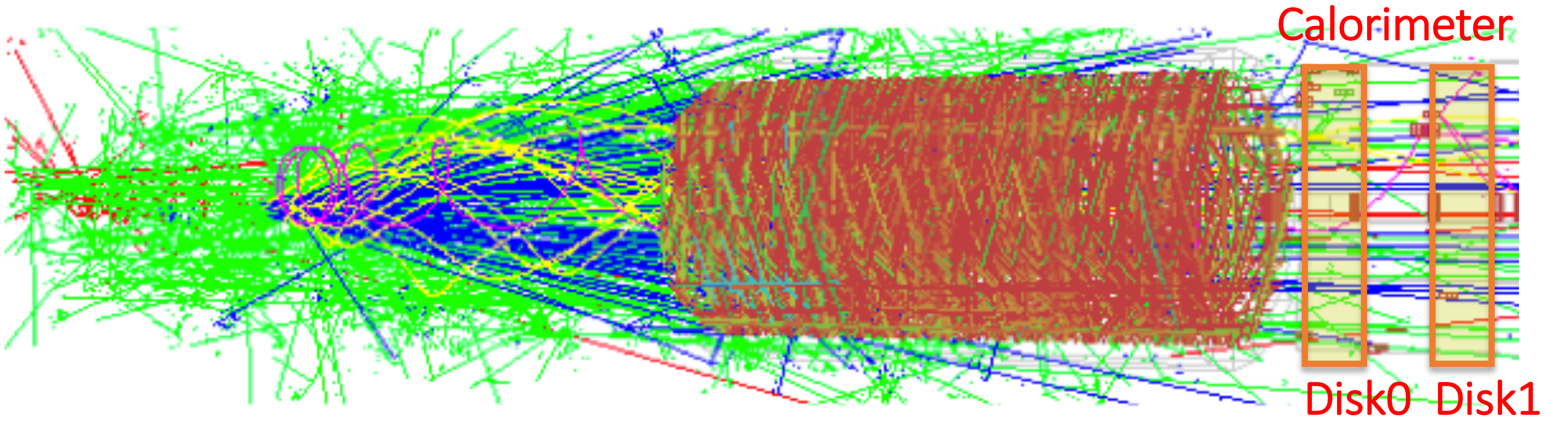
SiPM + Holder + FEE

CsI crystals


UV-extended SiPMs

- **High granularity** → 1348 undoped CsI crystals (3.4x3.4x20 cm^3)
- *Crystals arranged in 2* **disks** (inner/outer radius 37.4 cm / 66 cm, separation between disks 75 cm)
- *1 crystal coupled to 2* UV-extended ***SiPMs*** (14x20 mm^2 area) → 2696 electronic channels
- SiPM packed in a parallel arrangement of 2 groups of 3 cells biased in series
- DAQ ***crates located*** **inside the cryostat** to limit the number of pass-through connectors

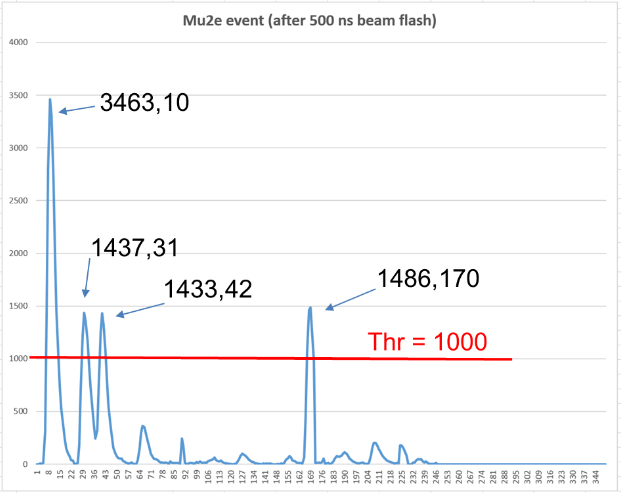
Why a digitizer?



Typical 1.7 µs Mu2e event

Very intense particle flux expected in the calorimeter

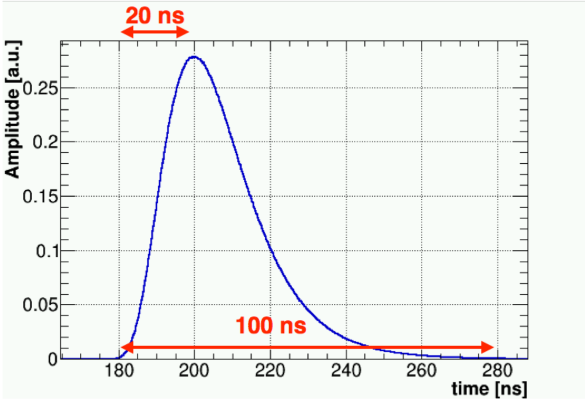
We need *high-sampling rate* digitizers to resolve pile-up

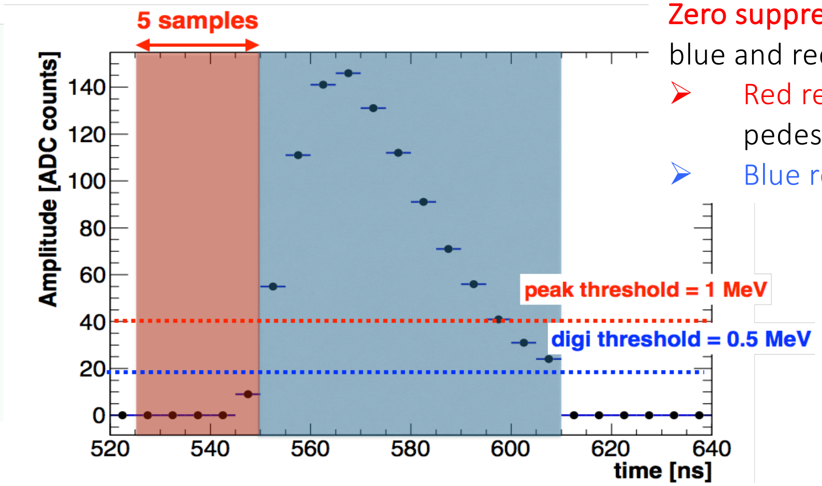


Pile Up Example (Front End output)

Which requirements? (1)

- Digitization requirements = function (calorimeter requirements)
- *Particle-Id:*
  - $\sigma_t < 500$ ps @ 100 MeV
  - $\sigma_E/E < 10\%$ @ 100 MeV
- We require the additional contribution due to the digitization procedure itself to be:
  - ***$\sigma_t < 200$ ps @ 100 MeV***
- Analog input waveform and calorimeter digitization scheme:
  - *Sampling frequency* and number of *ADC readout bits* impact time and energy resolution
  - Thresholds impact the total data throughput and Energy resolution





Zero suppression: acquire **only** samples in blue and red regions

- ➢ Red region needed for time and pedestal calculation
- ➢ Blue region for energy

Which requirements? (2)

- Simulation results show that a digitizer with:
  - Sampling frequency of *200 MHz*
  - ADC with *12 bits resolution*

Matches the calorimeter requirements on time and energy resolution

	150 MHz	200 MHz	250 MHz
8 bits	470 ps	440 ps	440 ps
10 bits	370 ps	250 ps	250 ps
12 bits	300 ps	170 ps	170 ps

Time resolution versus sampling frequency and ADC-bits

- *Time* is reconstructed by fitting the leading edge
- Time resolution for Conversion Electrons (~105 MeV)

	150 MHz	200 MHz	250 MHz
8 bits	9.8 MeV	8.0 MeV	7.8 MeV
10 bits	6.5 MeV	5.5 MeV	5.5 MeV
12 bits	6.2 MeV	5.5 MeV	5.5 MeV

Energy resolution versus sampling frequency and ADC-bits

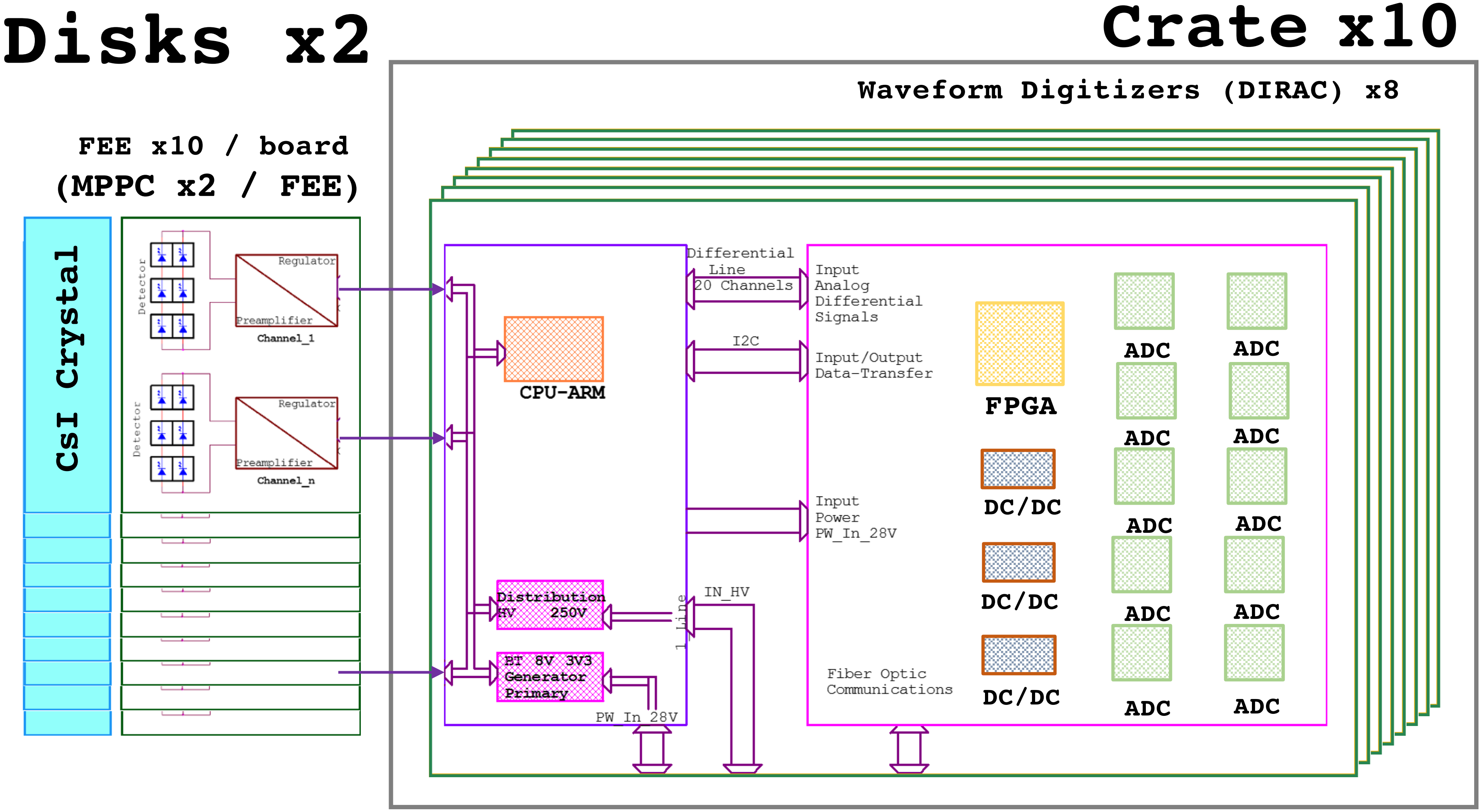
- *Energy* is reconstructed from the total number of ADC counts
- Energy resolution (FWHM/2.35) for Conversion Electrons (~105 MeV)

Which requirements? (3)

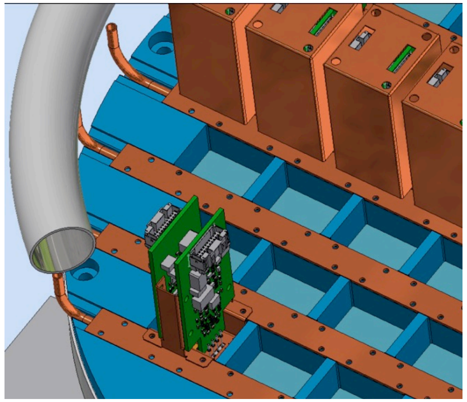
- System located inside the cryostat → *Harsh Environment*:
  - ***Magnetic field** of **1 T** and 10^{-4} Torr vacuum*
  - *Total Ionizing Dose (**TID**):*
    - *0.2 krad/yr (from simulation)*
    - *12 Safety factor (requested from collaboration)*
    - *5 years data taking*
    - *TID **12 krad***
  - ***Neutron flux** 5×10^{10} 1 MeV (Si)/yr (from simulation)*

- Mechanical constraints → DAQ crates located inside the cryostat:
  - *Limited space* → 20 ADC channels/board
  - Limited access for maintenance → ***Highly Reliable Design*** mandatory

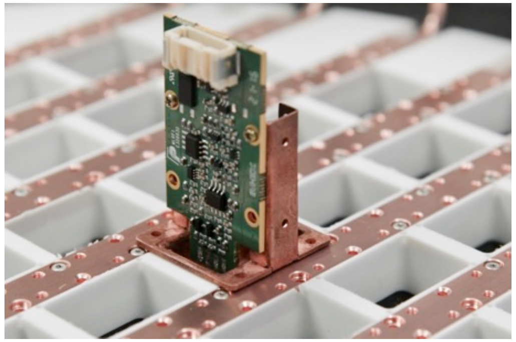
Calorimeter electronics scheme



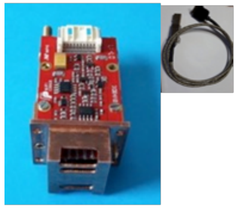
Front End Electronics



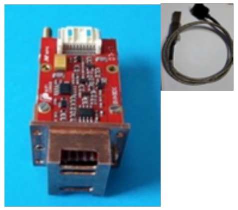
- FE boards connected to SiPMs to provide:
    - *Amplification*
    - Local **linear regulation** of the ***bias voltage***
    - Monitoring of current and temperature
    - Test pulse

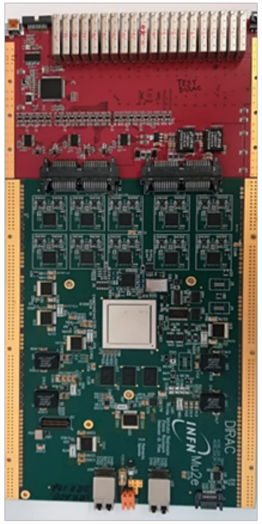


- Mezzanine boards:
    - 20 FE boards controlled by 1 Mezzanine Board (MB) → SiPM LV and HV distributed by an ARM controller
    - ***Differential signals from 20 FE boards sent to MB and then to 1 DIRAC***
- DIRAC:
    - sampling, processing and data transmission to the Mu2e DAQ



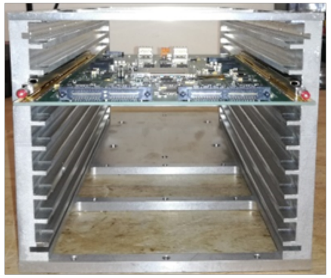
FEE
(X20)



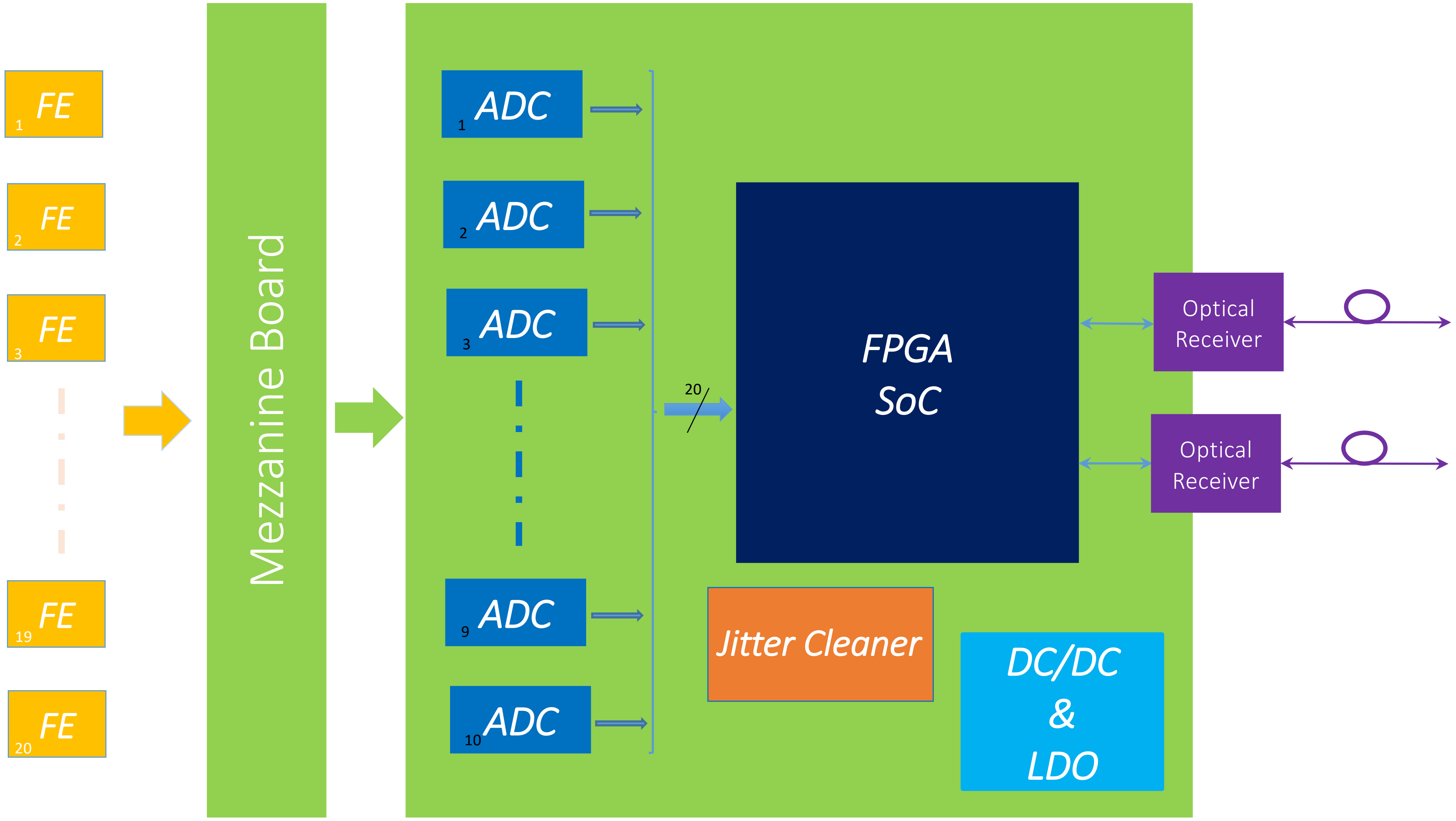


MB + DIRAC (X8)

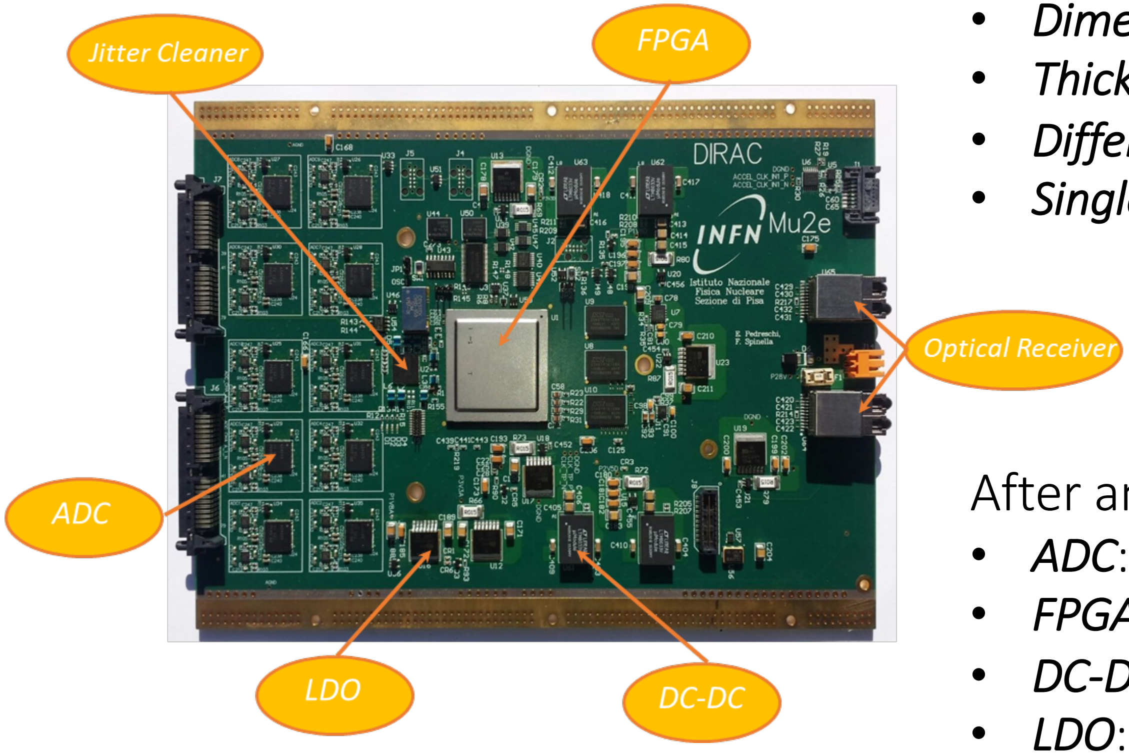
CRATE + DIRAC +MB
X20 (10 + 10)



DIRAC v1 architecture



DIRAC v1 design



PCB specs:

- ***Material:*** *FR408-HR*
- ***Layers:*** *16*
- ***Dimensions:*** *233x165 mm*
- ***Thickness:*** *2.127 mm*
- ***Differencial lines***: 100 Ω
- ***Single ended lines***: *50 Ω*

After an intense campaign of tests:

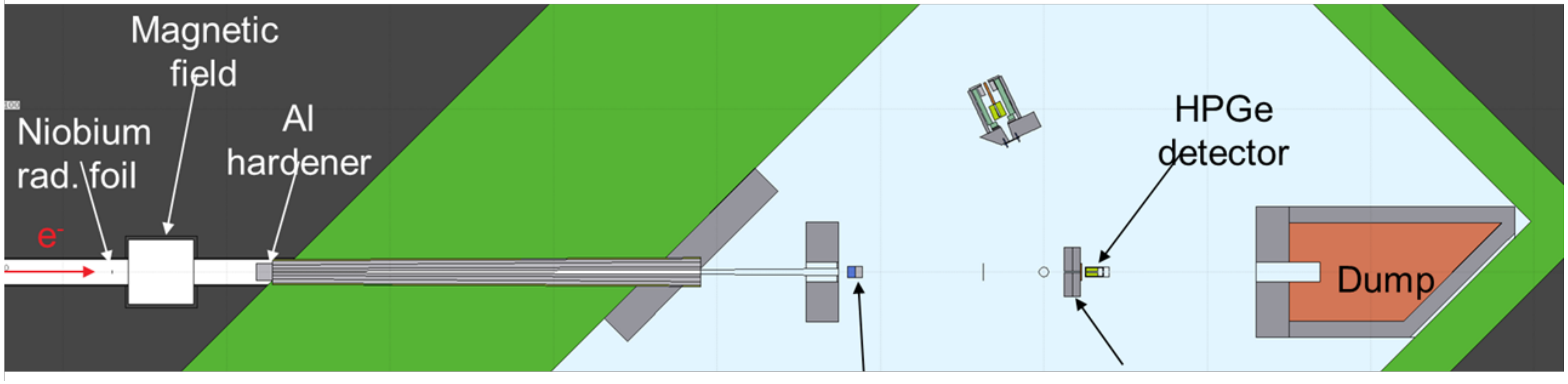
- *ADC*: ADS4229 (Texas Instruments®)
- *FPGA* (SoC): SM2150T (Microsemi®)
- *DC-DC*: LTM8033 (Linear Thecnologies®)
- *LDO*: MIC69502 (Micrel®)
- *Jitter Cleaner*: LMK04828 (Texas Instruments®)
- *Optical Transceiver*: RJ-5G-SX (Cotsworks®)

DIRAC qualification tests

Several test campaigns were performed:

- *Total Ionizing Dose (TID)* ⟶ requested 12 krad:
  - YELBE @HZDR
    - γ from Bremsstrahlung (0<E<14MeV)
    - Extimated dose ≈ 20 krad/h @ 600µA
    - Single components test
  - Calliope @ENEA
    - Co60 source
    - Dose in function of distance: Max 2krad/h, requested 1krad/h
    - Full board test
- ***Magnetic Field (B)***:
  - LASA @INFN Milano (1T)
- ***Neutron irradiation test***
  - FNG @INFN
    - Total neutron flux of 1.2 x10^12 n 1 MeV (Si) / cm^2
    - Total neutron flux of 6x10^11 n 1 MeV (Si) / cm^2
    - DCDC test

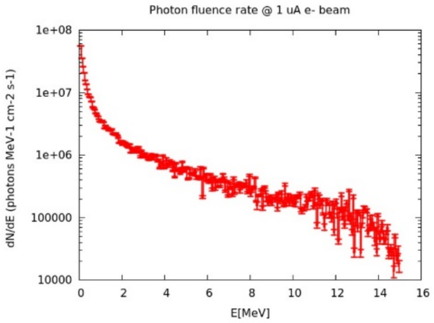
YELBE facility



- Photons is produced per Bremsstrahlung by the electron beam hitting a niobium foil in the accelerator hall
- Nominal beam conditions:
  17 MeV electrons, 600uA, 12.4 um niobium radiator foil

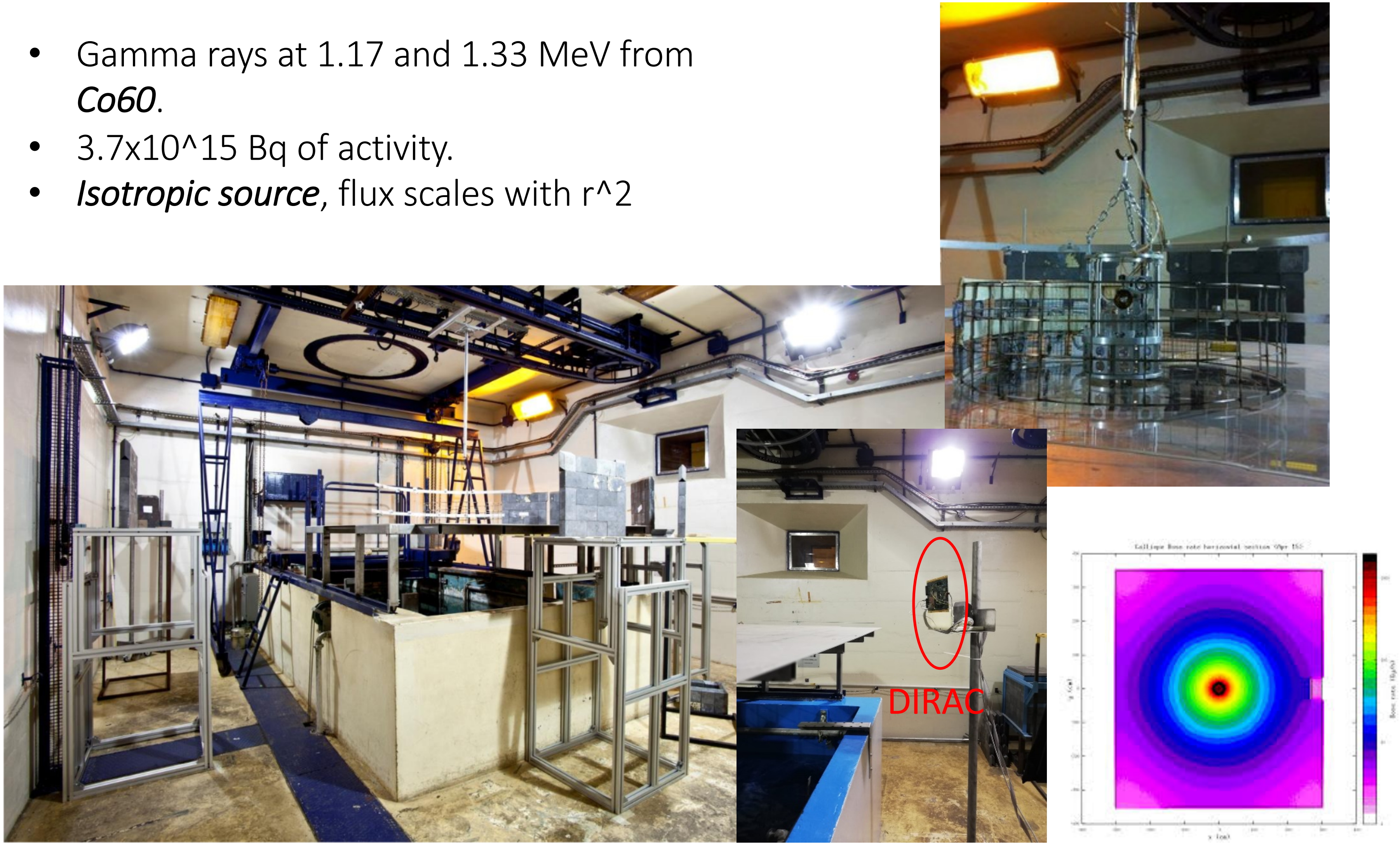
- Simulated ***dose rate ≈ 18.6 krad/h***

- Active dosimetry used to confirm simulated dose rate

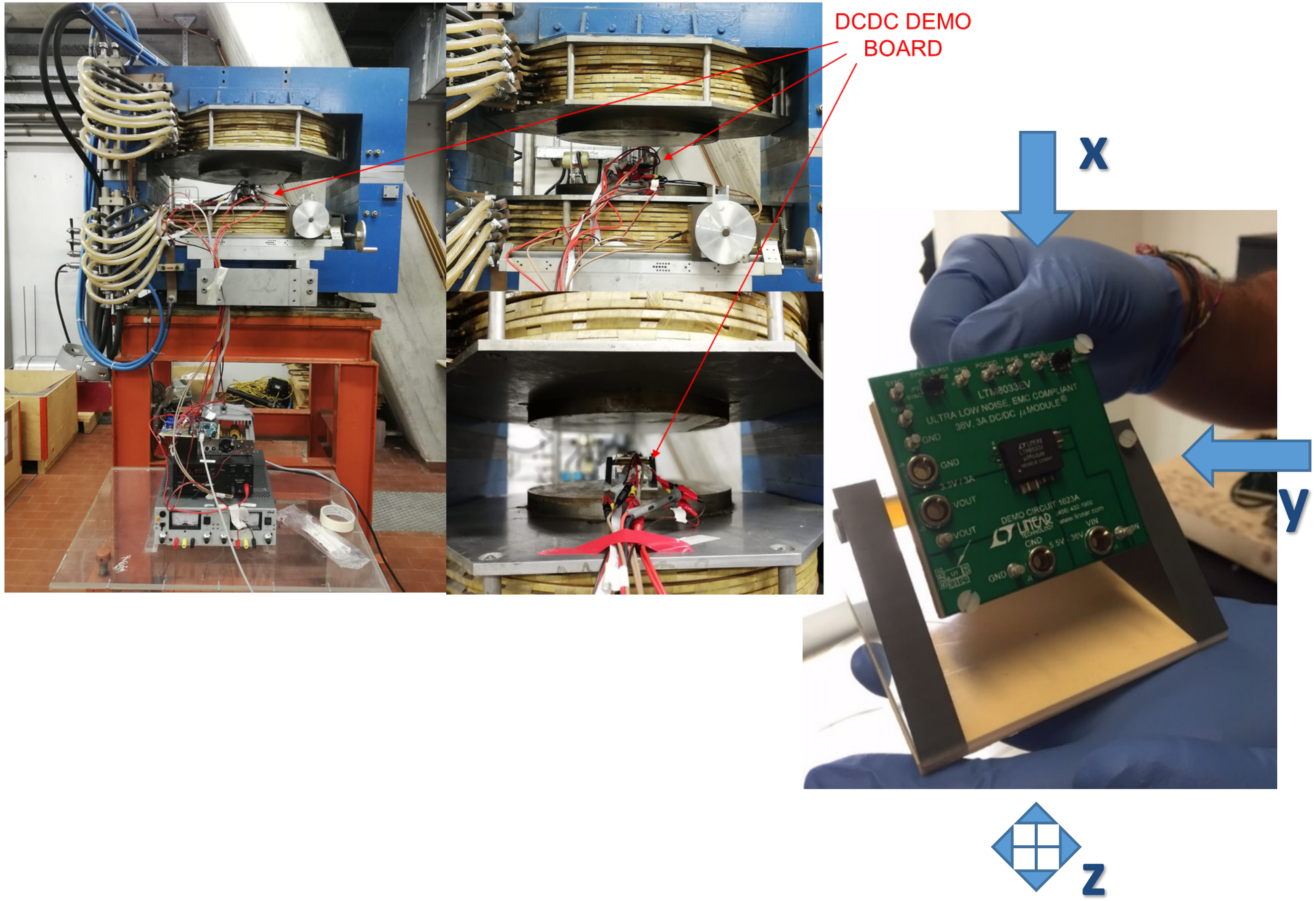


Calliope facility

- Gamma rays at 1.17 and 1.33 MeV from *Co60*.
- 3.7x10^15 Bq of activity.
- *Isotropic source*, flux scales with r^2



LASA facility

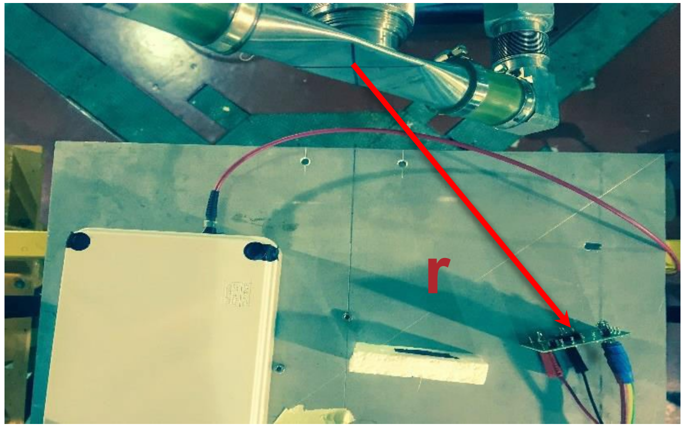


- *Uniform magnetic field up to 1.2 T*
- We tested different orientations of the DCDC with respect to the magnetic field
- Same setup of the radiation tests

FNG facility

Frascati Neutron Generator (FNG) is a linear electrostatic accelerator in which up to 1 mA D+ ions are accelerated onto a Tritium target

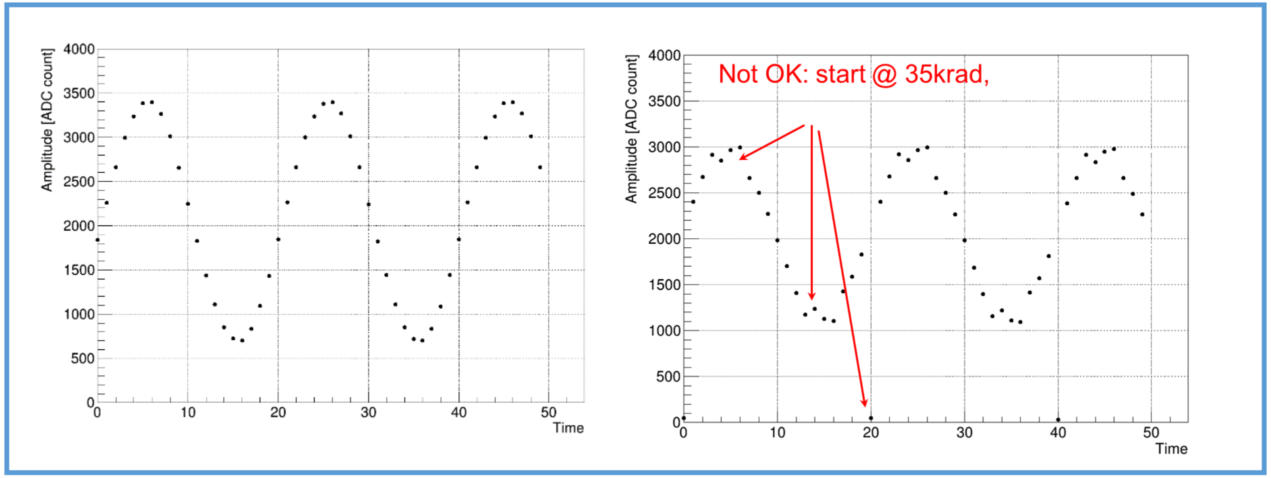
- *Up to 10^11 14 MeV neutrons/s*
- almost ***isotropic source***, flux scales with r^2
- calibrated at 3% level using alpha particles



D+T→ α +n

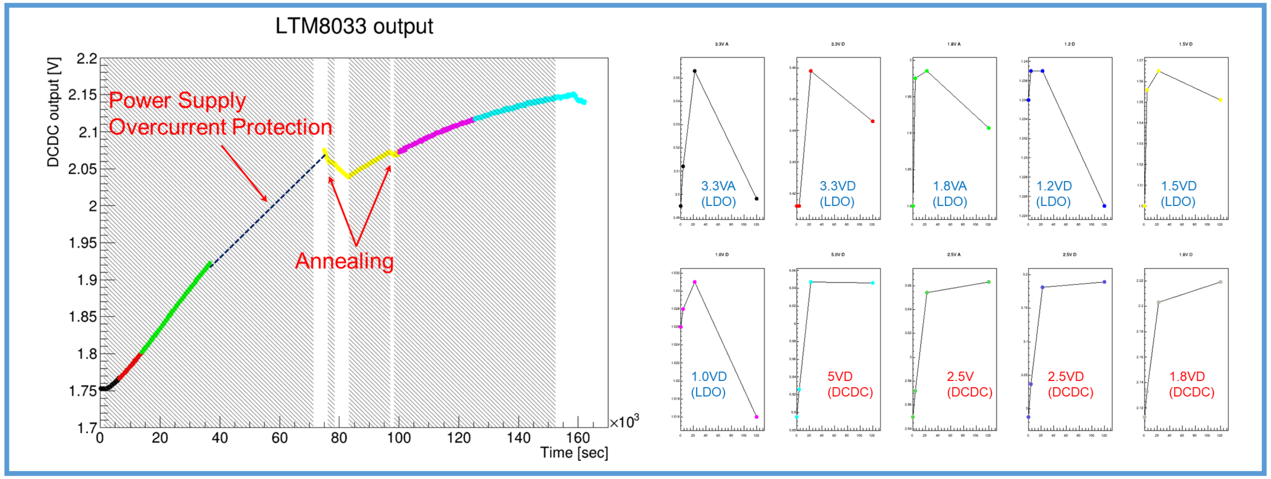
DIRAC: TID test results

- Input waveform →4.5@10MHz, readout waveform:



Not OK: start @ 35krad,

- LTM8033 and MIC69502 Vout(rad;t)



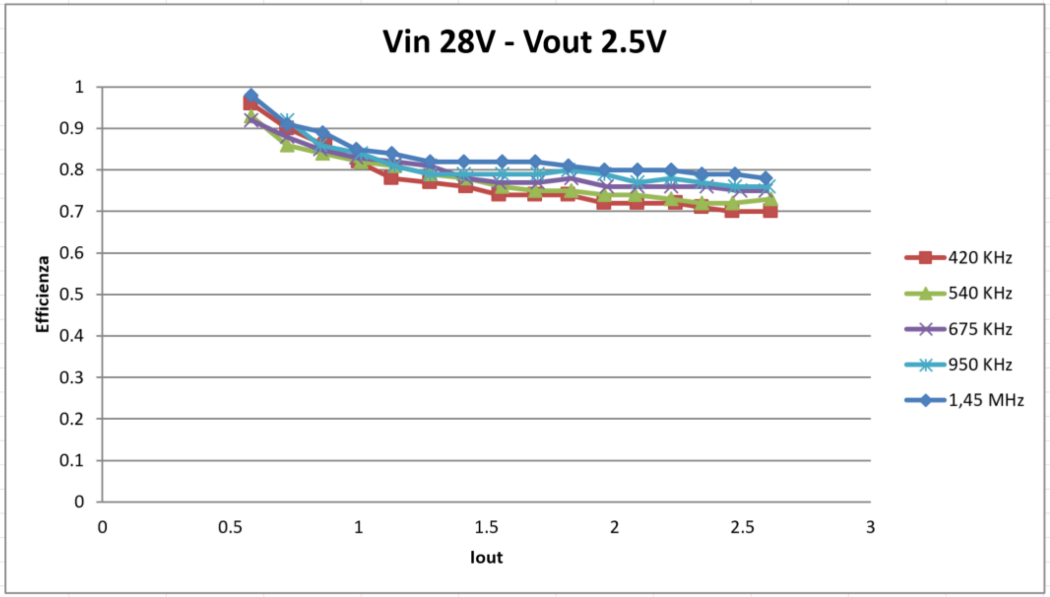
Power Supply Overcurrent Protection

Annealing

Conclusions:

- 41 h beam time
- Nominal Dose Rate ≈ 1krad/h
- TID ≈ 41krad
- No evidence of broken components up to 35 krad
- After 41 krad SM2 ARM does not restart after power cycle
- DCDC converters voltage increase: ≈ 20% @ 41 krad, no recover if no beam CHANGE IN V2
- LDO small increase, fast recover if no beam

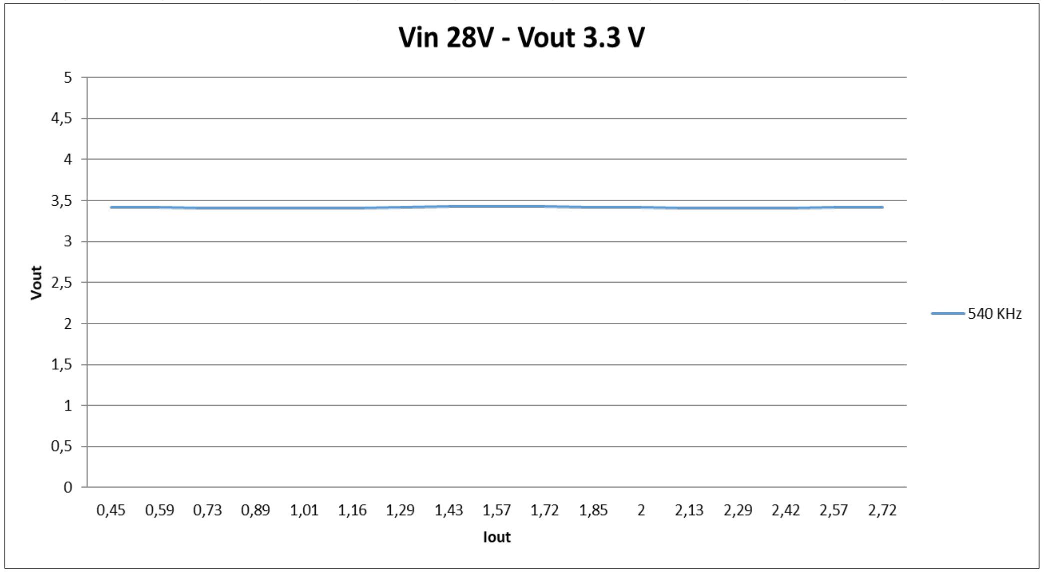
Tests in magnetic field results



Test conditions:

- View X (parallel to B)
- Vin 28V, Vout 2.5V
- Variable load
- Switching frequency

Efficiency quite low (still acceptable), higher if Vin lower

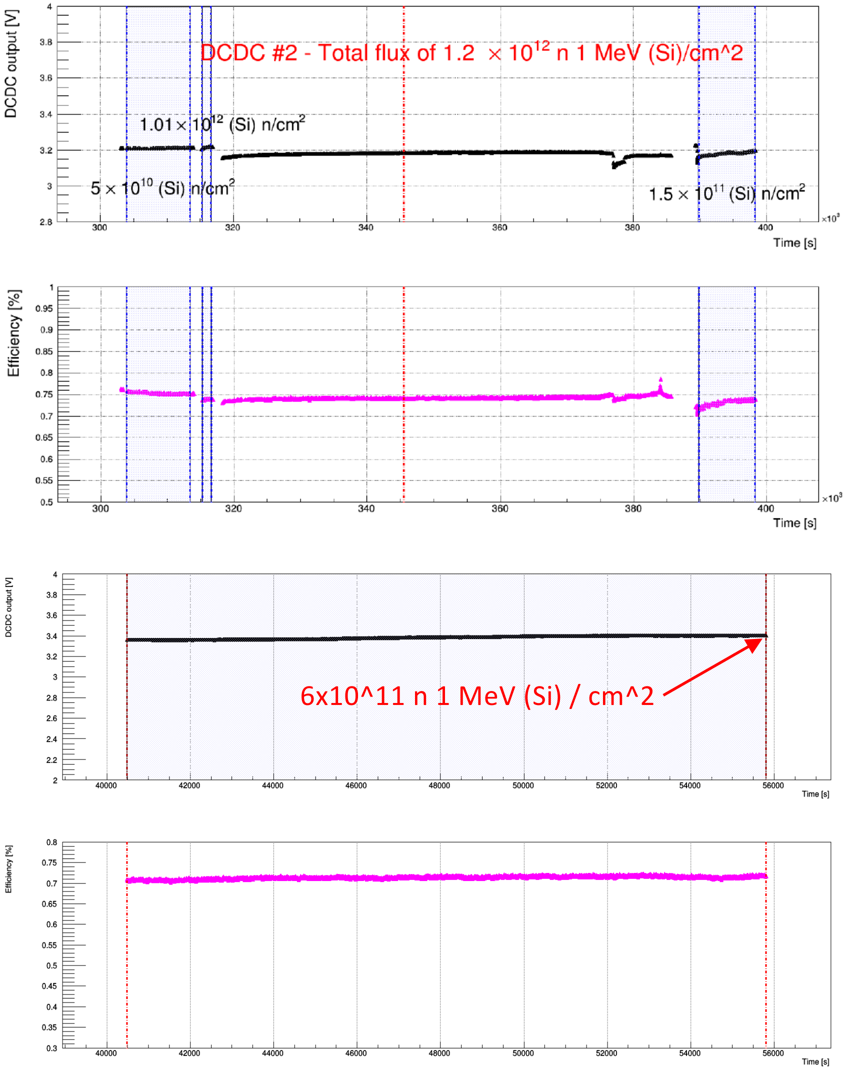


Test conditions:

- View X (parallel to B)
- Vin 28V, Vout 3.3V
- Variable load
- Constant frequency

Vout constant

LTM 8033 Neutrons tests



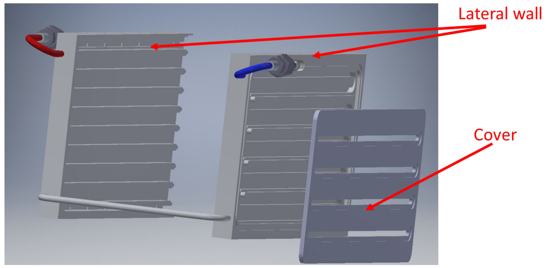
Test conditions:

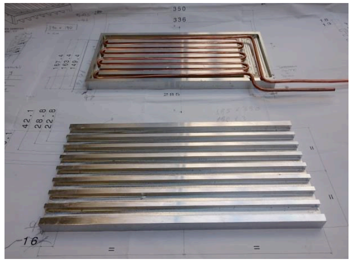
- Neutrons over DCDC up to 1.2E12 1MeV-eq-Neutrons/cm2
- DCDC Vout (loaded with 1 ohm resistor):
  - Measured before irradiation
  - Measured after the test

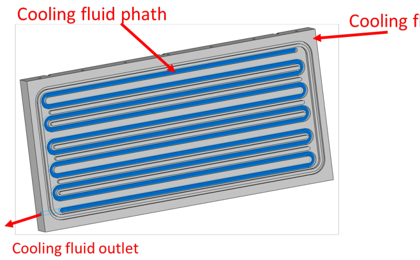
Negligible change …

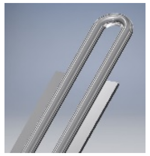
DIRAC cooling (1)

- **General cooling requirements**:
  - Maximum temperatures must not be exceed during operation → the max electronic components temperature is set to half specified values → set max temp = 60 ^{0}C
  - The ***cooling system*** must be ***robust and reliable***
  - ***Leak less*** cooling system
  - All component must be ***compatible with magnetic field***
  - All parts must have a low outgassing rate for ***operating in vacuum***
  - Components must be ***radiation hard***
- A ***compact crate*** with 9 slots designed → ***house the boards and provides their cooling***
  - The cooling channels are milled on the lateral walls of the crate and sealed with a welded covers



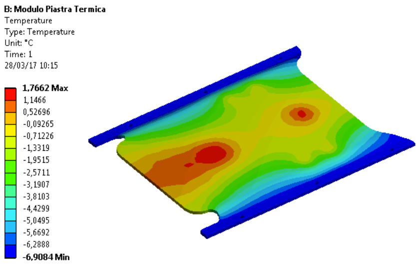


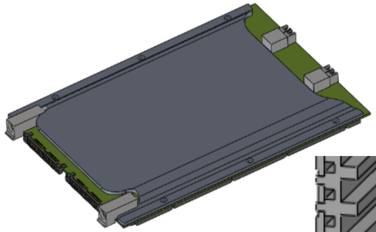


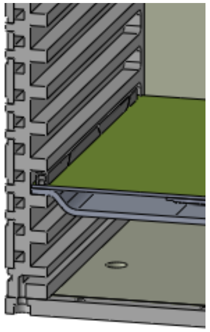


DIRAC cooling (2)

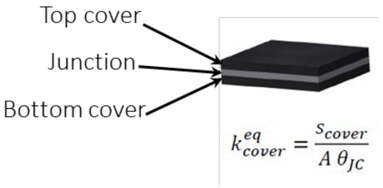
- DIRAC estimated power ***20W***
- 8 DIRAC/crate + MB ⟶ ***200 W/crate***
- **Vacuum environment** ⟶ the ***heat generated*** from the components is ***removed*** through:
    - *Thermal plate* (Cu) pre-formed (radiator)
    - Thermal Interface Material (TIM): *thermal grease*
    - *Bridge resistors* (Beryllium Oxide)
    - *Card Lok* Retainer (CALMARK® Series 265)
- The electronic components modeled in three regions: top cover, junction and bottom cover
- TIM allows the thermal contact between the top cover and the thermal plate



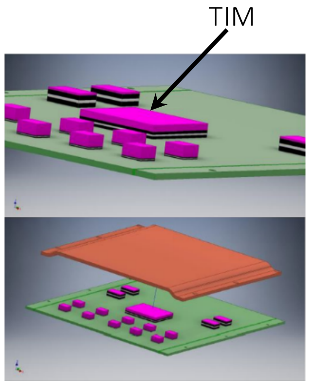




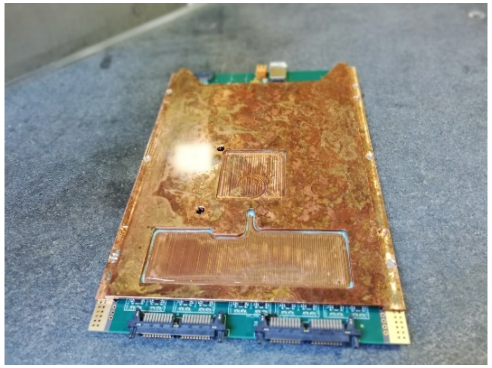
Bridge resistors



$$k^{eq}_{cover} = \frac{s_{cover}}{A\,\theta_{JC}}$$

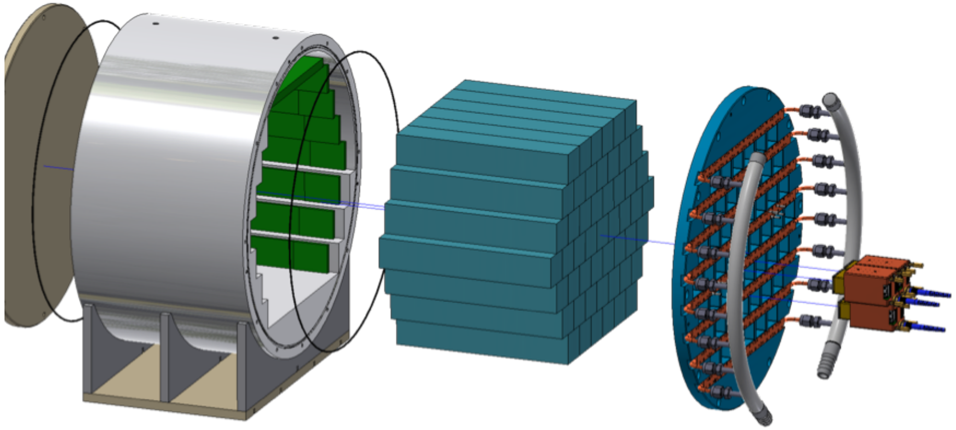


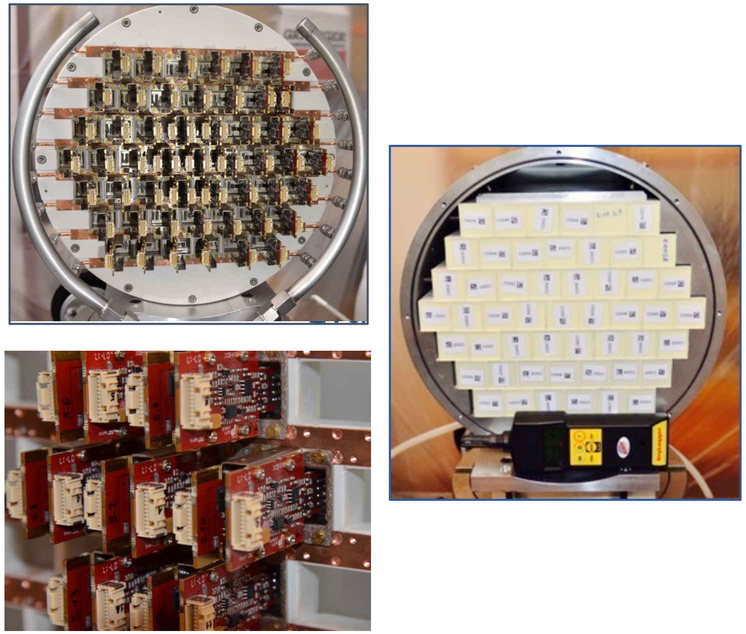
Card Lok



DIRAC + Cu Thermal plate

Module-0





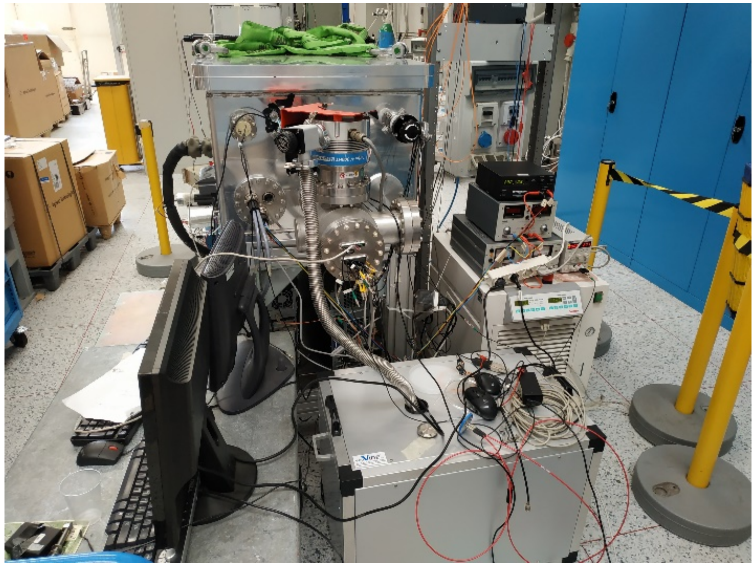
- Large scale EMC prototype:
    - 51 CsI crystals
    - 102 Mu2e SiPMs
    - 102 FEE boards
    - 1 DIRAC board handle 20 channels
- Mechanics and cooling system similar to the final ones (vacuum and low T)

Goals:

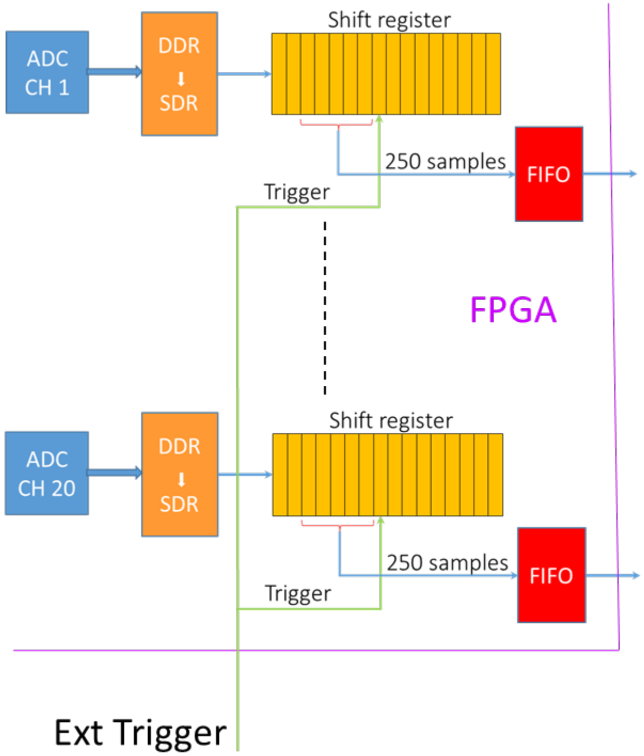
- Validate the acquisition chain → *Slice Test*
- Test integration and assembly procedures

Slice test

- Calorimeter electronics readout chain test using cosmic rays
- Module-0 equipped with FE boards
- SIPMs cooled @18°C (external chiller)
- 1 DIRAC v1 (16 channels) + 1 MB
- Firmware → Preliminary version
- External trigger → Cosmic ray coincidence



Slice test firmware



Firmware:

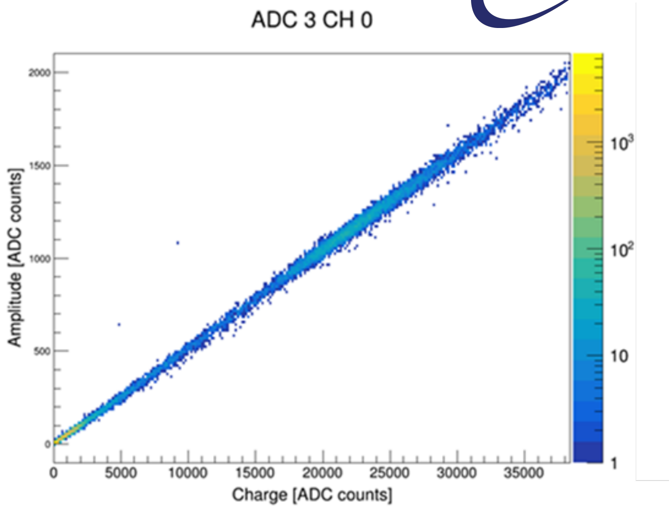
- Initializes ADCs and Jitter Cleaner
- Synchronizes clock phases
- Digitizes 20 channels @ 200 MHz (DDR)
- Stores 250 samples for channel, with an initial buffer of 60 before the trigger (1.2 µs) without zero suppression
- *External trigger* ⟶ 2 plastic scintillator paddles coupled PMTs placed over and below the Module-0 (outside the vessel)
- Binary data output through UART interface @ 1 Mbs (event rate 5Hz enough for cosmics)

DAQ software:

- Written in python and C++, based on ROOT libraries
- Transforms the received binary data in a standard rootopla containing:
  - *The waveform*
  - Reconstructed quantities like pedestals, ***charge*** and time
- Online monitor

Slice test results

An example of the resulting waveform (Fig.A) and the distribution of the peak amplitude versus the integrated charge (Fig.B) is shown



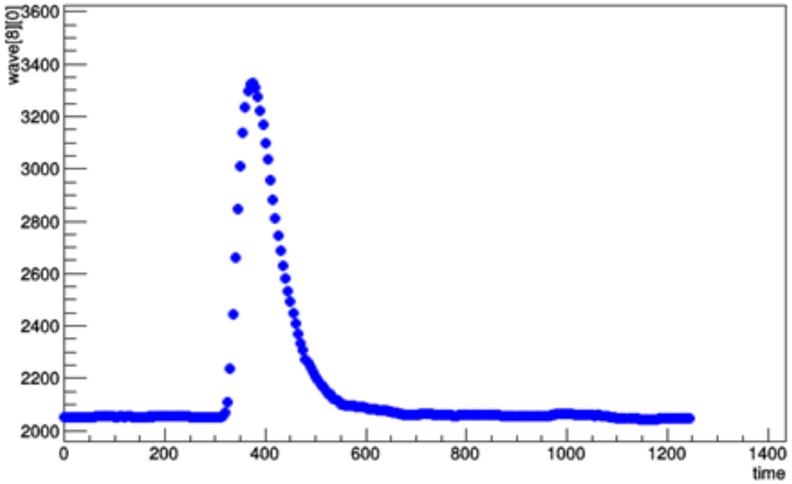


Fig.A: Resulting waveform

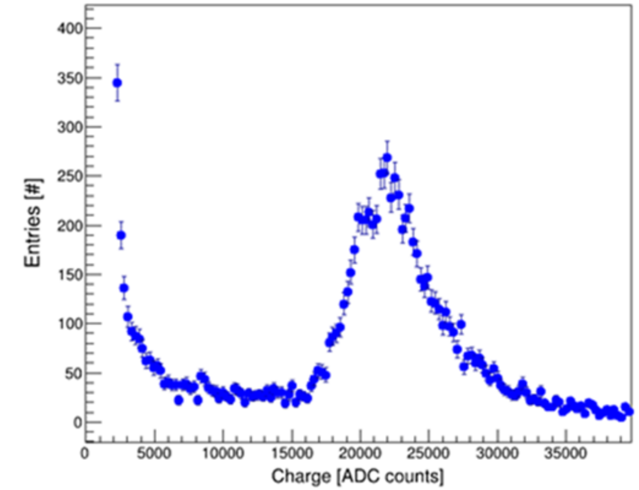


Fig.B: Energy distribution deposited by cosmic rays (ADC counts)

DIRAC v2

Changes due to radiation resistance:

- FPGA: Microsemi PolarFire® MPF300 (FGC1152, 300K LE, 512 user IO, 20.6 Mbits RAM) was M2S150
- Optical tranceiver: CERN VTRX (radhard up to 1Mrad) was Cotswork RJ-5G-SX
- DCDC converters: Texas Instruments® LMZM33606 was Linear Technology LTM®8033

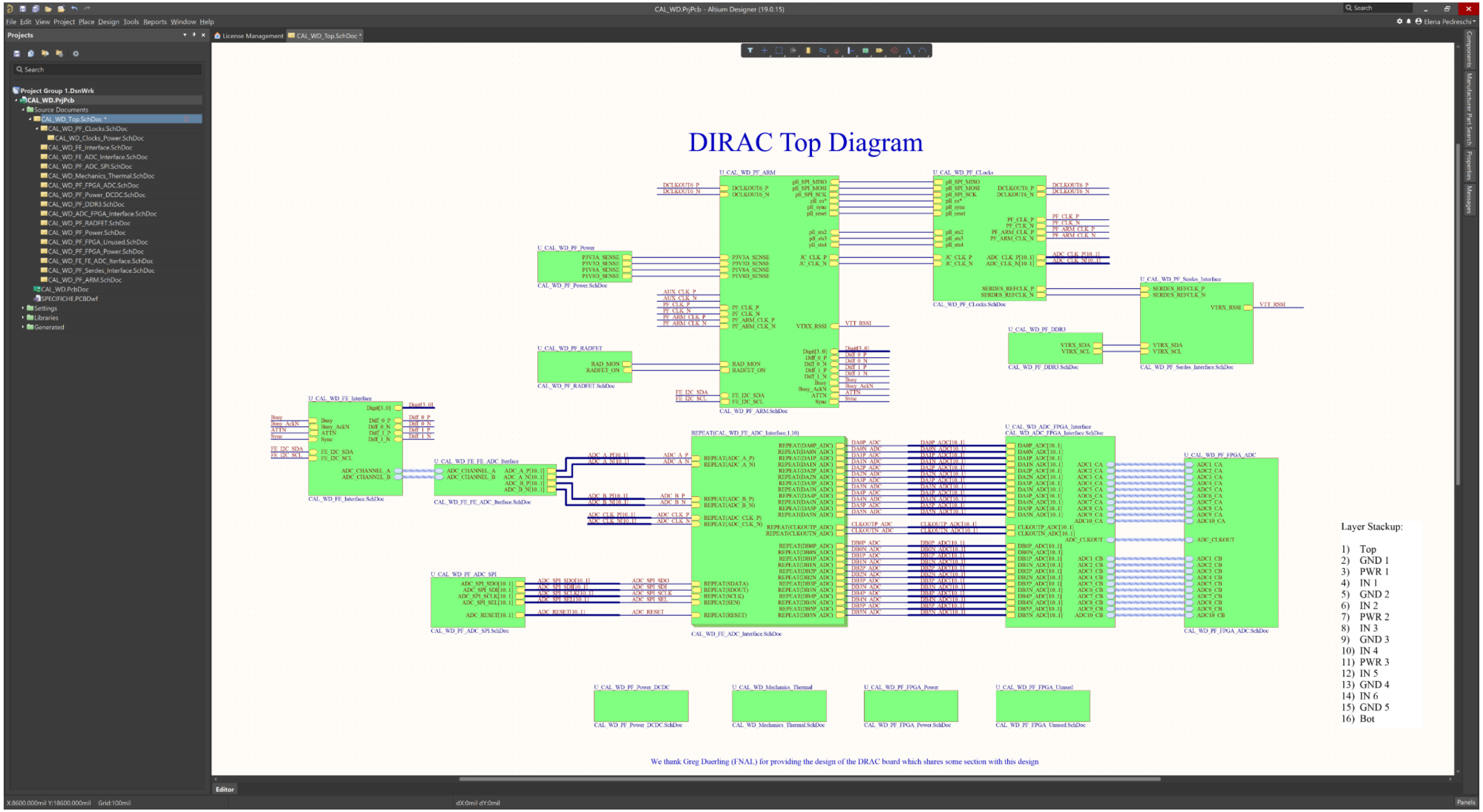
Changes due to changes in specifications:

- Clock chain encoded in the data
- Readout point-to-point (only one optical driver)
- CAN BUS
- DDR3 bigger

DIRAC V2 status:

- TID, neutrons and B tests performed to validate all new components
- Single channel test to verify MPF300/ADS4229 compatibility
- Prototype should arrive in November

DIRAC v2 design



Project Group 1.DsnWrk
- CAL_WD.PrjPcb
  - Source Documents
    - CAL_WD_Top.SchDoc *
      - CAL_WD_PF_CLocks.SchDoc
        - CAL_WD_Clocks_Power.SchDoc
      - CAL_WD_FE_Interface.SchDoc
      - CAL_WD_FE_ADC_Interface.SchDoc
      - CAL_WD_PF_ADC_SPI.SchDoc
      - CAL_WD_Mechanics_Thermal.SchDoc
      - CAL_WD_PF_FPGA_ADC.SchDoc
      - CAL_WD_PF_Power_DCDC.SchDoc
      - CAL_WD_PF_DDR3.SchDoc
      - CAL_WD_ADC_FPGA_Interface.SchDoc
      - CAL_WD_PF_RADFET.SchDoc
      - CAL_WD_PF_Power.SchDoc
      - CAL_WD_PF_FPGA_Unused.SchDoc
      - CAL_WD_PF_FPGA_Power.SchDoc
      - CAL_WD_FE_FE_ADC_Iterface.SchDoc
      - CAL_WD_PF_Serdes_Interface.SchDoc
      - CAL_WD_PF_ARM.SchDoc
    - CAL_WD.PcbDoc
    - SPECIFICHE.PCBDwf
  - Settings
  - Libraries
  - Generated

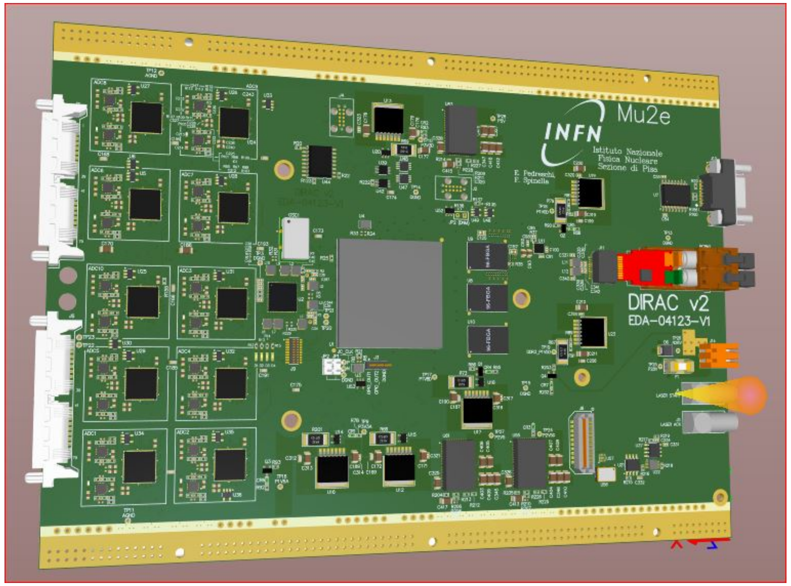
DIRAC Top Diagram

Layer Stackup:

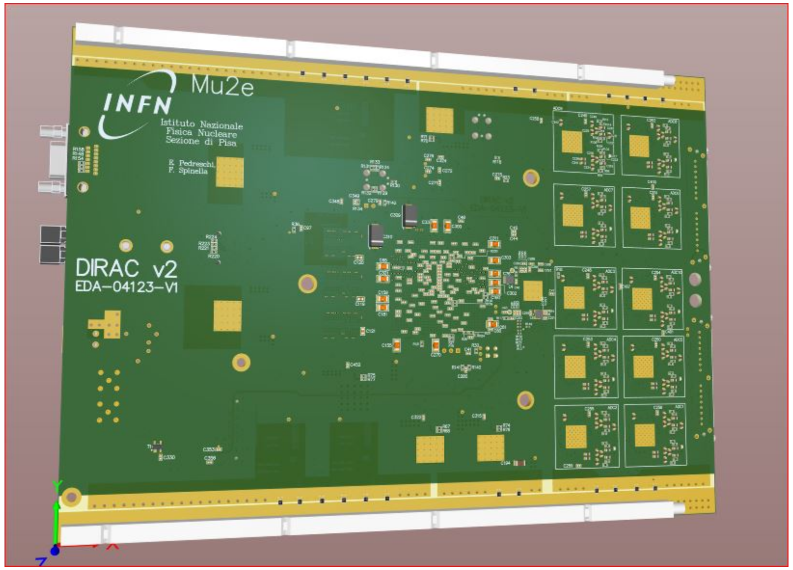
1) Top
2) GND 1
3) PWR 1
4) IN 1
5) GND 2
6) IN 2
7) PWR 2
8) IN 3
9) GND 3
10) IN 4
11) PWR 3
12) IN 5
13) GND 4
14) IN 6
15) GND 5
16) Bot

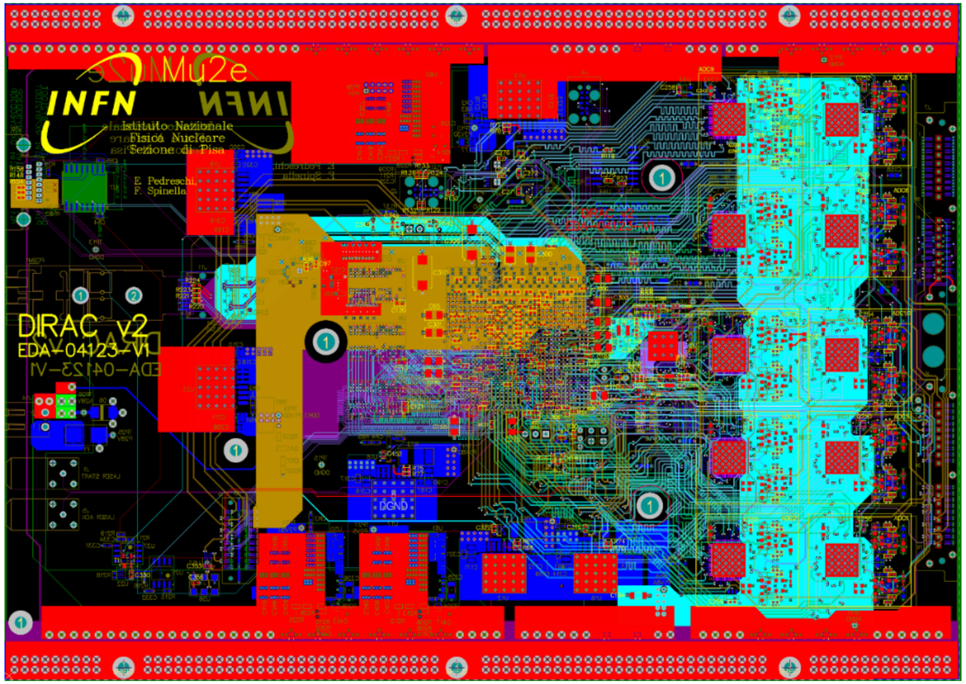
We thank Greg Duerling (FNAL) for providing the design of the DRAC board which shares some section with this design

DIRAC v2 PCB



- Design @ INFN Pisa: *COMPLETED*
- Routing @ CERN: *COMPLETED*
- PCBs under *PRODUCTION*
- The boards assembled (2 prototypes) will be ready in November





Conclusions

- A waveform digitizer designed to operate in hostile environment has been presented
- The DIRAC is designed to sample @200 MHz differential signals coming from the FEE of the DAQ of the electromagnetic calorimeter of the Mu2e experiment
- The presence of vacuum (10^{-4} Torr), high magnetic fields (1T) and radiation (Non-Ionizing Energy Loss 5×10^{10} n/cm^2 @ 1 MeV$_{eq}$ (Si)/y and Total Ionizing Dose 12 Krad) makes the environment particularly harsh and the design of the board very challenging
- A slice test on Module 0 has been performed and it validated the acquisition chain
- A new version V2 has been designed to strenghten the radiation hadrness