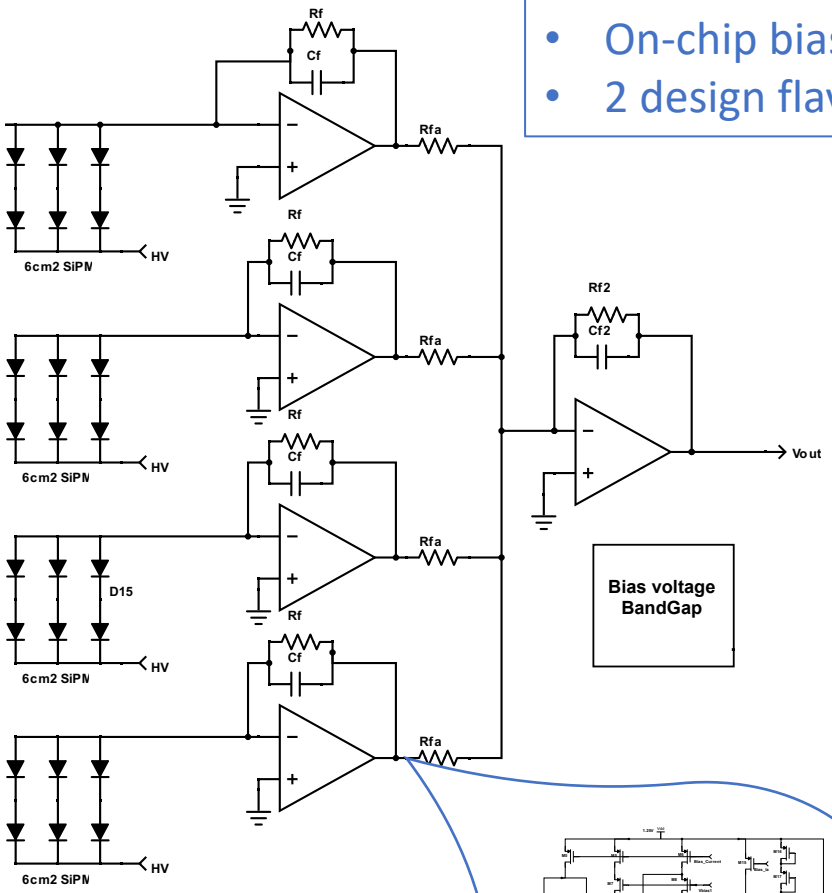
Alejandro Martinez

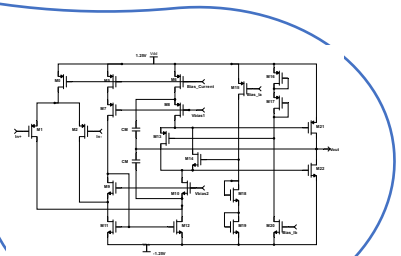
INFN Torino

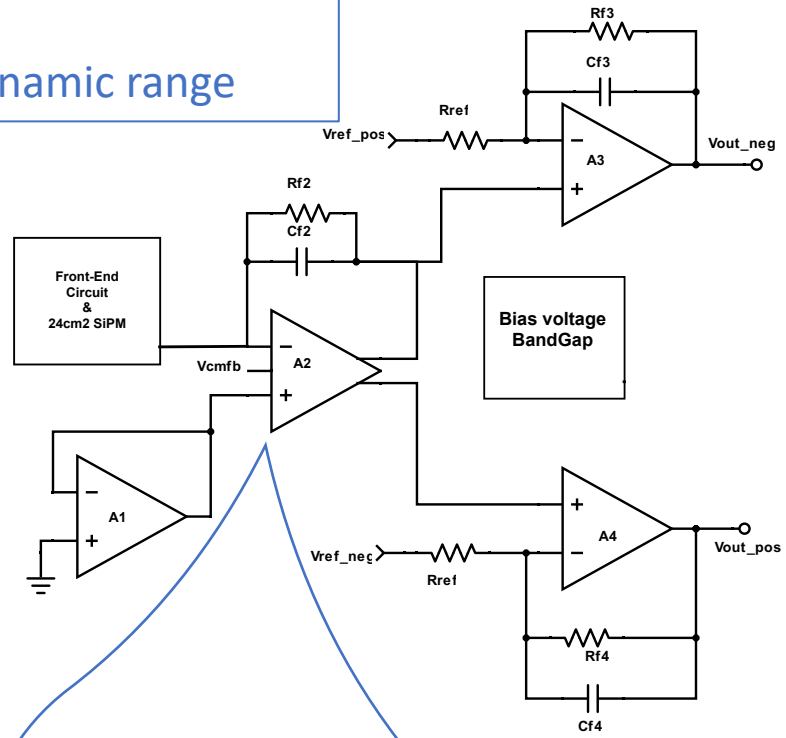
Update: DS20K_V3

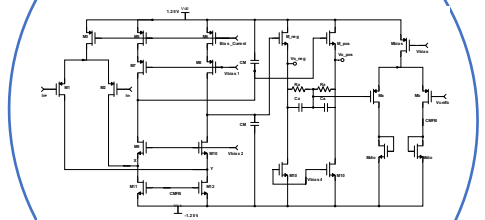
Block Diagram of DS20_V3 chip

- Single-ended and differential output available (s.e.-to-diff converter on dedicated power domain)
- On-chip bias and bandgap
- 2 design flavours, 100 or 300 PE dynamic range









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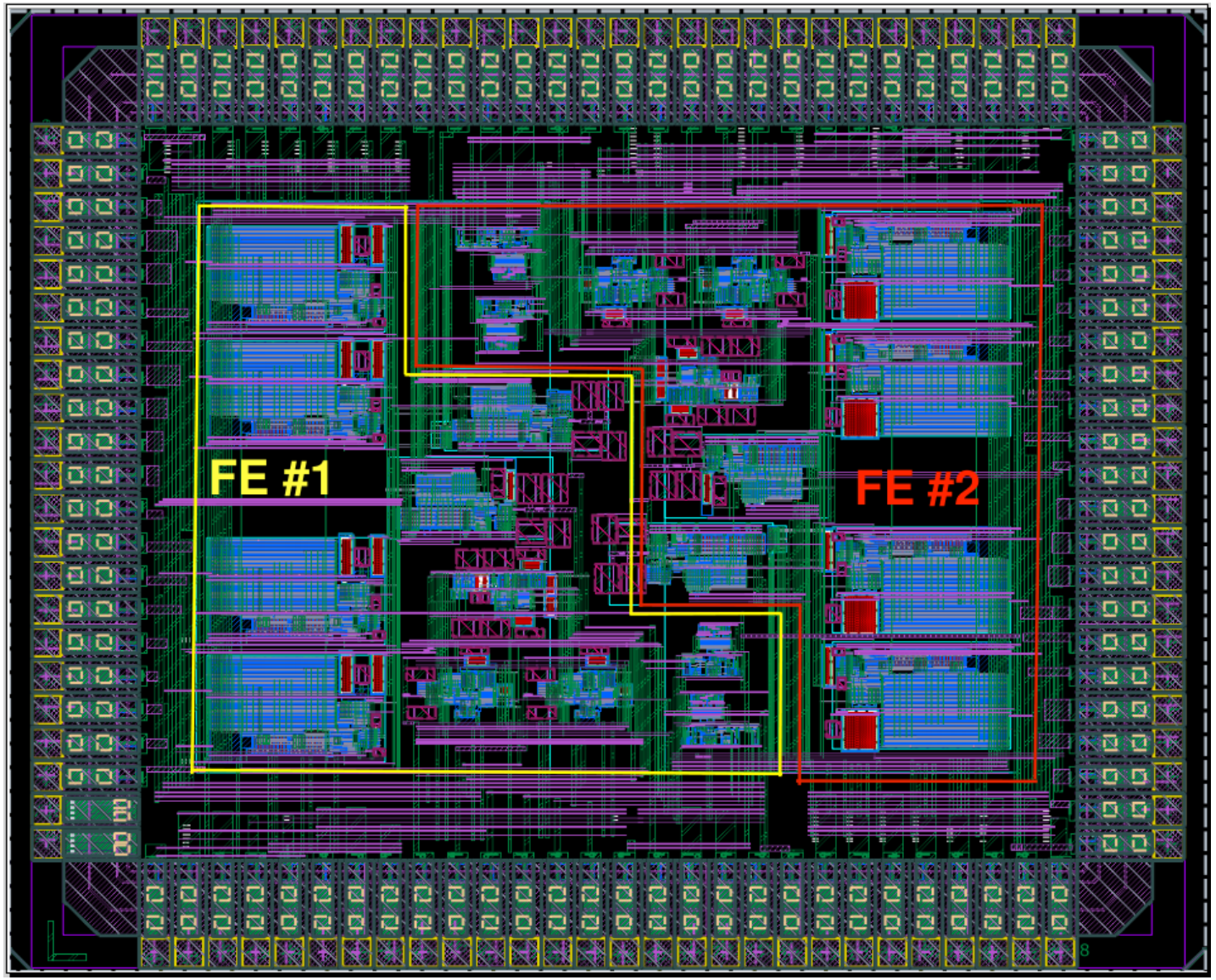
CAD Layout full chip

- Symmetrical 2 Front-end circuits



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DS20K_V3 Simulation Results

- Simulation were done considering a SiPM Triple Dose model and OV= 5 V.

Parameters	Front-End #1		Front-End #2	
	Single Ended	Differential	Single Ended	Differential
Vout (mV)	11.7	17.2	3.57	5.1
Vnoise (mV)	1.31	1.8	0.53	0.69
SNR	8.9	9.5	6.7	7.4
Jitter (ns)	13.5	17	8.7	13
t_{rise} (ns)	143	161	70.9	134
Power (mW)	100	140	100	140
Dynamic Range (pe)	100	90	310	305

LFoundry CMOS LF11is

CMOS structure characterization

- Parameter extraction activities towards the development of CMOS cryogenic models
- Behaviour of critical parameters of transistor at 300 K and 77 K.
- Gm/Id in weak inversion (left) and Threshold voltage variation (right)