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FOOT General Meeting, Rome - 05.12.19



## • Reminder of DAQ system

• Where we were

• What we've done so far

• What's missing

• Conclusions

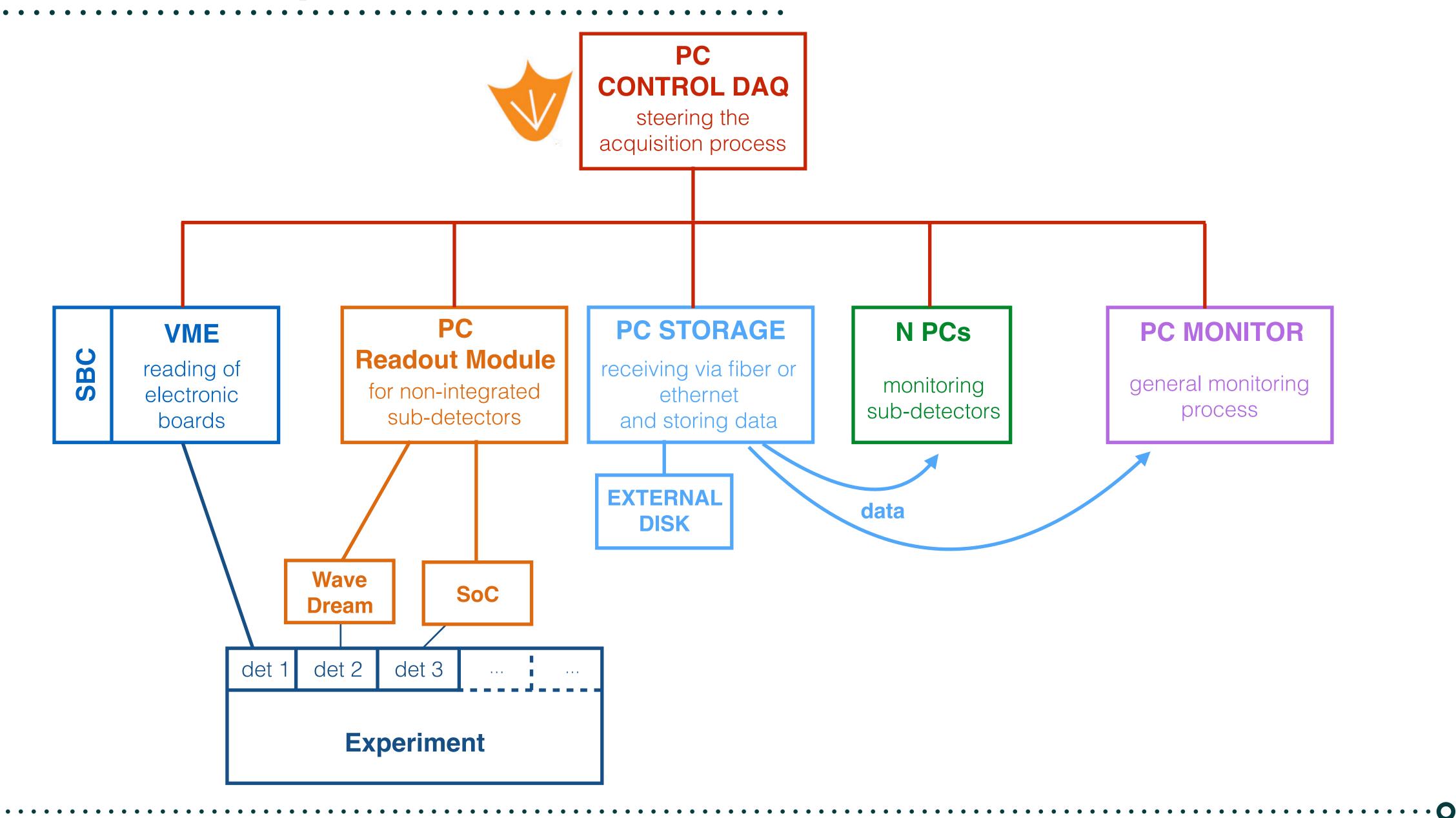




## **Reminder: DAQ system**

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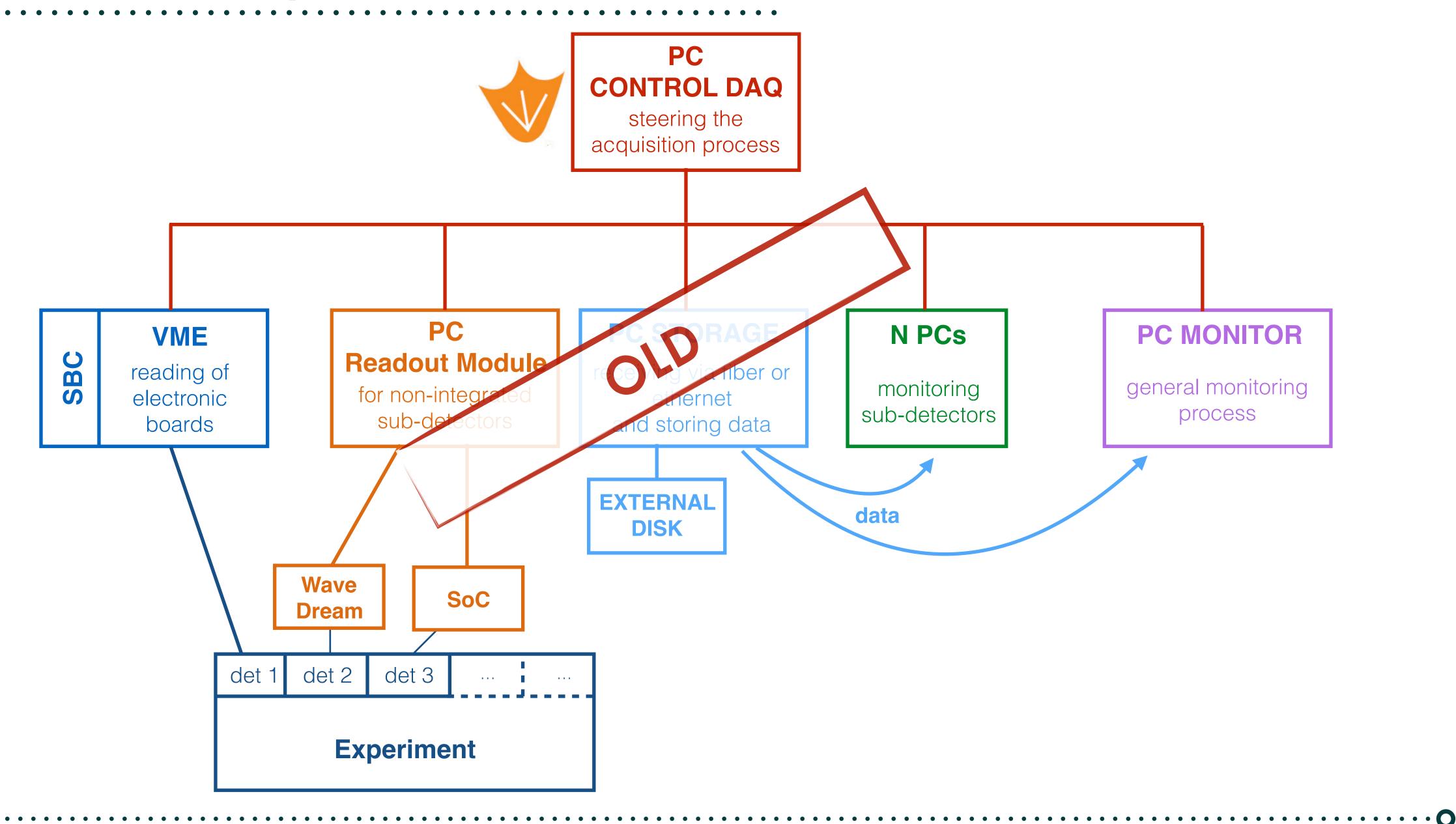




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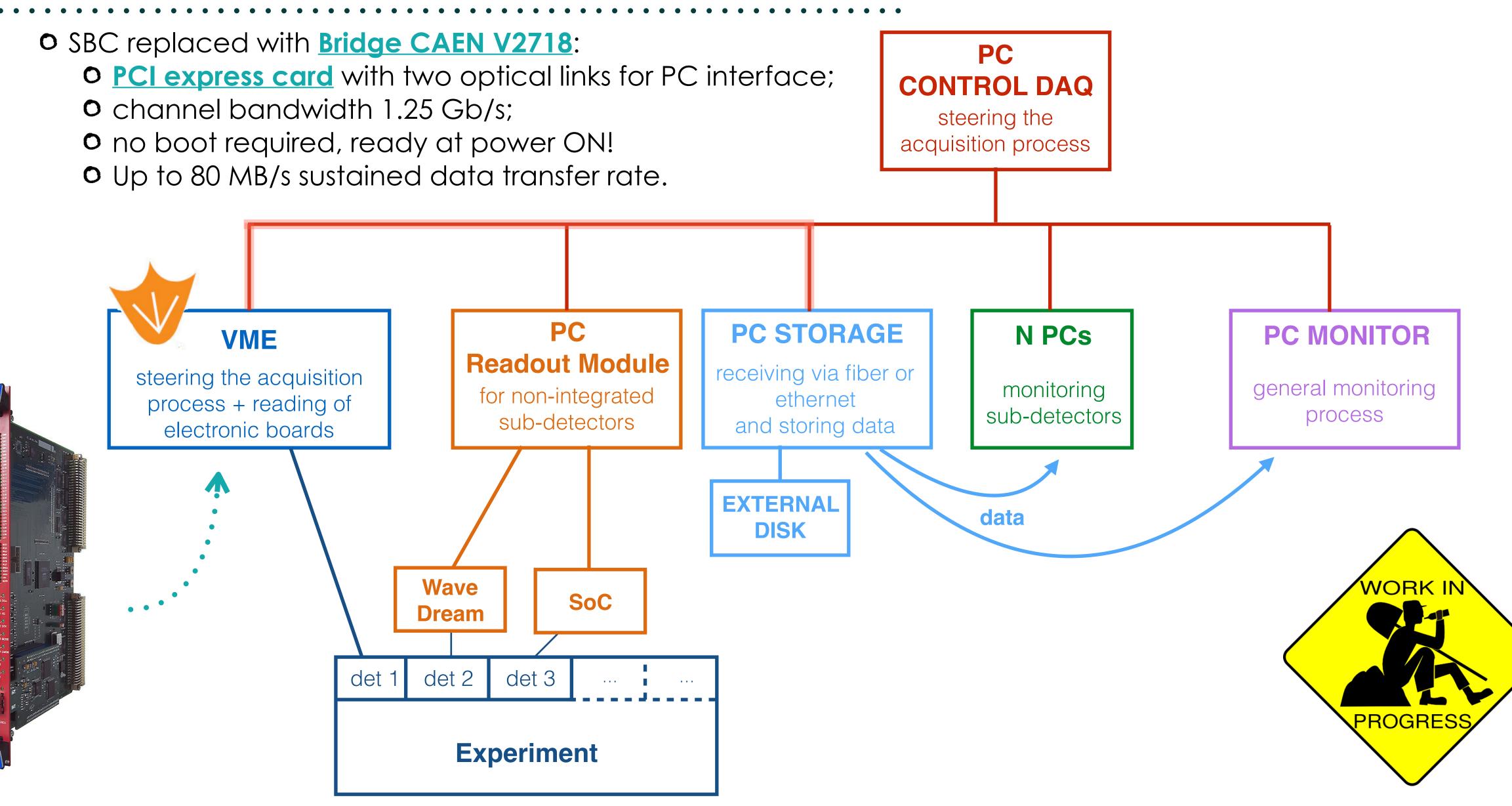
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## New DAQ structure



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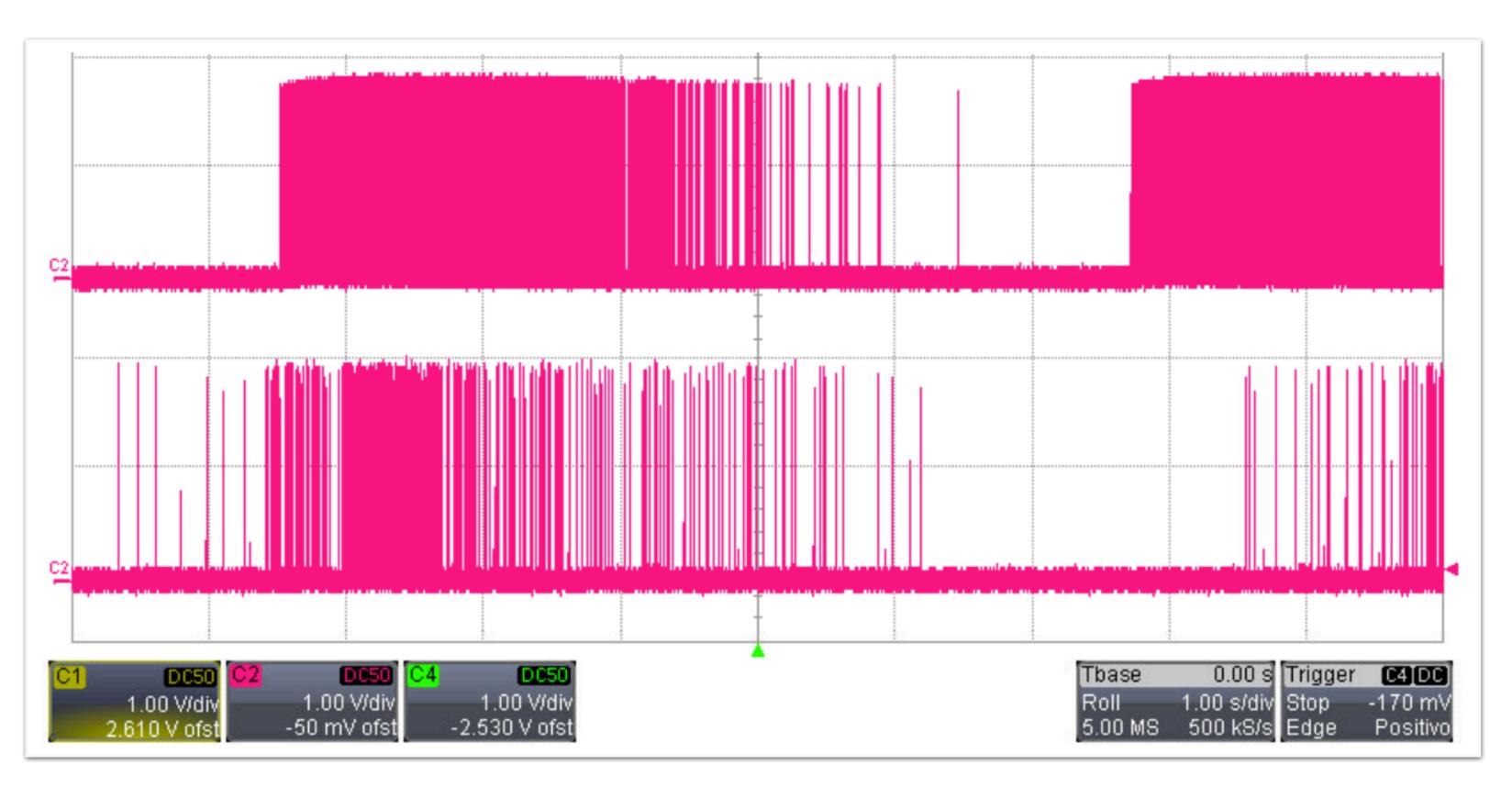




## **Beam simulator**

• Simulation of the beam we had at GSI; **O more realistic environment** for debugging systems integrations; O simulations are not enough.

• 6-8 s periods, varying intensity, random trigger.





## • VME boards only: no particular issues to run smoothly with DAQ;

## **O** Workplan:

- HV to be added in central DataBase;
- improve online monitoring;
- build a trigger system to reduce the  $T_0$  jitter (now ~10 ns); • need a discussion among DAQ, WD-DAQ and BM-DAQ.



### Event size: ~500 B/evt



## Wave Dream DAQ

• System in Bologna from June, for a long time • thanks to Pisa group's availability! :)

### • What we got:

- easier and more user-friendly trigger configuration;
- synchronisation of DAQ event segment and WD event segment;
- online event building still need some work, mainly by detector experts.

### **O** Workplan:

- improve online monitoring;
- test event building to check no event loss happens anymore; • decided to wait for the DataCollector board; • system to be re-tuned (with TCP/IP connection).
- more controls on threading;
- starting procedure needs to be automatic!



Event size: 29 kB/evt

8



## **VTX DAQ**

• GSI has been an extremely useful experience • more info about problems found in backup

• What we learned:

• not reliable event building without all the trigger/busy/time stamp signals connected • need to have an automatic start/stop procedure • need to have just one TCP/IP stream for VTX • need to have an improved online monitoring

• Plan to work on this with the system in Bologna, not yet happened **O Workplan:** 

• integration in Bologna, to be decided with interested people

• 2-day test beam with DAQ+VTX only?

- event building of 4 layers inside VTX system, with necessary synchronisation checks;

### Event size: 650 B/evt



• Plan to start the integration, not yet happened • general FPGA+CPU framework has been sent to Perugia people

• In principle it will be handled by the DAQ with the same approach as for the VTX

**O Workplan:** 

- need to start asap a joint DAQ-MSD HW tests • likely around January;
- in Bologna we have now 3 engineer students!



• DAQ system yet to be designed

O Main issue: data size

• plain FADC option: • 10/20 FPGA boards; • 320 channels x 1024 samples x 2 bytes = 640 kB  $\rightarrow$  640 MB/s at 1 kHz rate; • exceeding the max bandwidth of VME (~80 MB/s) and writing on SSD (~200 MB/s) • reduction of data size and bandwidth is mandatory • we assume an intermediate PC for this reduction (to 2/3 kB)

• Global DAQ will be tuned on these numbers



## Status of DAQ integration

Sub-detector	What we will use	What we need to work on	From which institute	What we have now
Start Counter	Wave Dream	PC interface	Roma+Pisa	working system*
<b>Beam Monitor</b>	TDC	parameters for board configuration	Milano+Roma	TDC (V1190B)*
Vertex	<b>DE10?</b>	software for TCP connection (CPU)	Frascati	DEO
IT	Achille Board ?	software for TCP connection (CPU)	Frascati	Achille board
Micro Strips	DE10?	software for board connection (CPU + FPGA)	Perugia	DEO
DE/TOF	Wave Dream	PC interface	Roma+Pisa	working system*
Calorimeter	?	strongly dependent on the type of chosen readout	Torino	

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### **O GNAM infrastructure**

need to add all the info from different detectors
 possibility to check directly comparisons between different systems

## Online Histograms infrastructure

o some already implemented
 o need a strong collaboration with detector experts to store useful info

• All this info can be used by shifters during data taking
• not to overload the DAQ shifters too much (from GSI experience)
• all detector expert should be "shifters" to check their own info

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## **Reminder: from our CDR**

from CDR	Detector	Board(s)	DAQ channels	max event rate (kHz)	Event size (bytes)
	Trigger	V2495	1	10	40 B
	Start Counter	DreamWave	4	1	8.2 kB
	Beam Monitor	$\mathrm{TDC}$	36	5	$0.1 \ \mathrm{kB}$
	Vertex detector	SoC on DEx	$4\cdot 10^6$	2	0.9 kB
	Inner tracker	SoC on DEx	$28\cdot 10^6$	2	2.1  kB
	Outer tracker	Custom	$6\cdot 10^3$	2	0.5  kB
	$\Delta E/\Delta x$	DreamWave	80	1	8.4 kB
	Calorimeter	QDC	400	2	1.7  kB
	Total DAQ	Storage PC	-	1	22 kB

• Numbers from GSI experience • DAQ (trigger+BM+file structure): 530 B O VTX: 650 B 29 kB • SC+TOFW:





## Conclusions

• Several problems have been observed at GSI • all of them could be observed only with <u>real detectors</u> (and with enough time!)

### **O WD system in Bologna**

• enough time to test solutions and alternatives;• still some work needed but in good shape.

### **O VTX system still as it was at GSI**

• some solutions have been drafted;

• tests foreseen with the detector experts.

### O Other systems (IT, MSD, Calo)

tests foreseen with detector experts, Calo when the readout will be defined;
need to define many technical points for all these systems;
integration will proceed as soon as they will be available

<sup>O</sup> we need to plan for a long integration phase well in advance ( $\geq$  5 months) wrt a test beam.

### • Works ongoing to finalise the DAQ structure (both HW and SW)

- online monitoring;
- reducing levels in DAQ structure;
- etc etc

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Supporting material



# DAQ-VTX interface problems - 1

- Integration done only at GSI not ideal...
- (about 2-3 ms) costing us a DAQ rate of 300 Hz
- BCO not forwarded to VTX - > problems in event building -> Timestamp candidates: framecounter (185 us period) internal clock value (0.5 us period)
- VTX is missing triggers (run dependent)

Busy signal from vertex missing; decided for a fixed busy lenght



# DAQ-VTX interface problems - 2

- Basically all variables that can be used for event building are NOT reliable:
  - HW triggers restarts after the first 100-200 event (approx) 11 s VTX black-out)
  - Sequential events with the same frame counter value have been observed
  - Clearly wrong frame counter values

  - Out of sequence internal clock values and/or frame counters Buggy HW trigger counters (rare)
  - Wrong event-internal clock value association (constantly off) by 1 event)



# DAQ-VTX interface problems - 3

- Observed VTX freezing:
  - About 11 s long, always after 100-250 events from the start, consistently on all runs and implying an hw trigger reset Can happen also during runs and without hw trigger reset
  - (e.g.: run 2212, VTX evts 39450-39451 matched with 40975 and 41248, 930 ms apart)
- Observed internal VTX time misalignment:
  - The 4 sensors are read out independently and shipped out via 4 UDP connections independently. The time alignment usually lasts till the first hw reset (i.e. on the first 100-250 events where most of the VTX tracks are found)
    - Exception: run 2211 where VTX detectors keep the time alignment after the hw reset for a total of 18641 events (out of 61322 in total)
  - Needed: internal VTX re-building for GSI runs; Monitoring for next data taking!



# DAQ-WD interface problems - 1

 BCO start, timestamp start (used for event synchronization);

WD starts early;

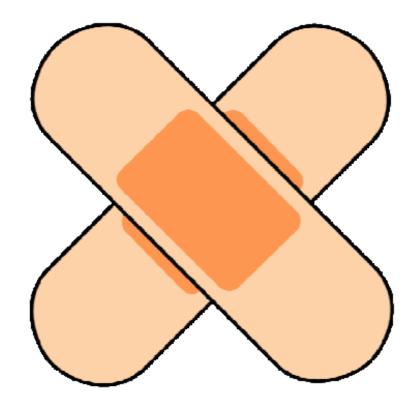
TDAQ sends two BCOResets: WD uses the first, trigger module uses the second (BTW: too few bits in the BCO#)

• Trigger start;

(between the first and the second BCOReset)

- Cured with changes in the V2495 firmware

- WD provides first triggers before the actual run start





# DAQ-WD interface problems - 2

- WD event losses
  - Examples from run 2212 116 k events for dag:
    - WD evt 0 not matchable
    - WD evt 1-12350 matched with dag 0-12349
    - written out (hw trig # jumps)
    - more events)
  - some point

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    From WD evt 12350-41367 one every three WD events is not
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    No more data after WD evt 41367, hw trig 51948 (dag has 64k)
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- Same pattern in other runs: ONE unmatchable event at the beginning, ~10k perfect, then 1 over three lost, stop recording at

