

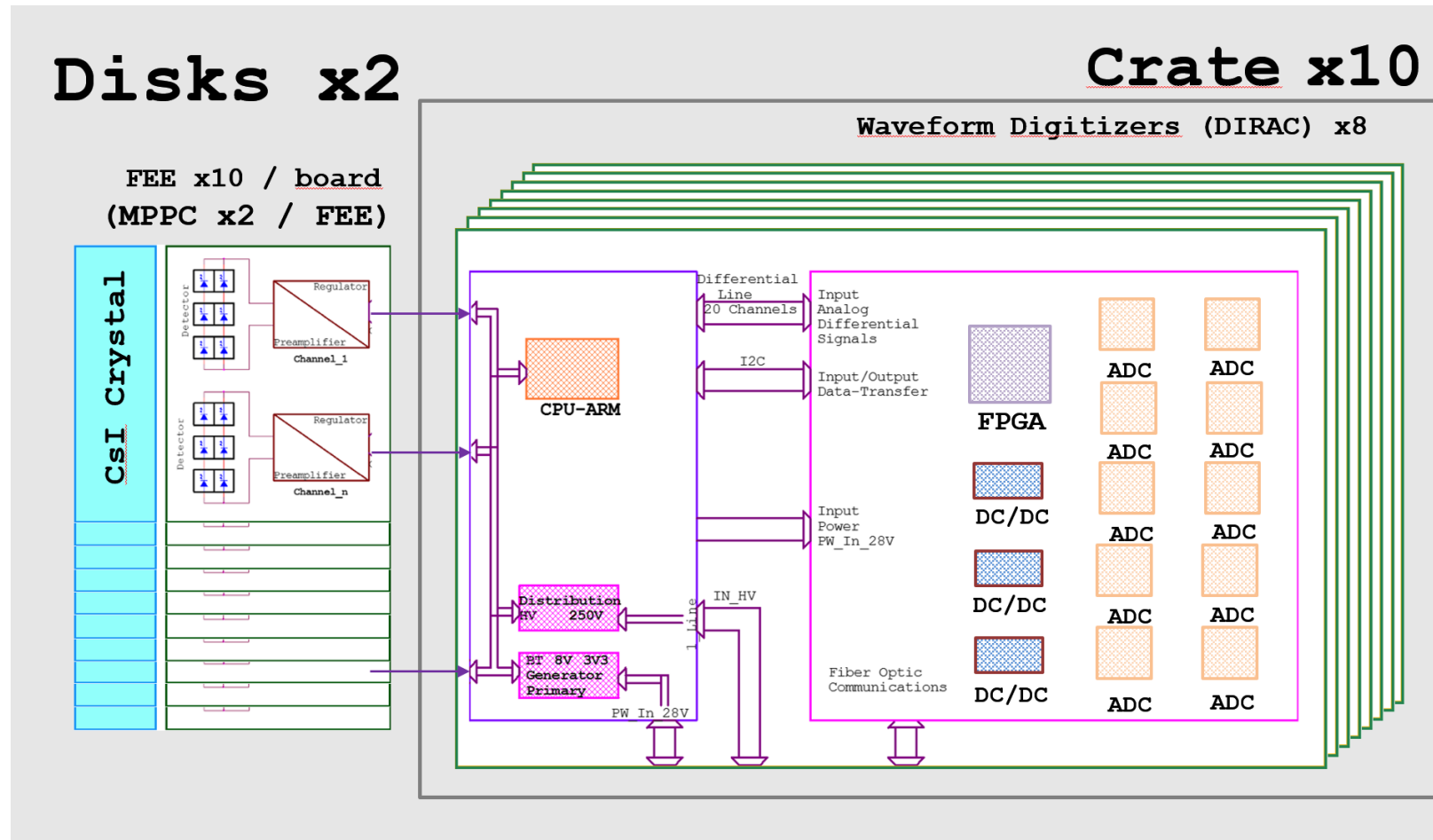
Status of DIRAC

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Luca Morescalchi

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Schema del DAQ



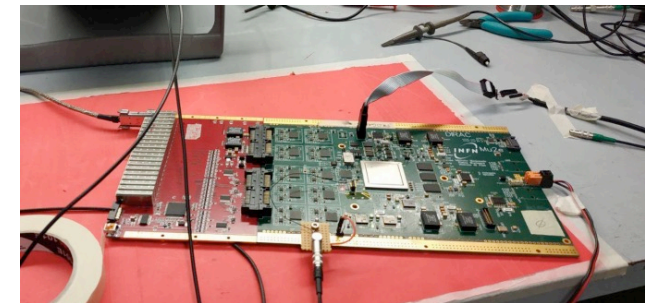
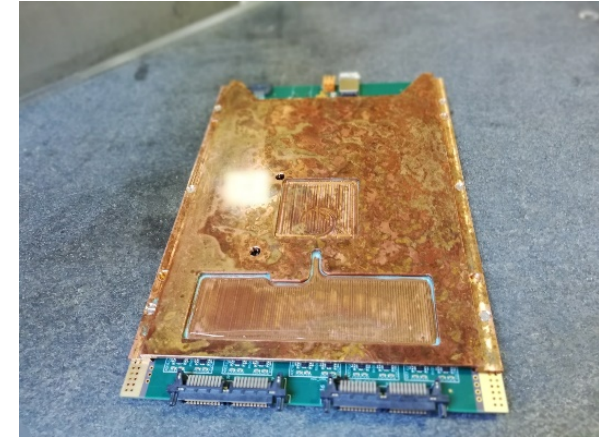
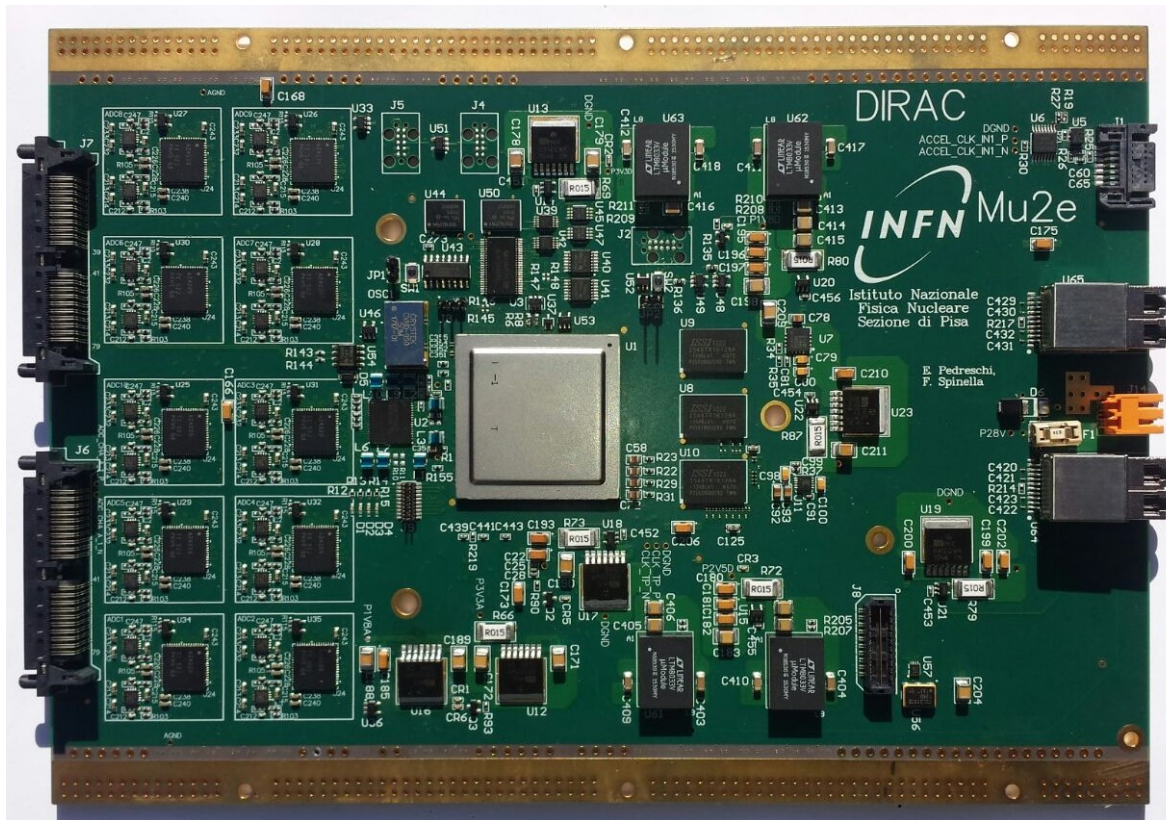
DIRAC spec ...

- DIRAC goal → Sample the SiPM signal (after FEE):
 - to achieve a **good energy resolution** O(7-10%)
 - **optimal time resolution** O(200 ps)
- Each crystal is readout through 2 SiPM → ≈ **2800 digitized channels**
- Limit the number of pass through connectors DIRAC is located inside the cryostat

This translates to the following requirements:

- Sample the signal with an **ADC with 200 Msamples - 12 bit**
- Harsh Environment → severe limitations on the components choice:
 - **Stand a radiation environment of 5×10^{10} n/cm² @ 1 MeV_{eq} (Si)/y and 12 Krad of TID (Total Ionizing Dose)/y = 12 Krad test level.**
 - **Work in presence of high magnetic field ($B= 1T$)**
 - **10^{-4} Torr vacuum → Low power**
- Have large reliability to allow to operate for 1 year w.o. interruption

DIRAC V1



Sotto test dal 2018, testata x dose, n, B, in vuoto, termica
Full chain slice test con modulo 0 e «single crystal»
Goal: validare parte analogica e la catena di amplificazione

DIRAC V2

DIRAC V1 funziona bene, ma e' da tempo prevista una V2 (identica nella parte analogica, molto diversa nella parte digitale)

- **Cambiamenti dovuti alla resistenza alla radiazione:**
 - FPGA: Microsemi Polarfire (al posto di SM2)
 - Scelto modello 300 (al posto del 500) molto piu' economico
 - CERN VTRX (optical TRX Cotsworks in V1 muore a qualche Krad)
 - DCDC converters (scelta sofferatissima ...)
- **Cambiamenti dovuti alla variazione delle specifiche:**
 - Catena di clock (adesso encoded nei dati)
 - Readout point-to-point (un solo driver ottico)
 - CAN BUS come canale dati secondario
 - DDR3 piu' grande
- **Cambiamenti dovuti ai cambiamenti:**
 - Molti drivers, convertitori di livello, simple logic, ... dovuti al fatto che Polarfire e' molto diversa da smart fusion 2

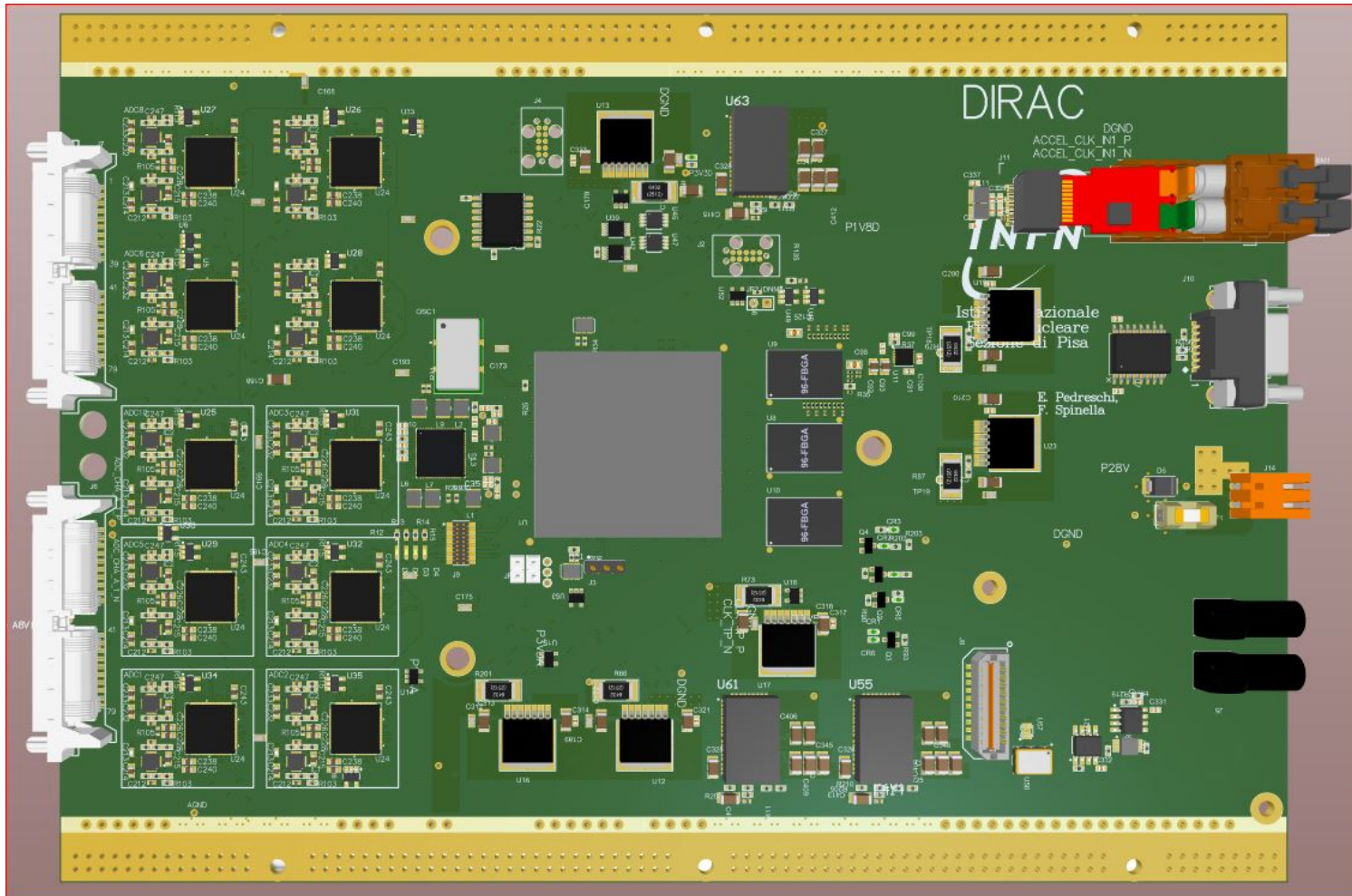
- **Fatti molti test di dose, neutroni, vuoto al livello del singolo componente prima di validare il progetto V2**

- **Test single channel compatibilita' PF vs ADC (ADS4229)**

- **Firmware PF tutto scritto per valutare 300 vs 500 e performance**

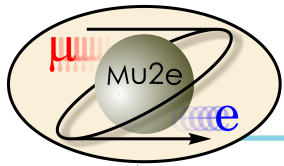
DIRAC V2

DIRAC V2 in costruzione (5 prototipi), attesa per prima meta' di ottobre

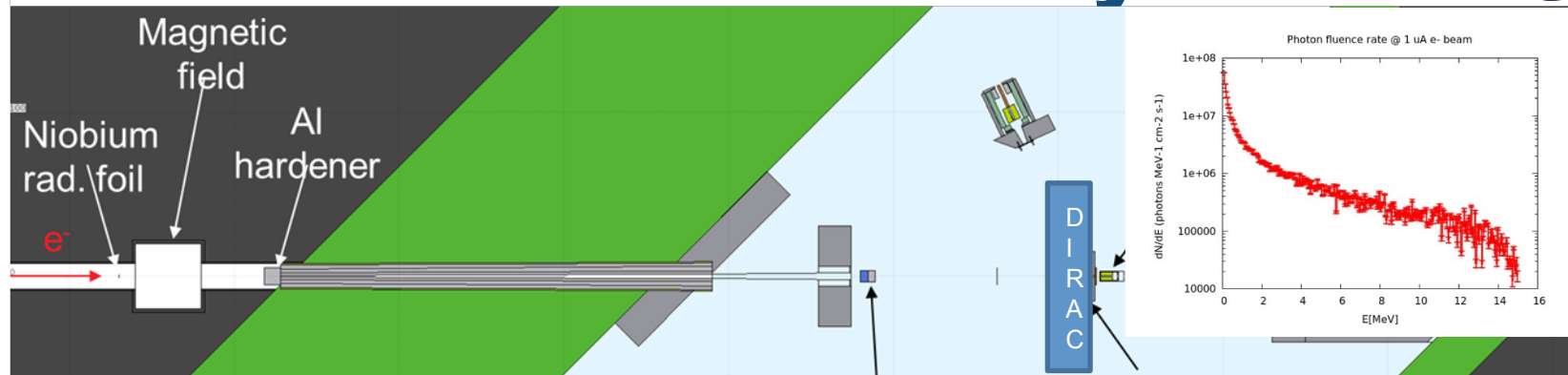


Test di qualifica (v1 & v2)

- Several test campaigns were performed in 2018-2019:
 - Total Ionizing Dose (TID):
 - ✓ **gELBE@HZDR** γ from Bremsstrahlung ($0 < E < 14 \text{ MeV}$) Jun 2018, May 2019
 - ✓ **Calliope@ENEA** (Co60 source) Jun 2018, Oct 2018, Jan 2019, Apr 2019
 - Magnetic Field (B):
 - ✓ **LASA@INFN** Milano (1T) Dec 2018, Feb 2019
 - Neutrons:
 - ✓ **gELBE@HZDR** ($1.06 \times 10^{12} \text{ n/cm}^2$) Mar 2019
 - ✓ **ENEA** ($6 \times 10^{11} \text{ n/cm}^2$) Apr 2019

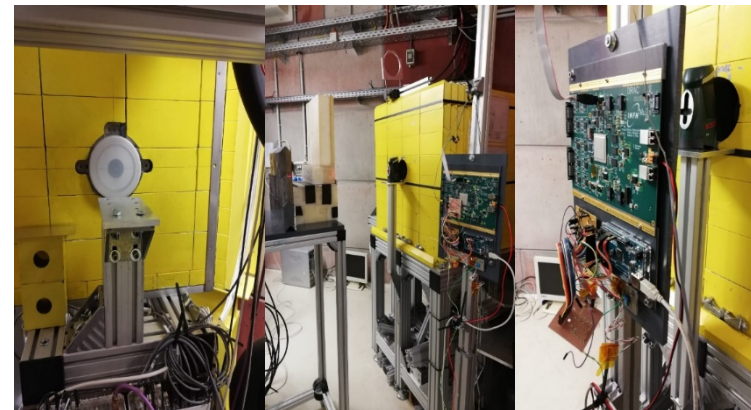


YELBE facility

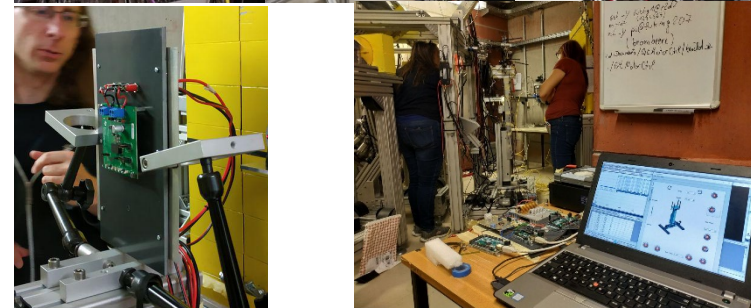


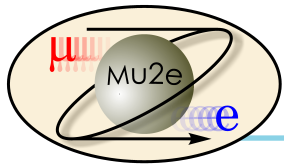
- Photons is produced per Bremsstrahlung by the electron beam hitting a niobium foil in the accelerator hall
- Nominal beam conditions:
17 MeV electrons, 600uA, 12.4 um niobium radiator foil
- Simulated **dose rate** $\approx 18.6 \text{ krad/h}$
- Active dosimetry used to confirm simulated dose rate

V
1



V
2

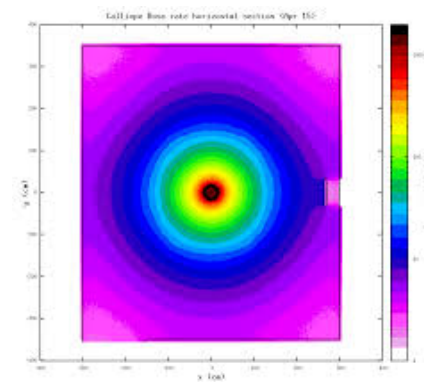


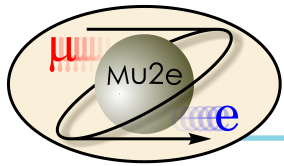


Calliope facility



- Gamma rays at 1.17 and 1.33 MeV from **Co60**.
- 3.7×10^{15} Bq of activity.
- **Isotropic source**, flux scales with r^2

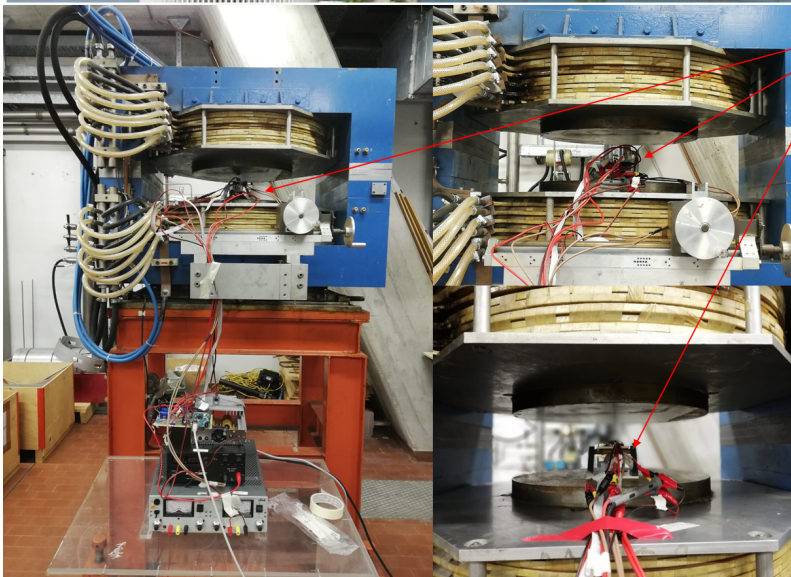




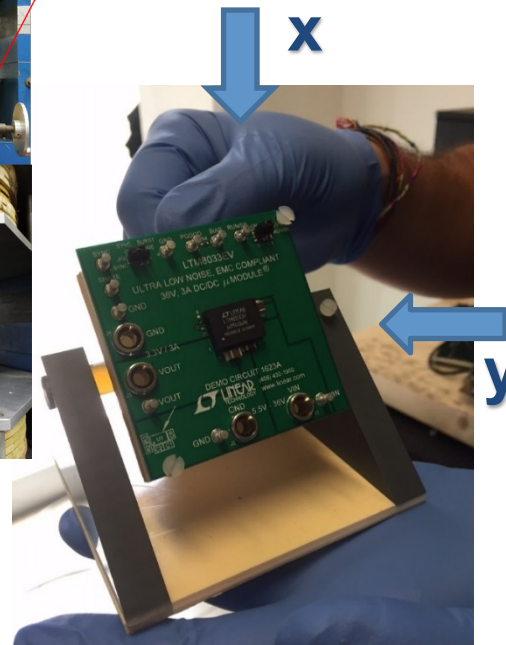
LASA facility



Laboratorio Acceleratori e Superconduttività Applicata

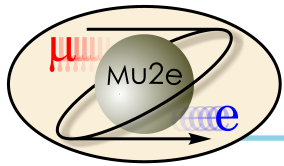


DCDC DEMO BOARD



- **Uniform magnetic field up to 1.2 T**
- We tested different orientations of the DCDC with respect to the magnetic field
- Same setup of the radiation tests



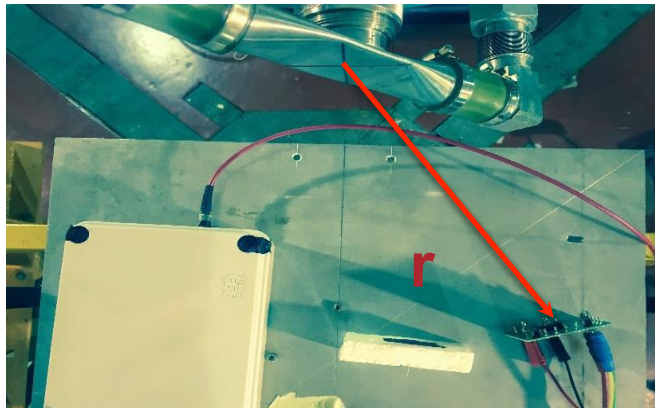


FNG facility



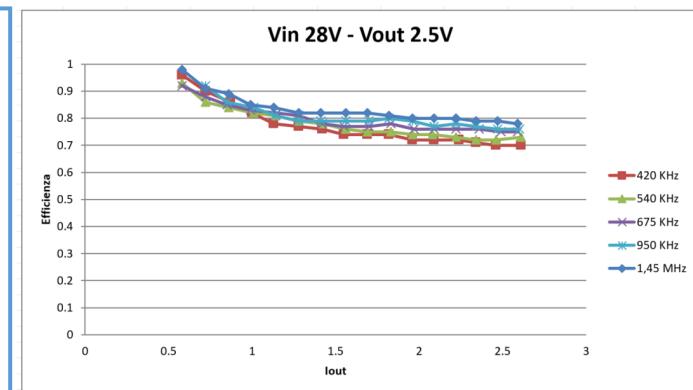
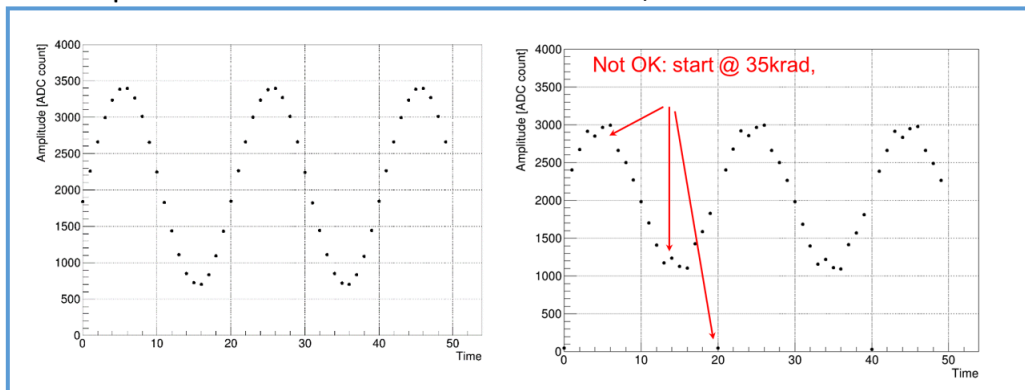
Frascati Neutron Generator (FNG) is a linear electrostatic accelerator in which up to 1 mA D⁺ ions are accelerated onto a Tritium target

- **Up to 10^{11} 14 MeV neutrons/s**
- almost *isotropic source*, flux scales with r^2
- calibrated at 3% level using alpha particles



Risultati qualifica DIRAC V1 (condensati)

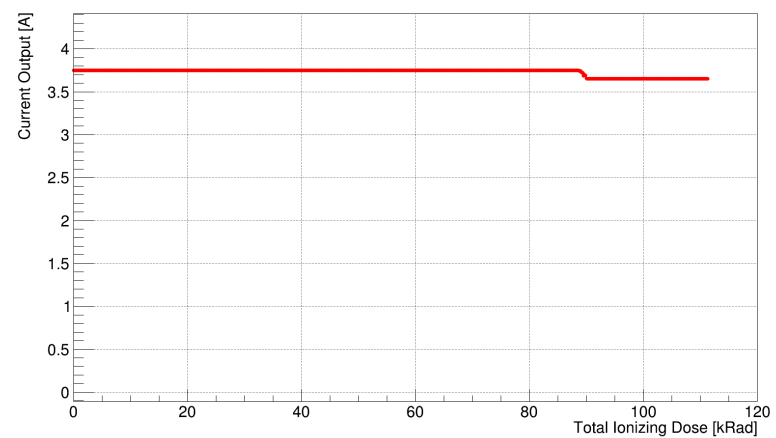
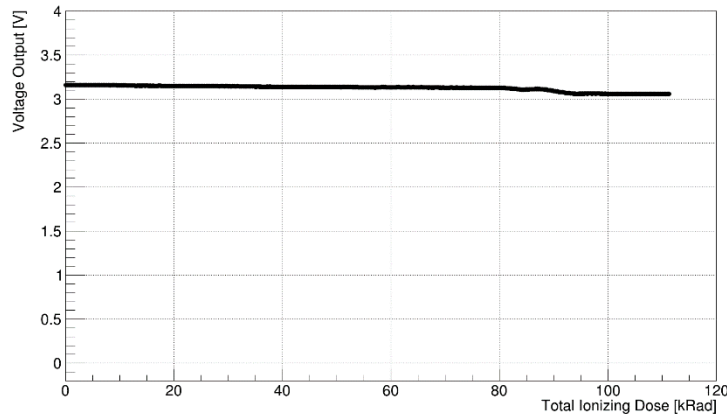
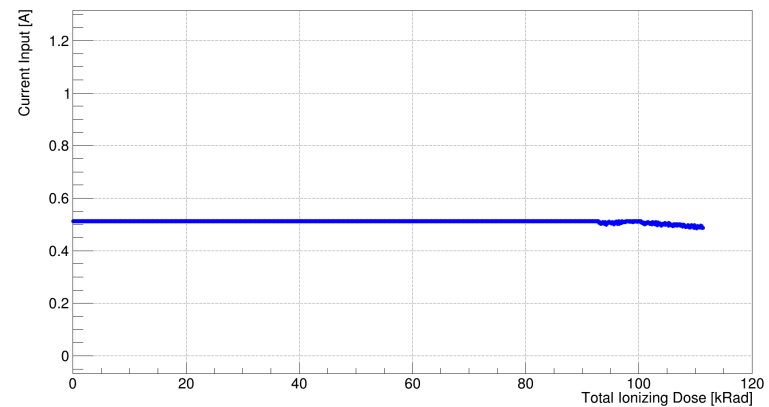
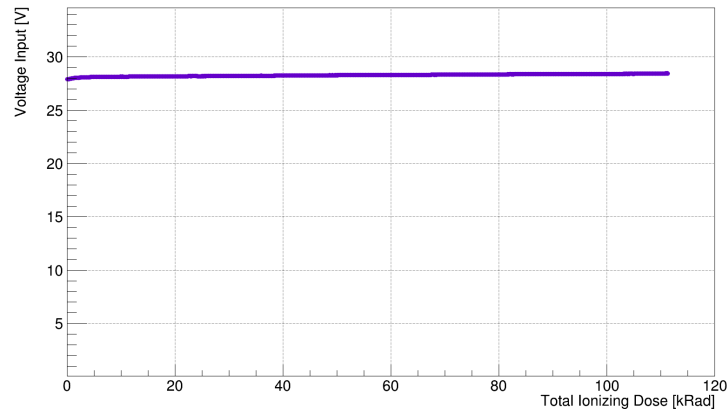
- Dirac V1 qualificata fino a 30 Krad, ma DCDC hanno Vout che cresce linearmente (10 % a 30 Krad), FPGA non riprogrammabile dopo pochi Krad, ritardi interni peggiorati
- Nessun degrado sui componenti analogici o mixed (ADC)
- Effetto neutroni trascurabile
- Efficienza DCDC peggiora parecchio in B
- Test termici (Pisa) OK, test vuoto (LNF) OK



Risultati qualifica componenti V2 (condensati) 1/2

- Il componente piu' critico e' il DCDC converter.
- Deve resistere a TID (Vout stabile) , n, rimanere efficiente in B = 1T
- Testati LTM8033,LTM8053, LMZ31710,**LMZM33606**
- LMZM33606 e' risultato qualificato (testato 3 volte per TID, 2 per neutroni, 1 per B=1T)

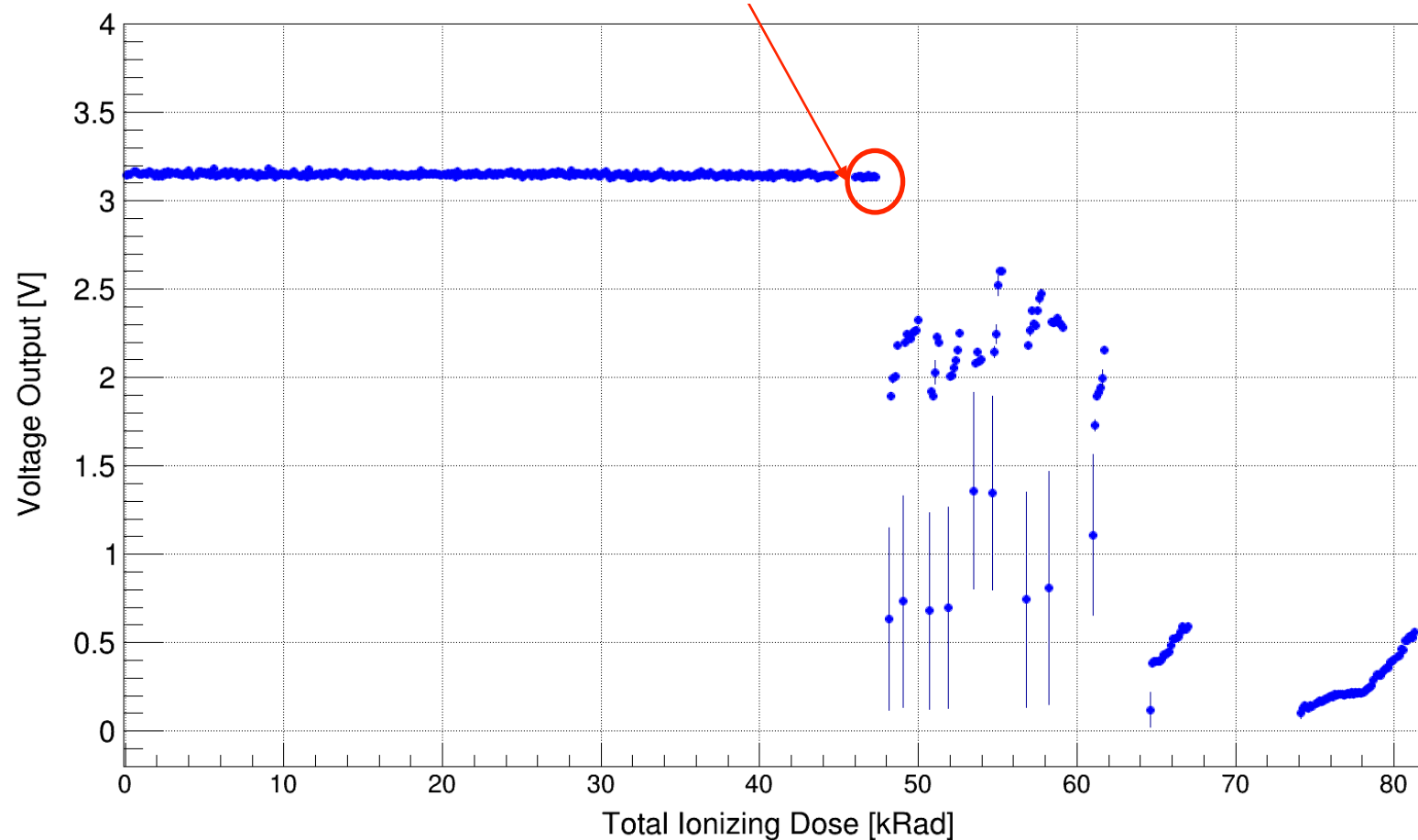
DCDC Radiation test 4 feb 2019



- Ok up to 80Krad, then small drop in V_{out} , $Eff = 85\%$
- **48 Krad in the following 2 tests ... qualification level 12Krad**

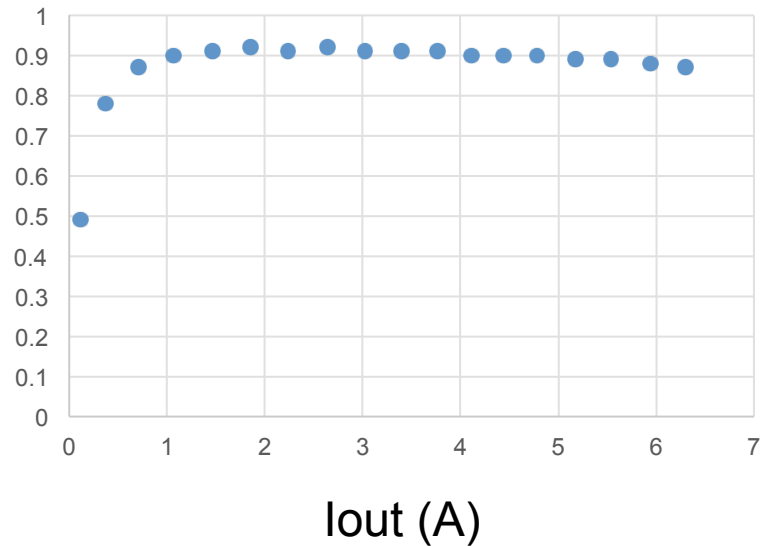
LMZM33606 TID @HZDR: test results

LMZM33606 works fine up to 48 krad

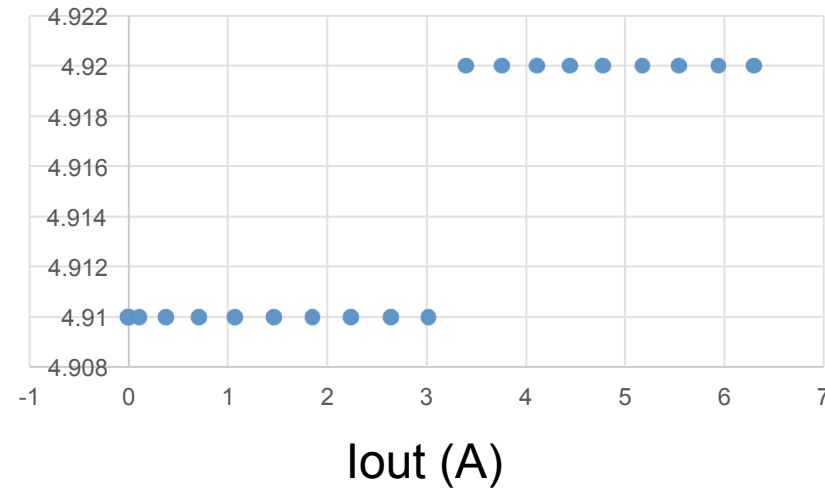


LMZM 33606 B field test results LASA 20 Feb

Eff vs Iout



Vout vs Iout



- Test OK: no evidence of drop of performance in B=1T
- Same results for many Vout (1.8,2.5,3.3,5) and all views (X,Y,Z)

Risultati qualifica componenti V2 (condensati) 2/2

- Alcuni nuovi componenti sono stati testati dal gruppo di FNAL (Polarfire, LDO, VTRX)
- Altri sono stati testati da noi a GELBE (HZRD) : CAN RXTX, translator di livello, ...

Tutti i componenti «nuovi» della V2 sono stati qualificati per TID, DCDC per n e B

Firmware V2

- Polarfire completamente diversa da SM2.
- Modello 300 o 500 ? Pin sufficienti ? Logica ?
- Performance sufficienti per supportare 20 ADC 200MHz DDR (400 MHz) ?

- Necessario scrivere il firmware VHDL ~ completo
- Necessario testare una versione del firmware «single ADC» su una demo board Polarfire + demo board ADS4229 (ADC)

DIRAC V2: firmware completo

The screenshot displays the I/O Editor interface for a CortexM1 subsystem. The top window shows a table of port configurations, including GPIO_OUT, NTRST, REF_CLK_0, RESETN, SCL0, RX, SCL1, SDA0, SDA1, SPISCKO, SPISCKO_0, SPISCKO_1, SPISDI, SPISDI_0, SPISDI_1, SPISDO, SPISDO_0, SPISDO_1, SPISDO_2, SPISDO_3, SPISDO_4, SPISDO_5, SPISDO_6, SPISDO_7, SPISDO_8, SPISDO_9, SPISDO_10, SPISDO_11, SPISDO_12, SPISDO_13, SPISDO_14, SPISDO_15, SPISDO_16, SPISDO_17, SPISDO_18, SPISDO_19, SPISDO_20, SPISDO_21, SPISDO_22, SPISDO_23, SPISDO_24, and SPISDO_25.

The bottom window shows the synthesis progress, with a list of tools and their status. The synthesis process is currently in the 'Synthesize' phase.

The right window shows the resource usage table:

Type	Used	Total	Percentage
4LUT	30514	299544	10.19
DFF	20483	299544	6.84
I/O Register	0	510	0.00
Logic Element	32192	299544	10.75

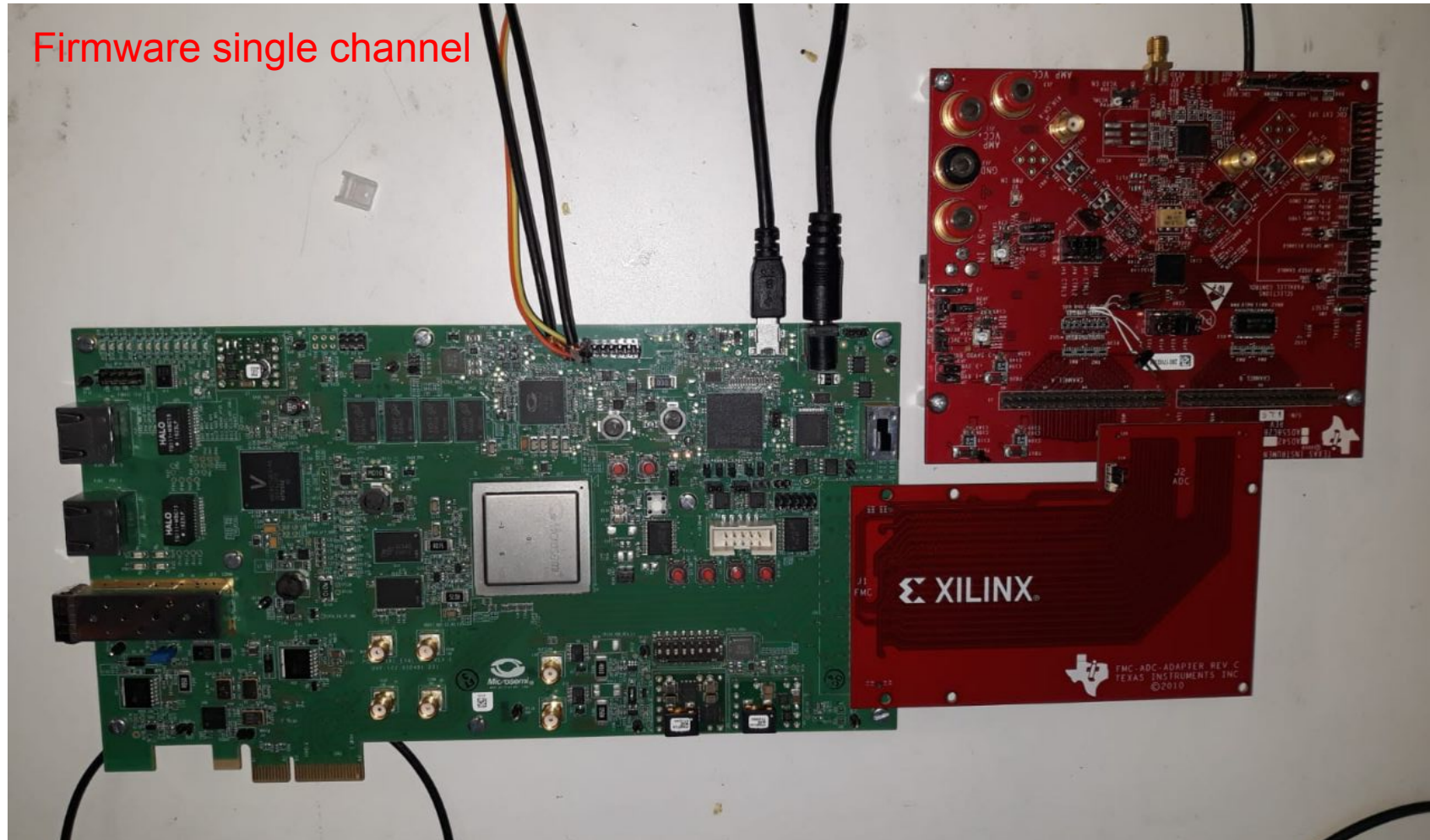
The bottom right window shows the synthesis log, which includes the following message:

```

Found inferred clock CORECORTXM1_ZS|JDRCK with period 10.00ns. Please declare a user defined clock on net CORECORTXM1_ZS|JDRCK.

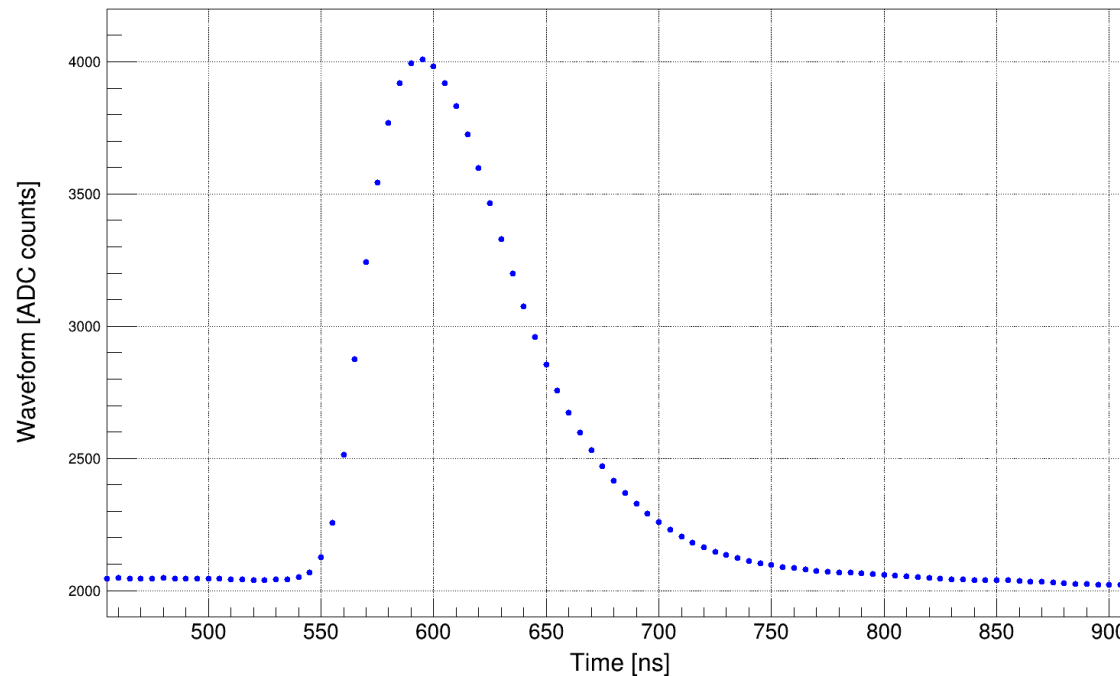
```

Polarfire + ADS4229 Demo board



Polarfire + ADS4229 Test @ Pisa

- First interface between Evaluation Boards of FPGA Polarfire and ADC
- We tested the system with a signal generator
- Full speed ADC readout



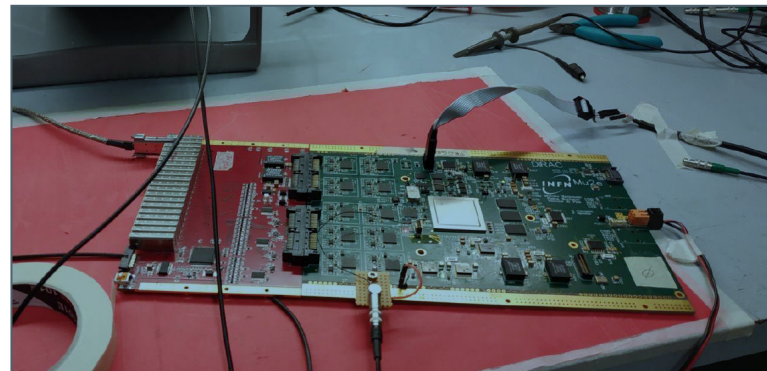
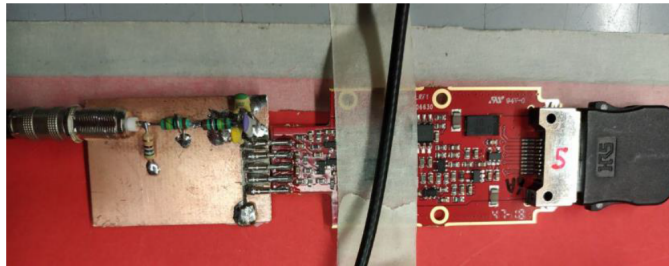
Test full chain v1 (vertical slice test)

- Validare il sistema (cristallo + sipm + fee + mezzanino + dirac) su segnali fisici
 - Validare parte analogica della DIRAC (non cambia in V2) in termini di dinamica, S/N, banda analogica, linearita', ...
 - Richiesta una dinamica di 150 MeV, zero suppression su soglia di 1 MeV
-
- 1) Test linearita' a banco (LNF)
 - 2) Test su modulo 0 a LNF, 20 canali (16 ...)
 - 3) Test «single channel» a Pisa con cristallo finale, cosmici + Co60 source

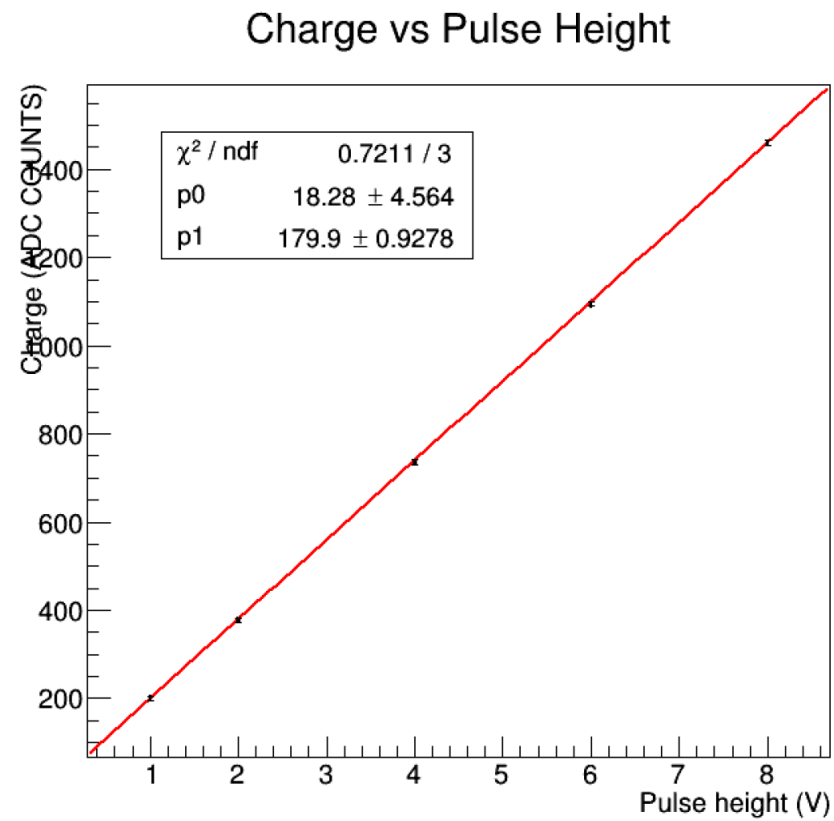
Test linearita' a banco 1/2

DIRAC + MEZZANINO + FEE + Charge injector

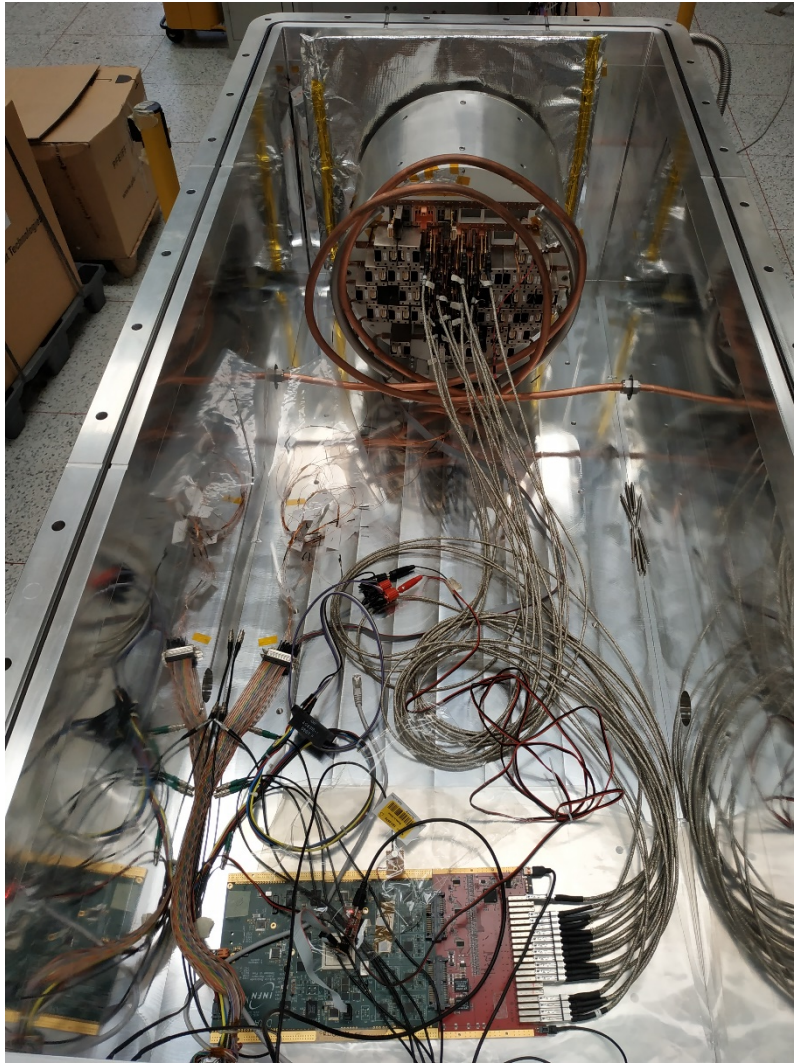
- The first week of May we joined Frascati group @ LNF to perform a first test of the full electronics chain
- Main goal: validate the analogic part of the Dirac in view of the production of the V2
- Resulting bandwidth and signal shape are as expected from simulations!
- First test of linearity performed by injecting charge in the FEE with a custom circuit



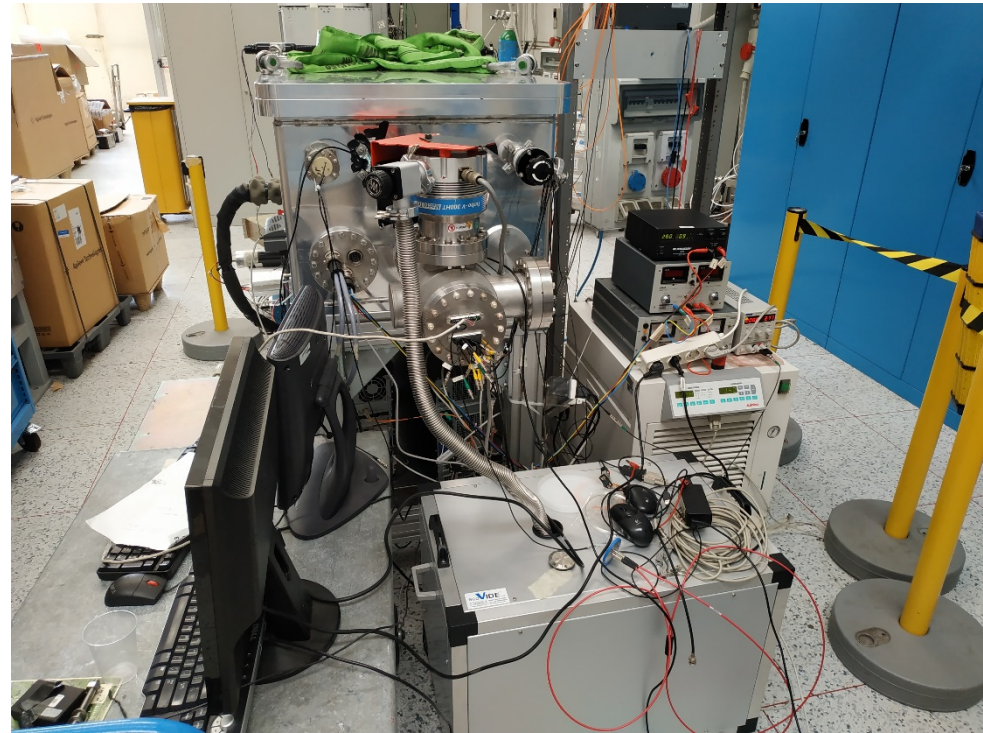
Test linearita' a banco 2/2



Slice Test @ LNF, Module-0, May/June 2019

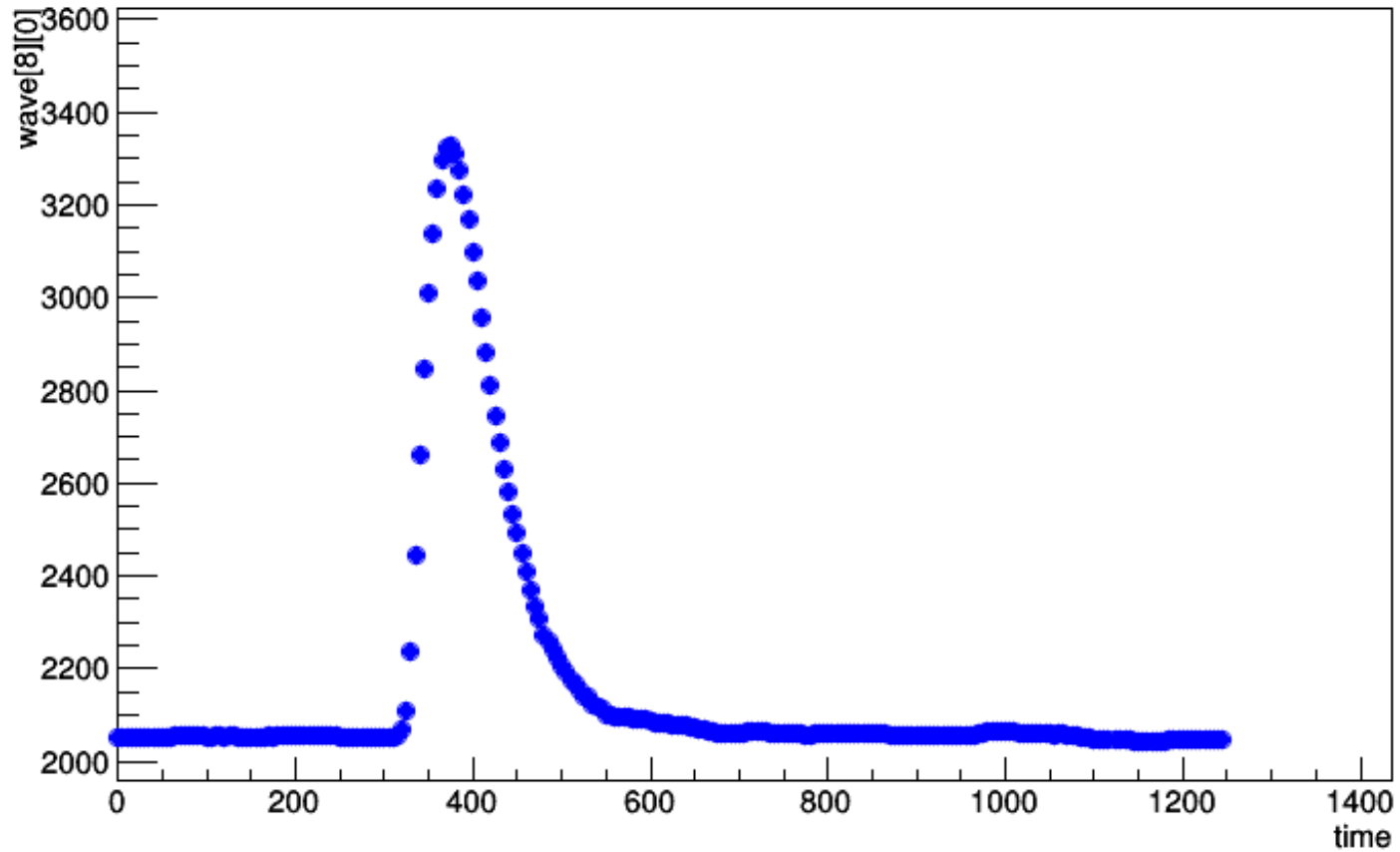


- We connected for the first time the DIRAC board + Mezzanine to 16 channels of the Module 0
- Module 0 equipped with FEE V3
- SiPMs cooled at 18 C degrees

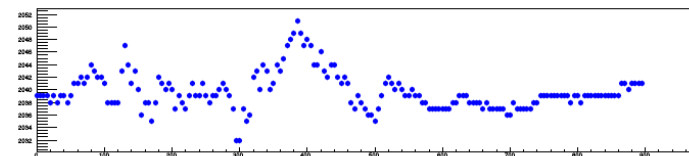
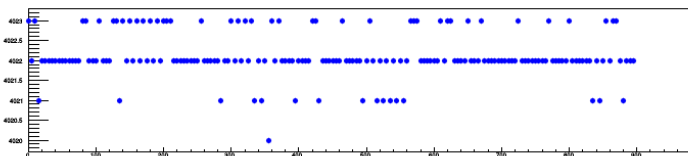
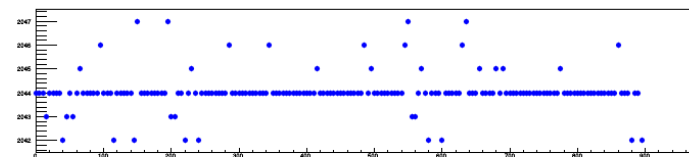
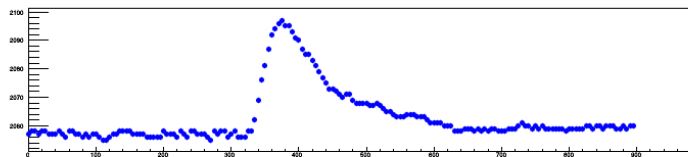
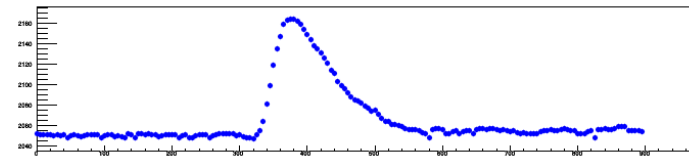
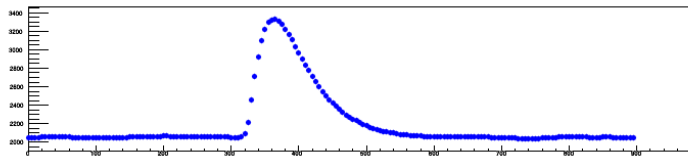
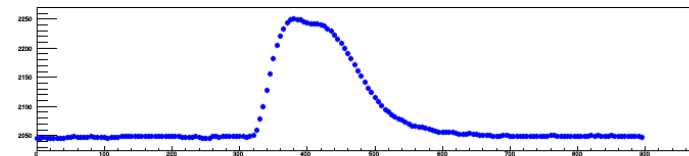
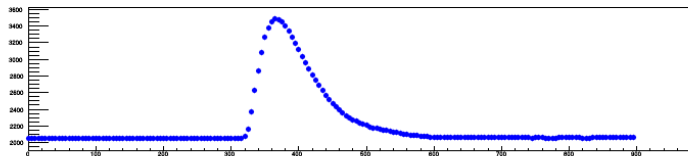
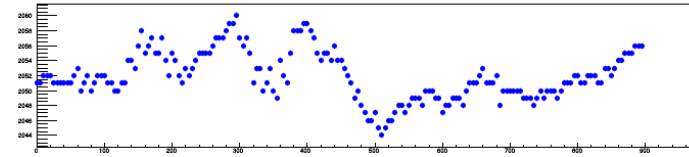
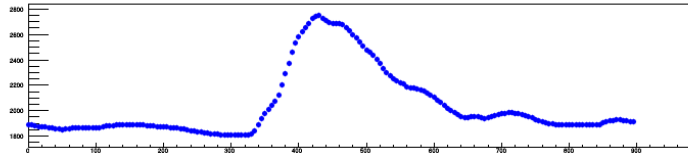


Waveform Example

wave[8][0]:time {nevt == 3268}

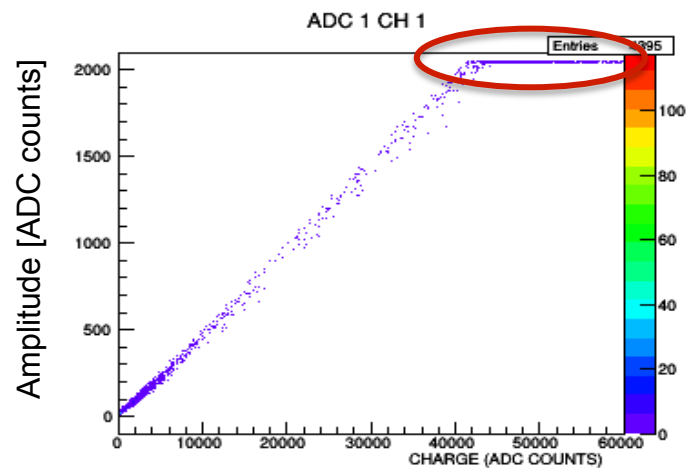


Example of Random Event

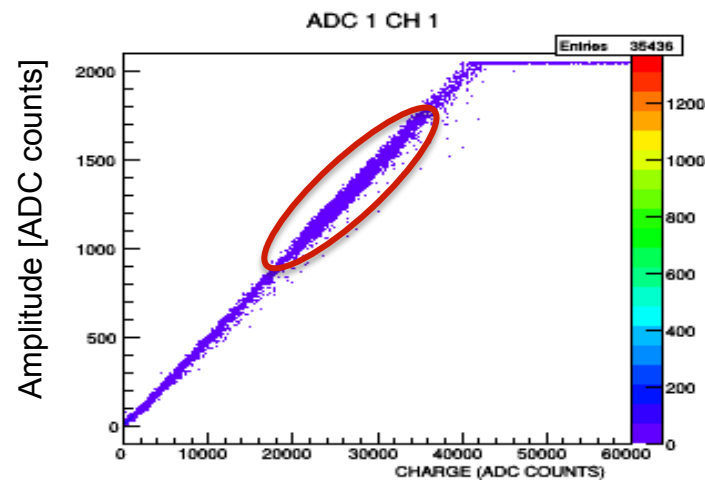


Dynamic Scale Check

- Trigger with the coincidence of 2 plastic scintillators out of the vessel
- At the operational voltage for the SiPMs we found that most of the cosmic rays saturated..
- We choose to run 3 V lower V_{op} ..



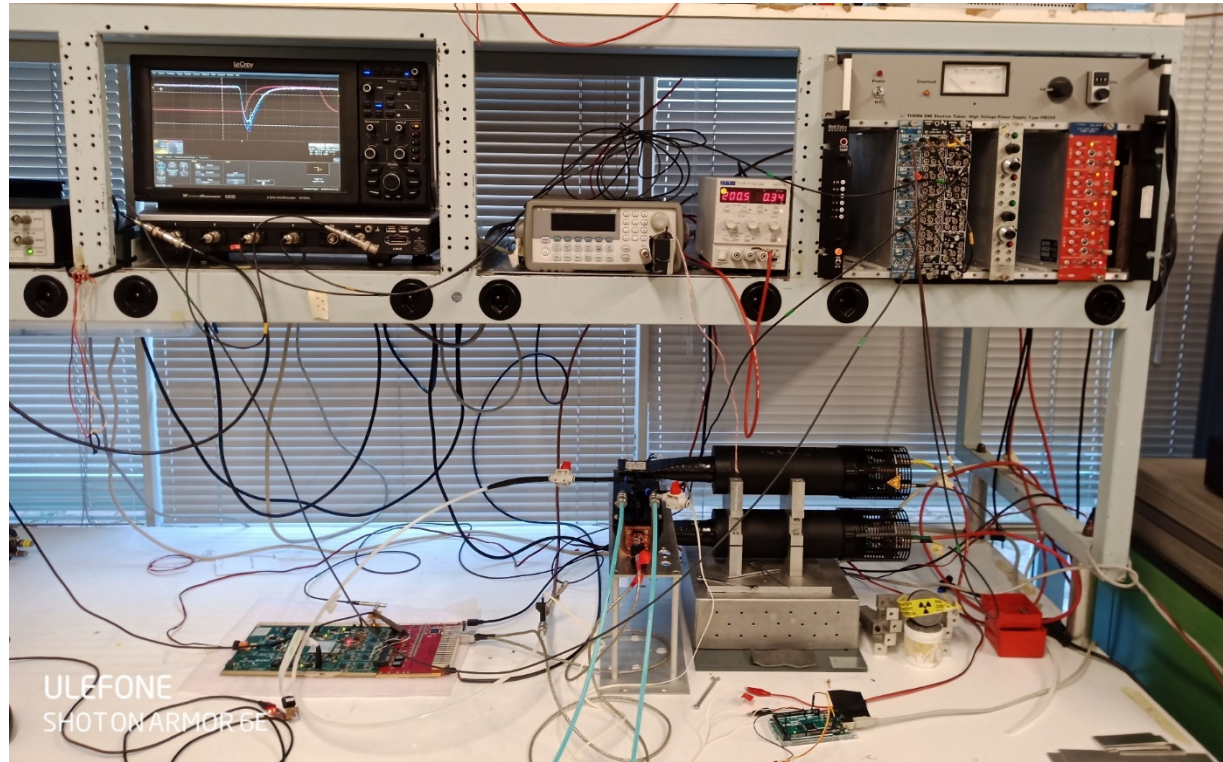
Operational Voltage



$V_{op} - 3 V$

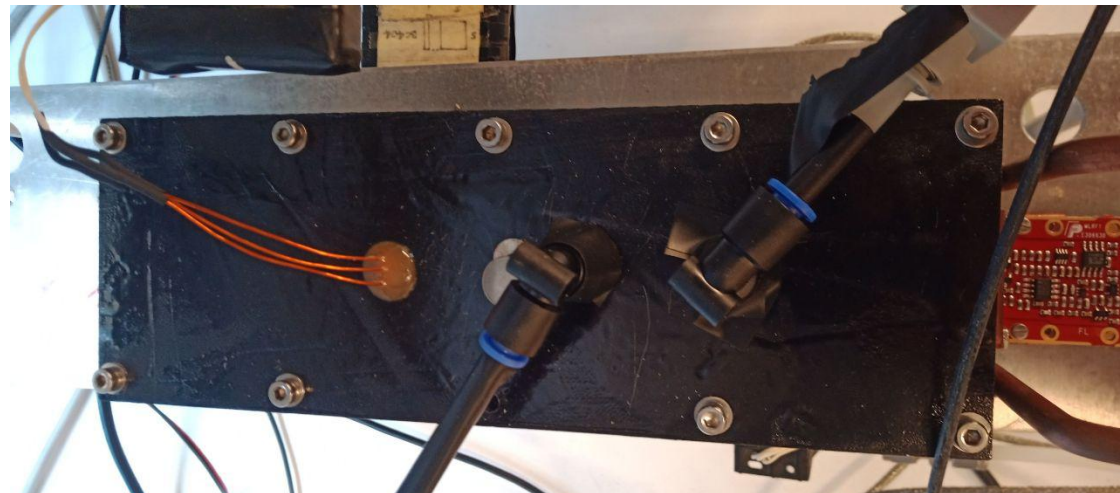
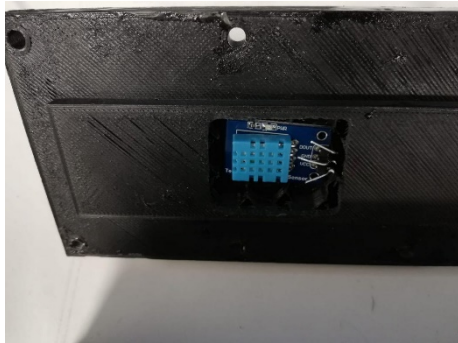
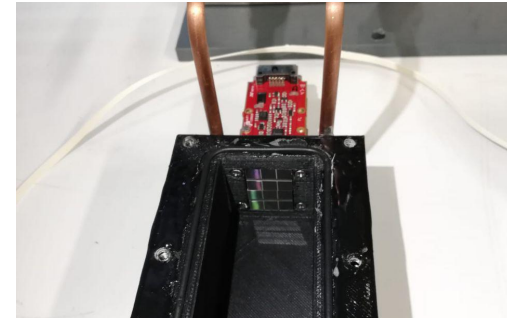
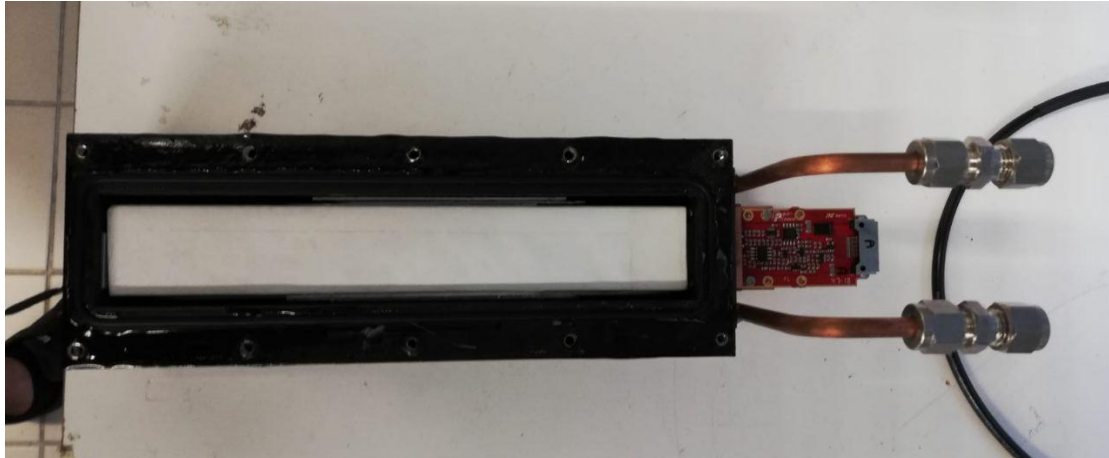
- About 50k events of cosmic rays collected..
- Data analysis is ongoing!

Slice Test @ Pisa – Aug 2019

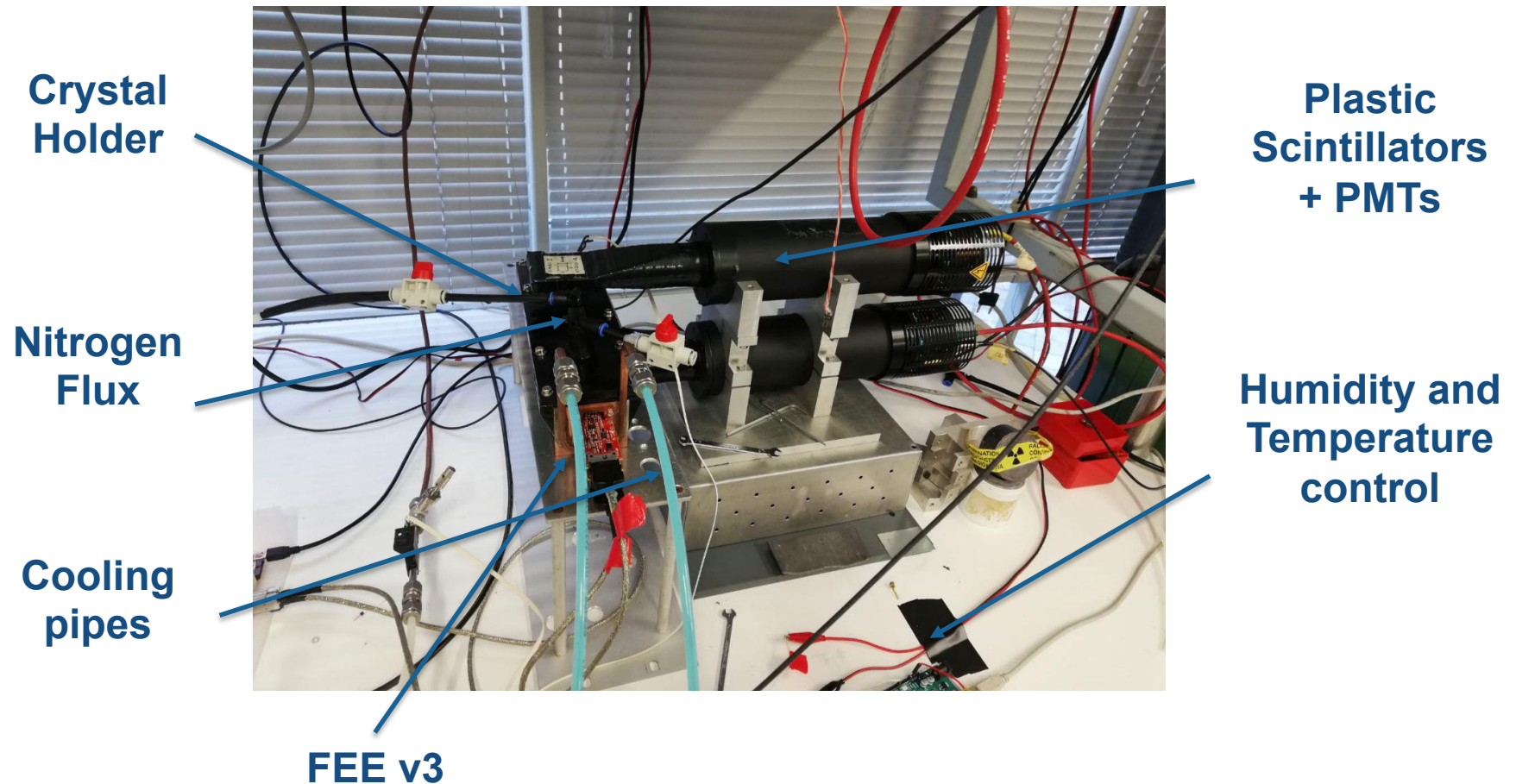


Catena di acquisizione completa: **1 cristallo di produzione**, 2 SiPM, 2 FEE,
1 cordellino, 1 DIRAC, 1 Mezzanino (usato per controllare HV)
Controllo di temperatura, flusso di azoto
Misure accurate dei parametri di amplificazione

Slice Test @ Pisa – Csl Crystal Holder Aug 2019

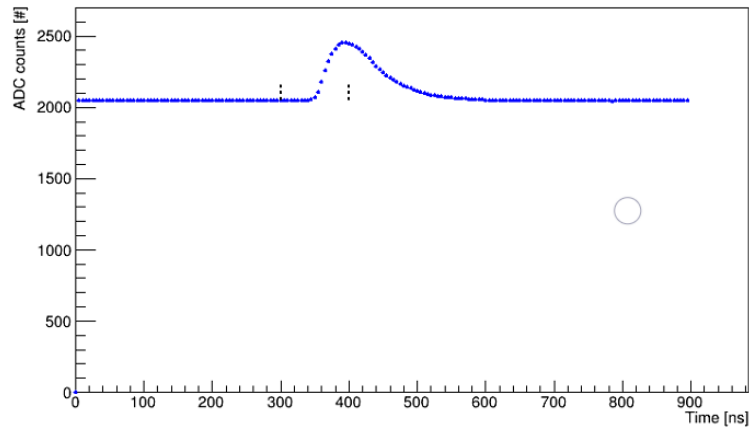


Slice Test @ Pisa – Experimental Setup

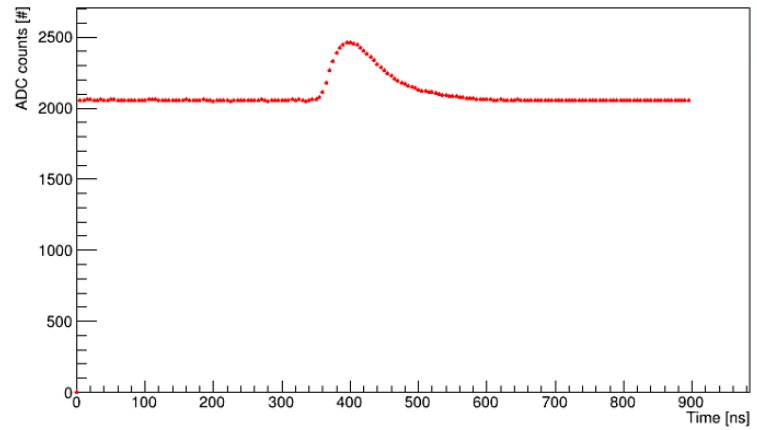


Slice Test @ Pisa – Online Monitor

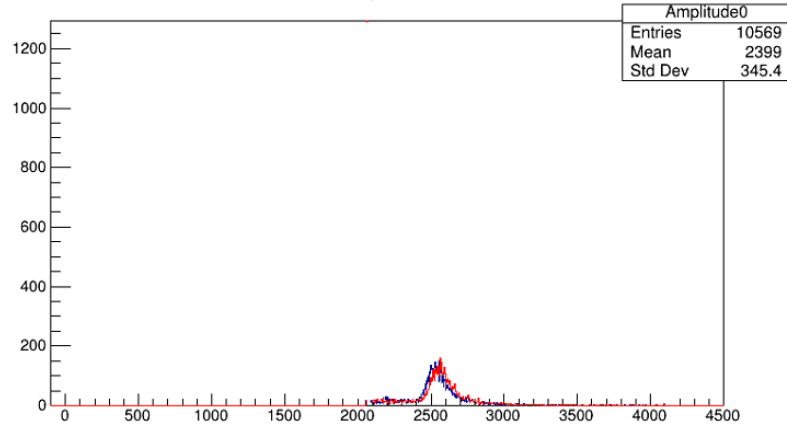
Channel A



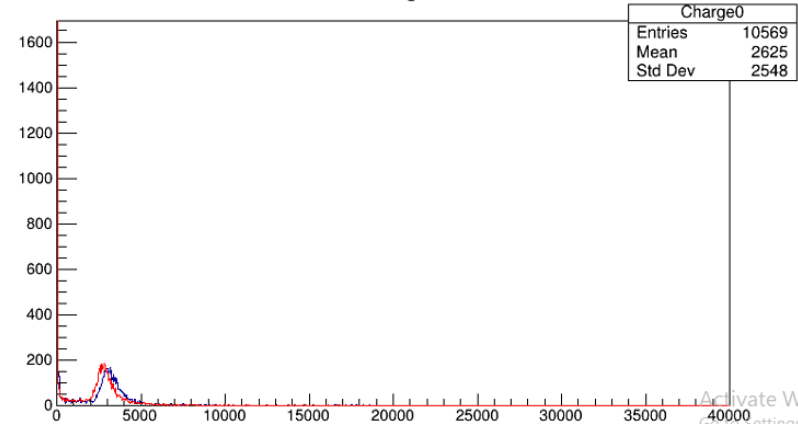
Channel B



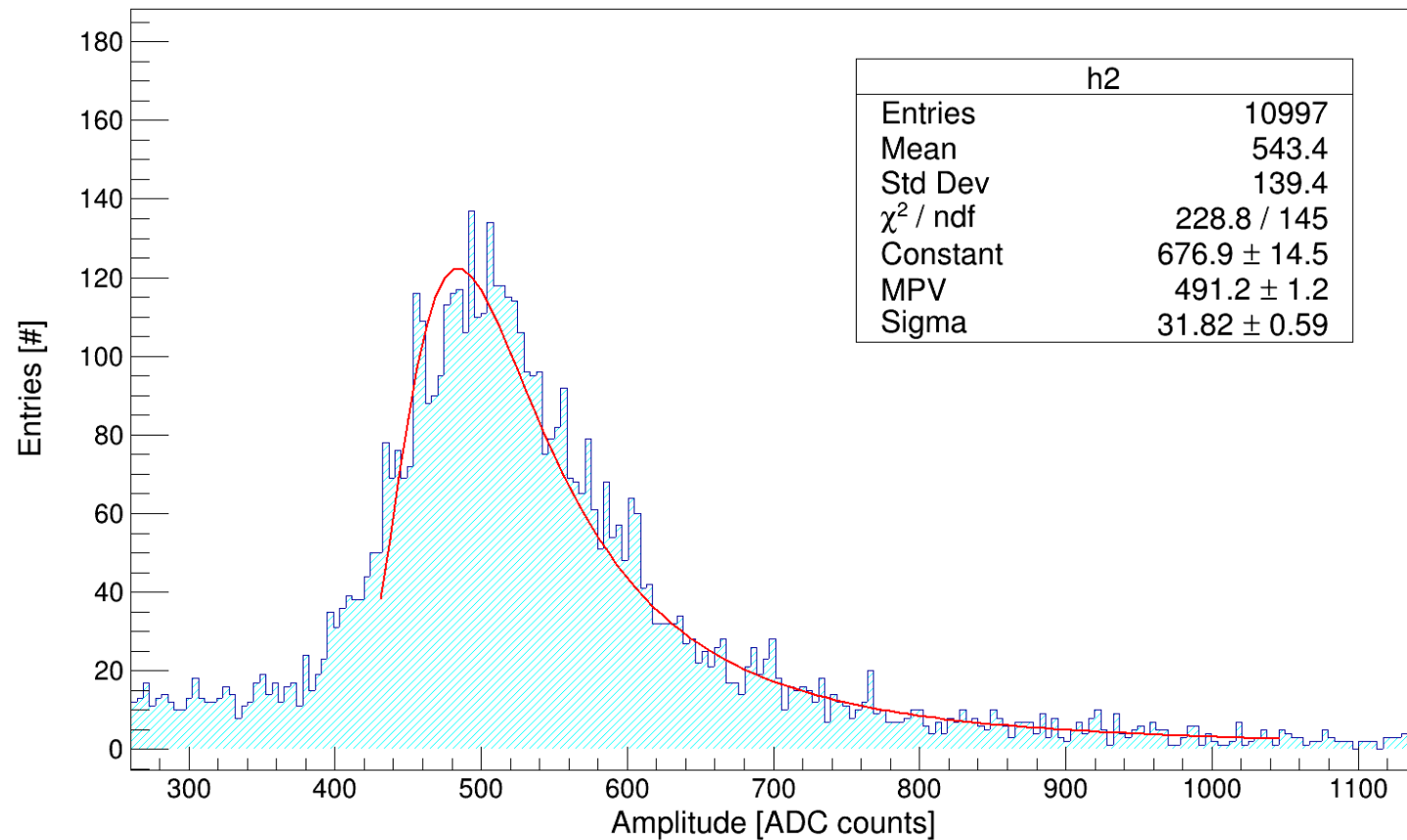
Amplitude



Charge

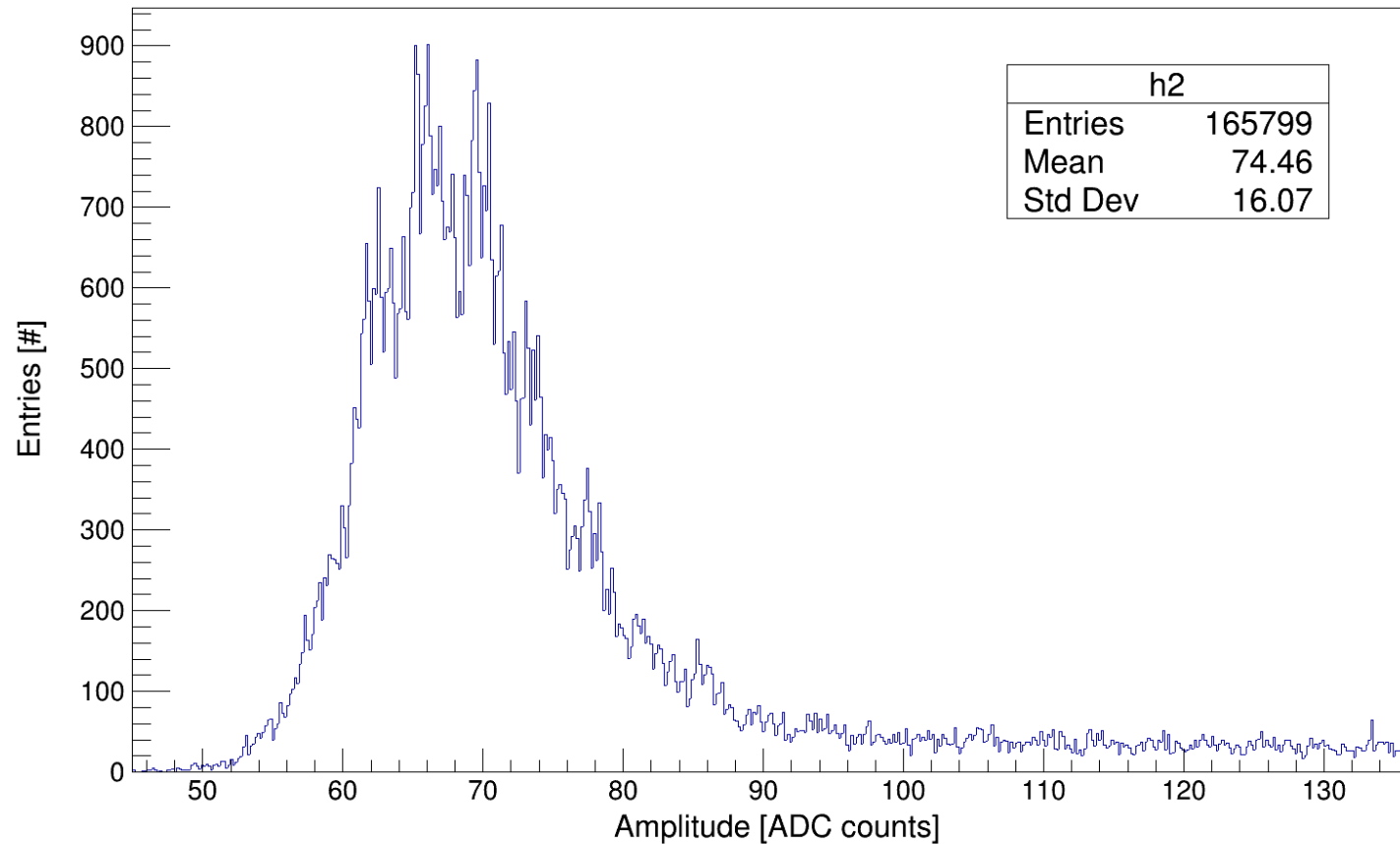


Slice Test @ Pisa – Cosmic Rays



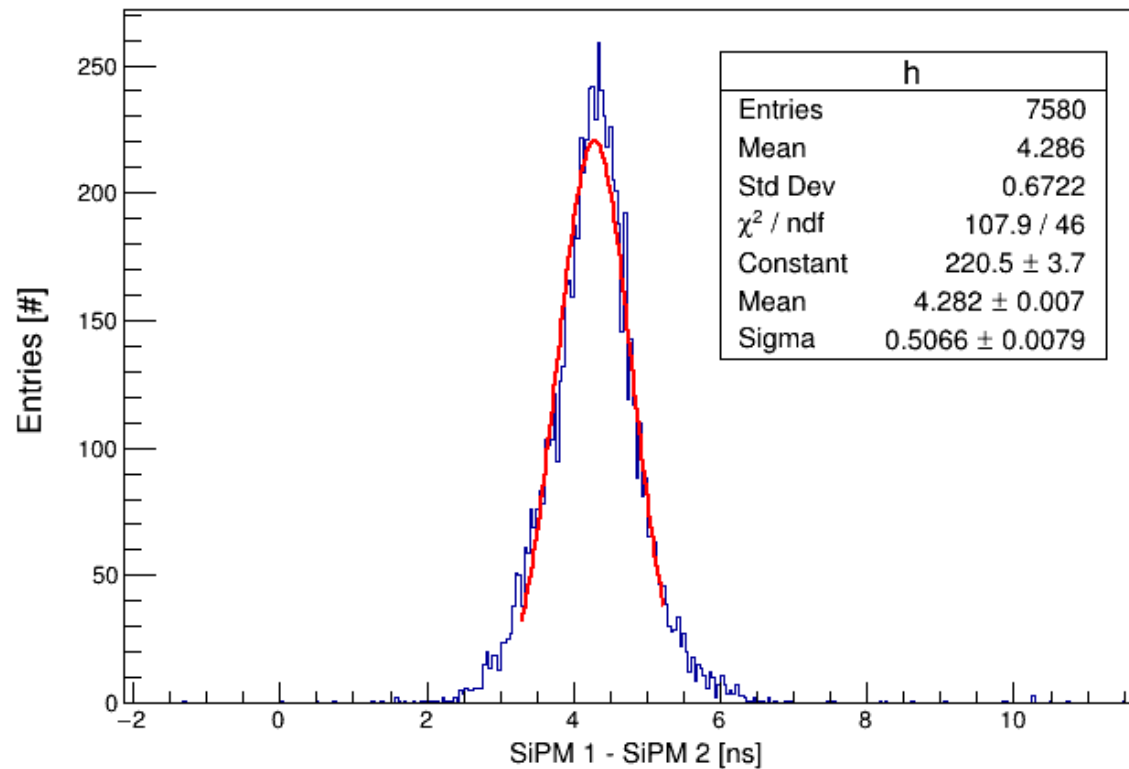
Slice Test @ Pisa – Radiative Bkg + 60 Co

amplitude[5][1]



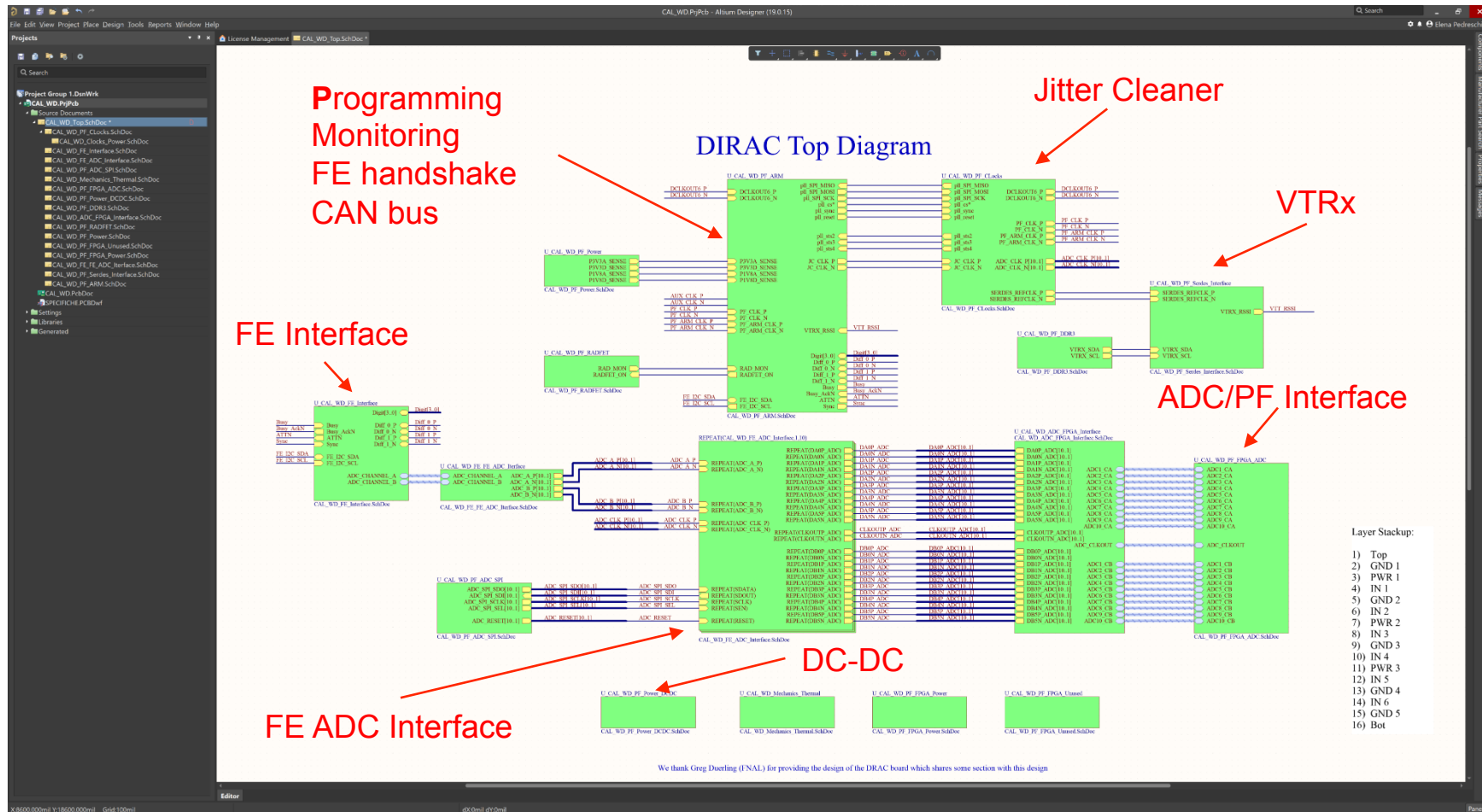
Slice Test @ Pisa – Time resolution

fittime[5][1]-fittime[4][1] (isTime[5][1] == 1 && isTime[4][1] == 1 && charge[5][1] >8000)



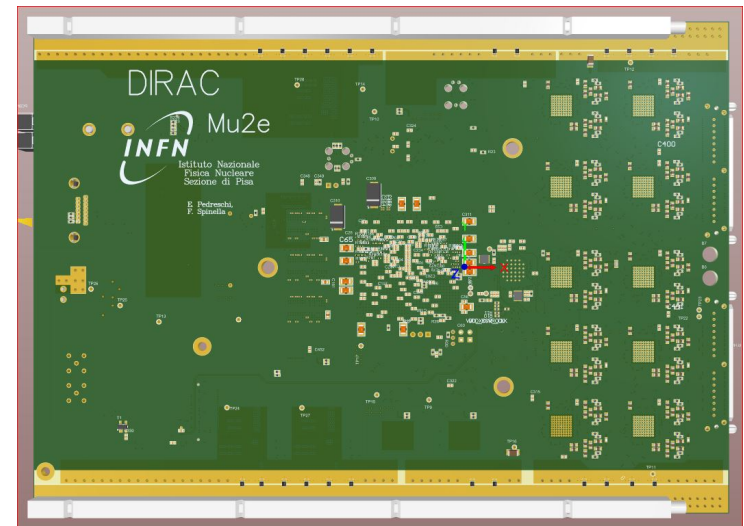
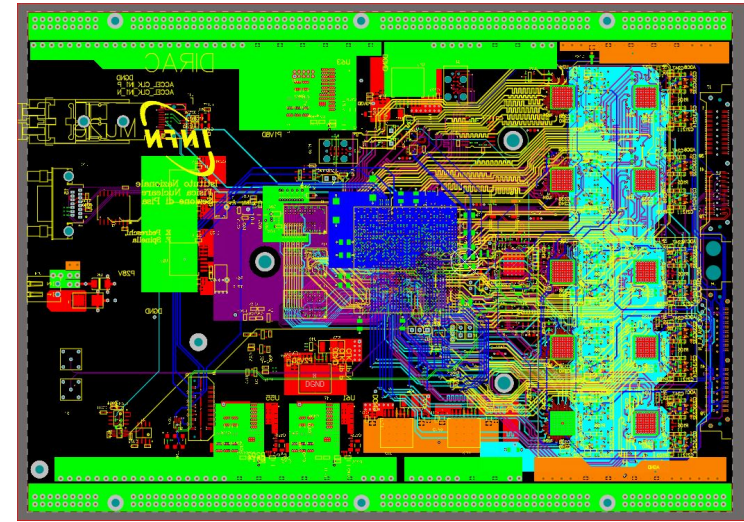
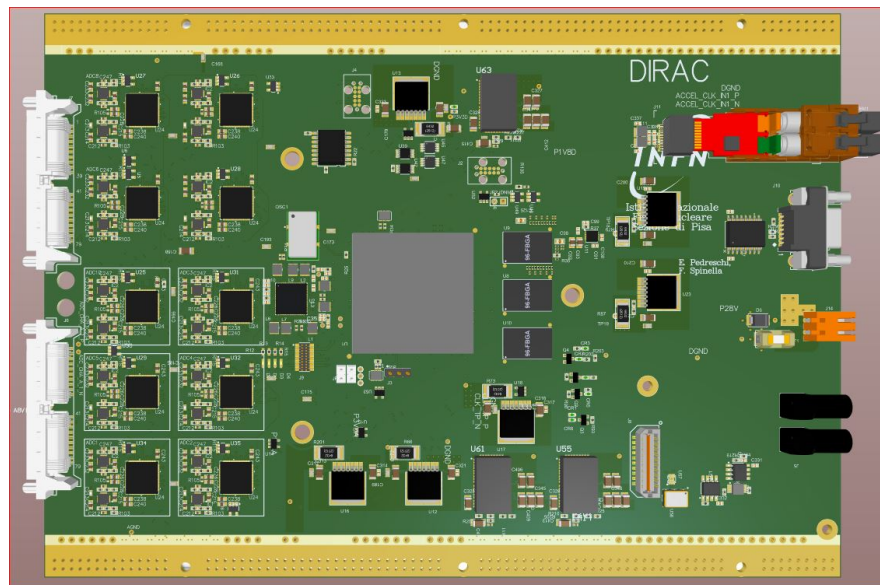
$0.50/\text{SQRT}(2) = 350$ ps, stesso risultati per
cosmici a 20 Mev col M0 e DAQ CAEN

DIRAC V2 design ...



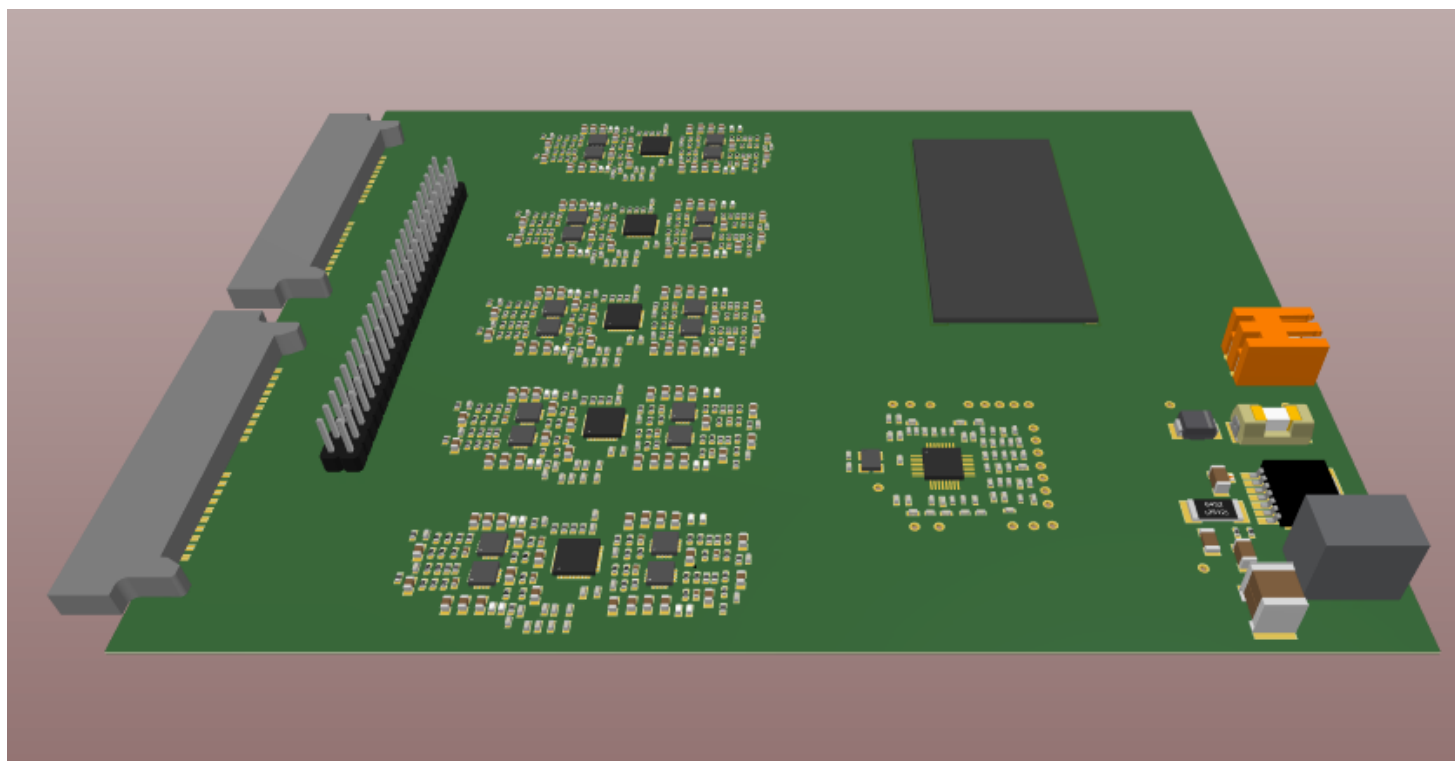
DIRAC V2 PCB

- Sbroglino commissionato al CERN
- GERBER consegnati qualche giorno fa
- Componenti x 5 prototipi a Pisa
- In produzione 2 + 3 prototipi
- consegna in ottobre



DIRAC V2: test board

- Necessaria scheda di test per impulsare DIRAC V2 con 20 segnali «noti», studi di crosstalk (F. Morsani, A. Taffara)
- Fondamentale per test della produzione
- Progetto e PCB pronti (consumi 2019 ...)



Interesse nel progetto ...

- Dal punto di vista dell'elettronica e della meccanica (vedi talk F. Raffaelli) il progetto del DAQ suscita molto interesse tra gli studenti ...
- 5 laureandi (laurea magistrale)

Staff		FTE	
Giorgio	Bellettini	0.0	Ass. Eminent Personalita'
Franco	Cervelli	0.0	Ass. Over 65
Riccardo	Ciolini	1.0	PA UNIFI
Francesco	D'Errico	0.5	PO UNIFI
Stefano	Di Falco	0.4	Ricercatore INFN
Simone	Donati	0.7	PA UNIFI
Carlo	Ferrari	0.5	Ric. CNR Pisa
Antonio	Gioiosa	1.0	Ass. Ric. UNIFI (1 Settembre 2019)
Valerio	Giusti	1.0	PA UNIFI
Andrea	Marini	1.0	Ass. Ric. UNIFI
Luca	Morescalchi	1.0	Ass. Ric. INFN
Elena	Pedreschi	1.0	Tecnologo Art. 36 INFN
Fabrizio	Raffaelli	0.3	Dirigente Tecnologo INFN
Franco	Spinella	0.6	Primo Tecnologo INFN

9 FTE nel 2020
8.9 FTE nel 2019
Numerosi studenti

Laureandi		
Gabriele	Taddei	Ing. Meccanica UNIFI
Alessandro	Crescini	Fisica UNIFI
Bastiano	Vitali	Fisica UNIFI (Borsa INFN 3 mesi a Fermilab)
Micol	Rigatti	Ing. Elettronica UNIFI
Francesco	Neri	Ing. Aerospaziale UNIFI

SummerStudents		
Giovanni	De Felice	Fisica UNIFI
Jacopo	Aurigi	Ing. Aerospaziale UNIFI
Leonardo	Gozzini	Ing. Meccanica UNIFI
Andrea	Fino	Ing. Meccanica UNIFI
Corrado	Comino	Ing. Elettronica UNIFI

Budget DIRAC : prototipi

- Prototipi DIRAC V2 finanziati nel 2018
- Sbroglio effettuato al CERN, V2 molto diversa da V1, aggravio costo di +10K (fondi 2019)
- V2 molto diversa da V1 ... non si esclude prototipo V3 con piccoli aggiustamenti (20K SJ fondi 2020)

Budget DIRAC : produzione 1/2

- Finanziata su fondi 2019: 290K + 30K SJ
- Analisi di mercato molto accurata tra giugno e luglio 2019
- Soluzione piu' conveniente: 2 gare separate, una per acquisto componenti e una per PCBA, DCDC acquistati tramite FNAL
- Offerte informali «precise» per le due gare.
- Gara 1: componenti 170K
- Gara 2: PCBA + spedizione 70K
- Totale 240K
- DCDC converter acquistati tramite FNAL 10K
- Sbroglio CERN 10K
- 30K rimanenti: 10K extracosto LV (vedi dopo) power supply, 20 K a LNF

Budget DIRAC : produzione 2/2

- 30K SJ 2019 chiediamo che siano spostati al SJ 2020 (gia' nelle richieste di Pisa)
- 10K extracosto produzione (gli importi max delle gare non hanno margine rispetto all'offerta informale ...)
- 20K eventuale prototipo V3

LV power supply system 1/2

- Selezionato il modello TTI CXP400SP , 20A 60V, programmabile da remoto, compatibile con slow control FNAL. Testato a FNAL, LNF.
- Ne servono 44 pezzi + 1 spare
- Offerta con acquisto a FNAL e ricerca di mercato in Italia

SKU Manufacturer's Pa 49 57% 9:42 AM

Qty Price Ext Price

1.1	05X0011	RM460	EA/1
2		\$146.75 \$293.50	

Requested Part # 05X0011
Description: 4U Rack Mount for CPX400, QPX & PL PSUs
Manufacturer's Brand: AIM-TTI INSTRUMENTS
Minimum/Multiple Order Quantity: 1/1
On Hand Inventory: 0
Expected Ship Quantity: 2, Expected Ship Date: 05/28/19 **
Estimated lead time 32 days when no stock.
RoHS compliant?:
SPECIAL ORDER ITEM -- NON-CANCELABLE AND NON-RETURNABLE

3.1	04X9895	CPX400SP	EA/1
8		\$899.00 \$7,192.00	

Requested Part # 04X9895
Description: POWER SUPPLY, BENCH, ADJ, 10/P, 60V;
Power Supply Output
Type:Adjustable; No. of Outputs:1 Output;
Output Voltage Min:0V;
Output Voltage Max:60V; Output Current
Min:0A; Output Current
Max:20A; Power Rating:420W; Plug Type:US
Manufacturer's Brand: AIM-TTI INSTRUMENTS
Minimum/Multiple Order Quantity: 1/1
On Hand Inventory: 5 *
1st Expected Ship Date & Quantity: 04/25/19 , 5,
Final Ship Date: 06/03/19 **
Estimated lead time 37 days when no stock.
RoHS compliant?: Yes

CPX400SP - ALIMENTATORE DA LABORATORIO DUALE 420W / 60V / 20A - INPUT 100-240 VAC

909,48 €

Tasse escluse

da 786,70 € per 20 pz

Quantità	Prezzo
1-4	909,48 €
5-9	868,56 €
10-19	827,63 €
20 +	786,70 €

LV power supply system 2/2

- Acquisto in Italia + spedizione sembra piu' conveniente:
 - $786 \times 45 + 3\text{-}4\text{K}$ spedizione = 40K
 - FNAL $(899 \$ \times 45) * 1.38 = 50\text{K}$ euro (OH = 38 %)
- Consumi 2019 25 K + 5K SJ, mancano 10K da risparmio produzione DIRAC

RICHIESTE 2020

Sistema misura rad ionizzante e non, Temp 1/2

- 12 stazioni di misura x disco
- Per i neutroni utilizzeremo i SiPM standard, misurando l'aumento di Idark con la radiazione (calibrato con dati presi a ENEA varie volte)
- Per dose: RadFet Tyndall Ty1003 (standard), fondo scala 100 Krad, calibrato dalla fabbrica.
- Temperatura: DS18B20
- RadFeT e DS18B20 sono stati qualificati a HZDR (Maggio 2019)

Sistema misura rad ionizzante e non, Temp 2/2



- Readout basato su DIRAC V2
- Necessario sviluppare un mezzanino nuovo e delle schede FE per alloggiare RadFet e sensori di temperatura
- Architettura in via di definizione ...
- Costi:
 - 4 DIRAC : 8K
 - 24 FE + spare : 12K (include 4K RadFET)
 - 4 Mezzanini modificati + spare : 4K
 - Sviluppo prototipi: 6K
 - Totale 30K

Feedthrough fibre elettronica TDAQ e laser

- Sviluppati in house a FNAL
- Connettore FIBRA: MTP-12
- 28 MTP-12 x CAL READOUT
- Costo preventivo FNAL 0.8 K/feed
- $0.8 \times 24 = 20K$
- Chiediamo 10K + 10K SJ (SJ non riportato nei preventivi, stima di FNAL recente)



Fibre elettronica TDAQ

- Due tipi di fibre:
- RadHard, single LC, da Feedthrough a DIRAC, 136 fibre, 10m
- MTP-12, da feedthrough a counting room, 28 fibre, 60m
- Preventivi da FNAL in fase di definizione
- Richiesta 19K SJ arrivo preventivi FNAL (richiesta non presente sui preventivi INFN)

Sistema di distribuzione laser

- Vedi talk Stefano
- Alcuni parti comprate a LNF. A Pisa: fibre e laser feedthrough
- Fibre ottiche 8 + 4 spare.
- Fibre corte dentro DS, lunghe all'esterno
- Offerta da Optiprim: 350 \$ corte, 1500 \$ lunghe
- $(1500 + 350) * 12 = 22000 \$ = 20K \text{ euro}$ (preventivi 2020)
- Laser feedthrough $12 * 450 \$ = 5400 \$ = 5K \text{ euro}$ (non inseriti nei preventivi 2020)