Activities List(BrainStorming)

- Simulation Activities:
  - Setup Cadence.
  - Definition of a minimal set of simulation/functionalities to be used step by step to check the design.
  - Step by Step Design verification (Synthesis, P&R, Backannotation).
  - Test Vector Preparation.
- Full Custom Activities:
  - Standard CAM Preliminary Studies: Area estimation, Specifications Analogue Simulation.
  - Layer "CAM" design: layout and analogue simulation.
  - Layer CAM as std-cell: timing libraries generation, LEF, DEF, characterization in the 3 corners (bc, wc, tc)
  - Single Pattern analogue simulations.
  - Pattern Block Analogue Simulation/Check
- STD-CELL Activities:
  - Synthesis with Fake Pattern Bank
  - P&R with Fake Pattern Banks (assuming std-cell development faster than full custom...)
  - Backannotation and timing studies in the 3 corners.
- Floorplane
  - Area Estimation std-cell and full-custom
  - Die Area and Pinout definition.
- Others
  - Documentation ("Written" by the designers and tested by the simulator people)
  - CVS :
  - Package Definition

Schedule (no yet detailed)

- **DICEMBRE**
  - FLOORPLANE ACTIVITIES: Area Estimation STD-CELL (Synthesis with Fake Pattern Bank) and Full-Custom (Preliminary Studies CAM and *Layer*).
  - FLOORPLANE ACTIVITIES: Die Area and Pinout definition.
  - Setup Cadence Simulation, definition of a minimal set of simulation.
- **GENNAIO**
  - Standard CAM Studies: Specifications, Layout, Analogue Simulation.
  - Layer "CAM" design: layout and analogue simulation.
  - Layer CAM as std-cell: timing libraries generation, LEF, DEF, characterization in the 3 corners (bc, wc, tc)
  - Synthesis with Fake Pattern Bank
  - P&R with Fake Pattern Banks (first check of the overall design).
  - Simulation of the design synthesis (check of behavior)
- **FEBBRAIO**
  - P&R with Real CAM backannotation production.
  - Pattern and Block Analogue Simulation
  - Simulation of the P&R design (check of the timing)
- **MARZO**
  - Simulation with Final Timing
  - Timing Check
  - Pattern and Block Analogue Checks
- **APRILE**
  - Test Vector production/ Simulations