Recent developments of a monolithic silicon pixel detector on medium resistivity substrates

M. Caselle[1,2],
W. Snoeys[1], K. Kloukinas[1], A. Rivetti[3], H. Mugnier[4] , J. Rousset[4], P. Chalmet[4],
A. Dorokhov[5]

1) CERN, 2) INFN Bari 3) INFN-Torino, 4) MIND, Archamps, France,
5) IRES, Strasbourg, France

Outline

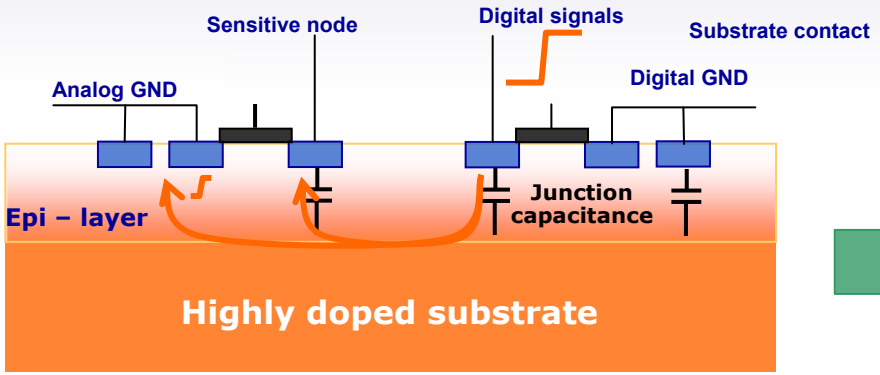
- Standard CMOS in lightly doped substrate
- New matrix concept & readout architectures
- Pixel concept & strategies
- Chips matrix sent to foundry (march 2010)
- Conclusions

References:

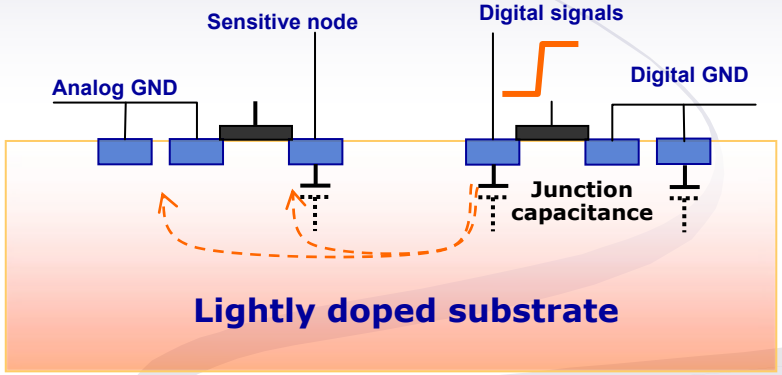
- **M. Caselle, IFAE 2009**, Bari 15-17 April 2009, **"A monolithic pixel detector for future HEP experiments",** IL NUOVO CIMENTO - DOI 10.1393/ncc/i2009-10480-x
- **A. Rivetti, ICATPP Conferences,** Villa Olmo 5 – 9 October 2009, **"Lepix: monolithic detectors for particle tracking in standard very deep submicron CMOS technologies**.

Standard CMOS on lightly doped substrates

- First feedback from the foundry that standard deep submicron CMOS processes can be reliably implemented with wafer of higher resistivity (> 100 Ωcm).
- Higher substrate resistivity enhances the separation between different circuit blocks (better insulation between digital and analogue).



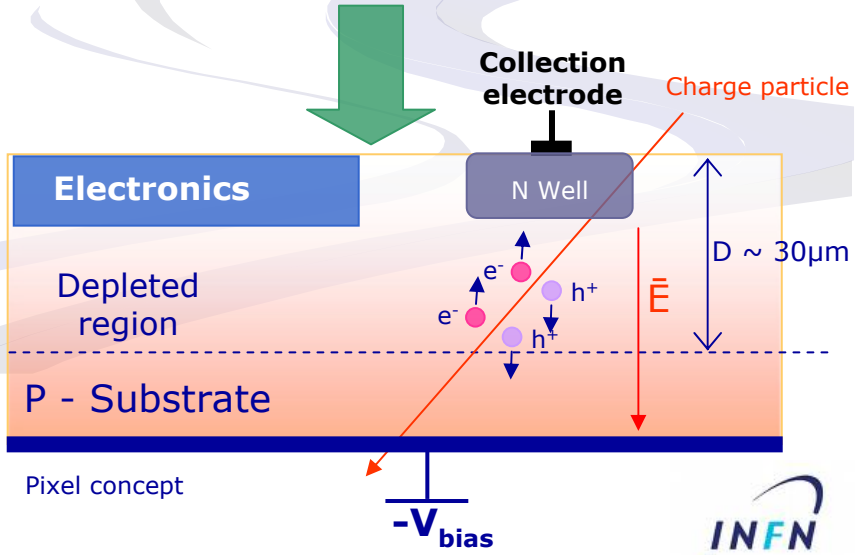
CMOS process



New standard deep submicron CMOS process

A resistivity of 200 Ωcm should allow a uniform depletion layer of 30μm – 40μm with a reverse bias voltage of 100 V.

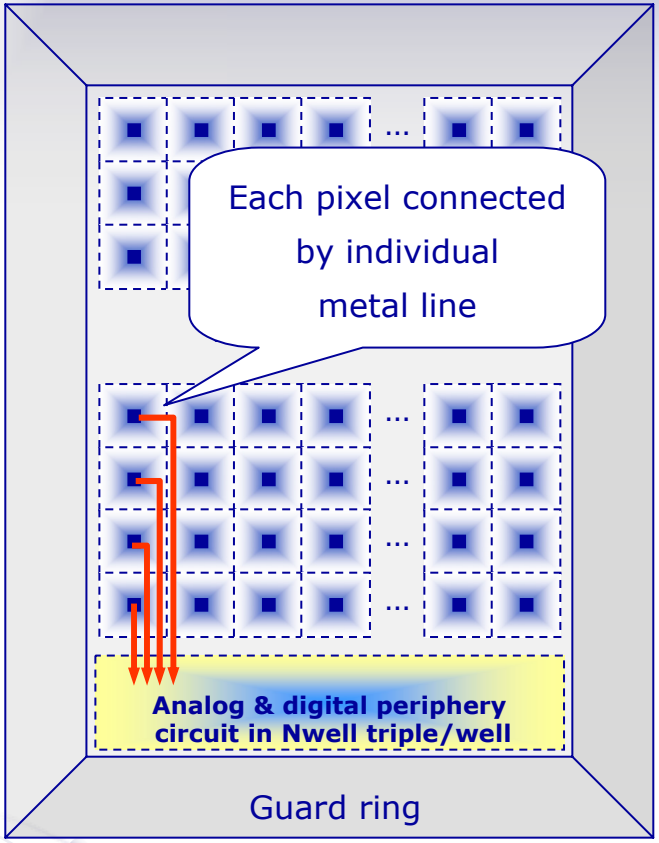
Collection by drift + moderate resistivity: good radiation hardness (adequate for LHC upgrades).



Pixel concept

New matrix readout concept

High metal density in 90 nm CMOS allows to connect every pixel in the matrix to the periphery by means of an individual metal line. This solution allows to make the information of the fired pixels prompt available at the periphery at the bunch crossing frequency (*i.e.* 40MHz for LHC/sLHC).

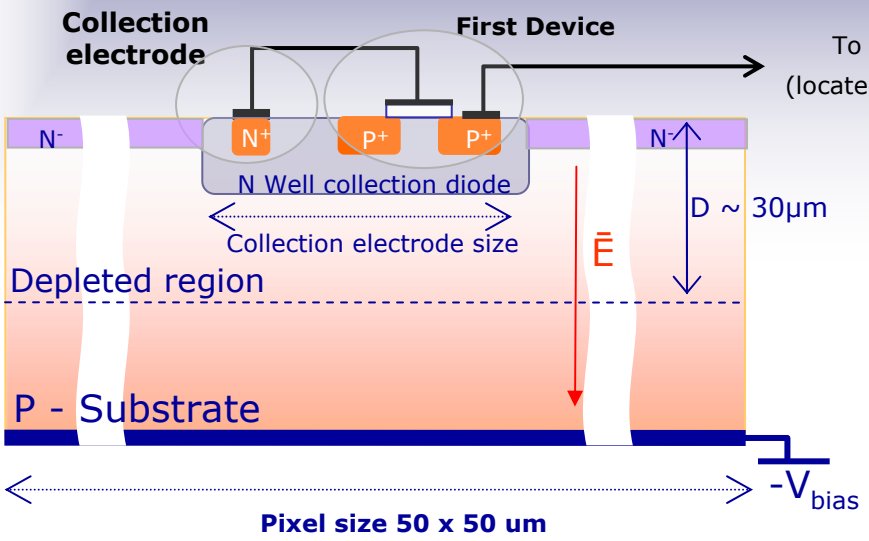


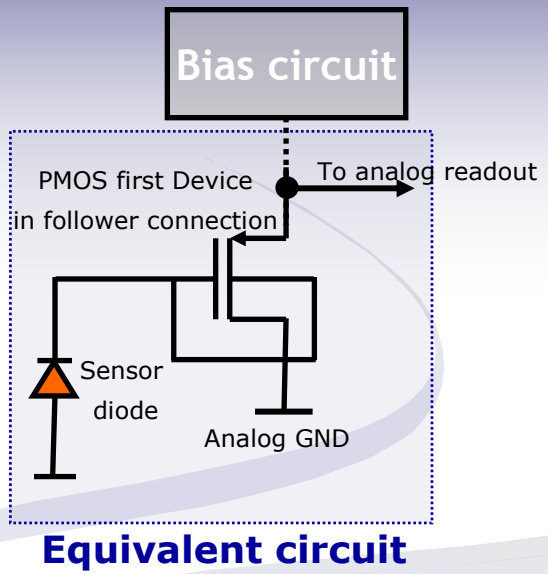
- Different concept from the typical current pixel detectors where the information is temporarily stored in the pixel cells until it is transferred at the end of a column of the column-wise organized R/O-chip.
- The ***S/N*** and the **power consumption** for clock distribution profit of the absence of digital signals distributed over the matrix, the overall power budget estimated is around **10mW/cm²**.
- A challenge is to keep the area of the readout to a small fraction of the total surface of the chip.
- All circuit is in Nwell triple well to garreteer a proper insulation from High Voltage bias applied to substrate

Concept implemented in the first demonstrator

First sensor concept

In the center there is the charge collection electrode, an Nwell with PMOS transistor embedded.





Equivalent circuit

Both the **S/N** ratio and electrical power depends from the total input capacitance $C_{IN\ TOT}$, we would like to keep smaller the total input capacitance.

$C_{IN\ TOT} = C_{Nwell} + C_{MOS} + C_{paras}$ → first contribute depends from Nwell collection electrode size, second from MOS type and size

(For 30 um depletion region and C_{IN_TOT} = 10fF capacitance → V_{signal} = 38 mV @ 1 MIP)

Two different Nwell electrode size a "small" and "large"

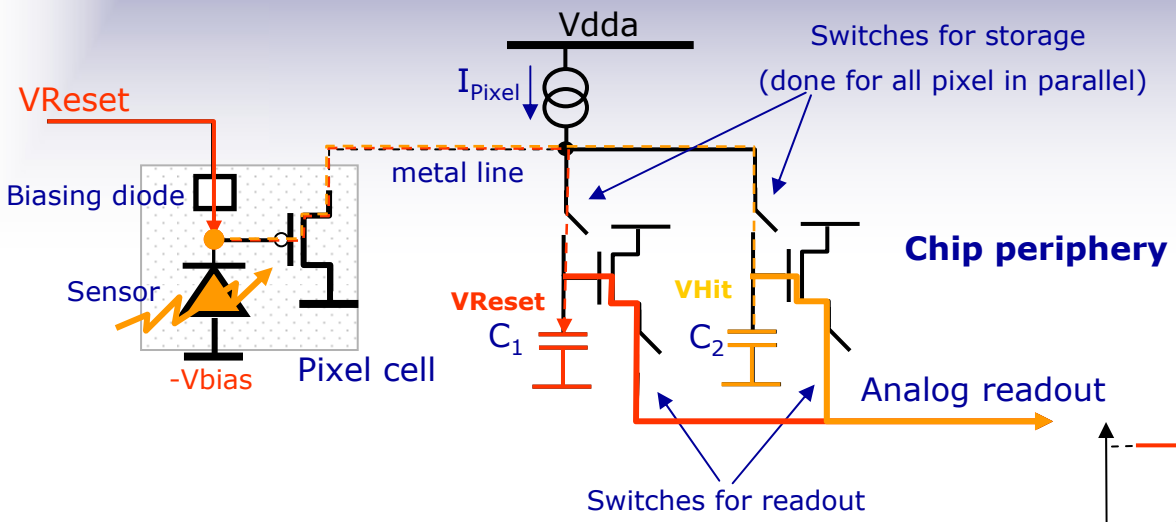
For ck"
PM

Each pixel is permanently connected to its front-end electronics located at the border of the matrix with one dedicated line → need of ultra fine pitch lithography

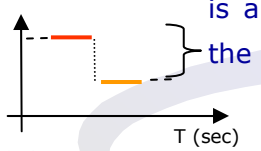
First demonstrator, focusing primarily on the sensor device both evaluation of tracking and radiation tolerance

Readout strategies

Analog sequential readout with double analog storage "Maps-like"

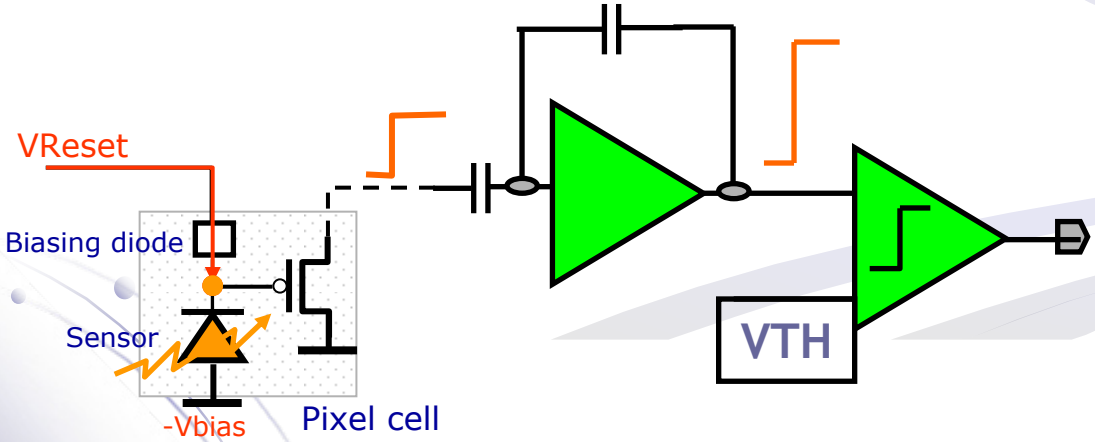


→ The sensitive period is independent from the readout frequency.



The difference between the two values is a measure of the signal collected in the pixel cell

Digital sequential readout with fast shaping time



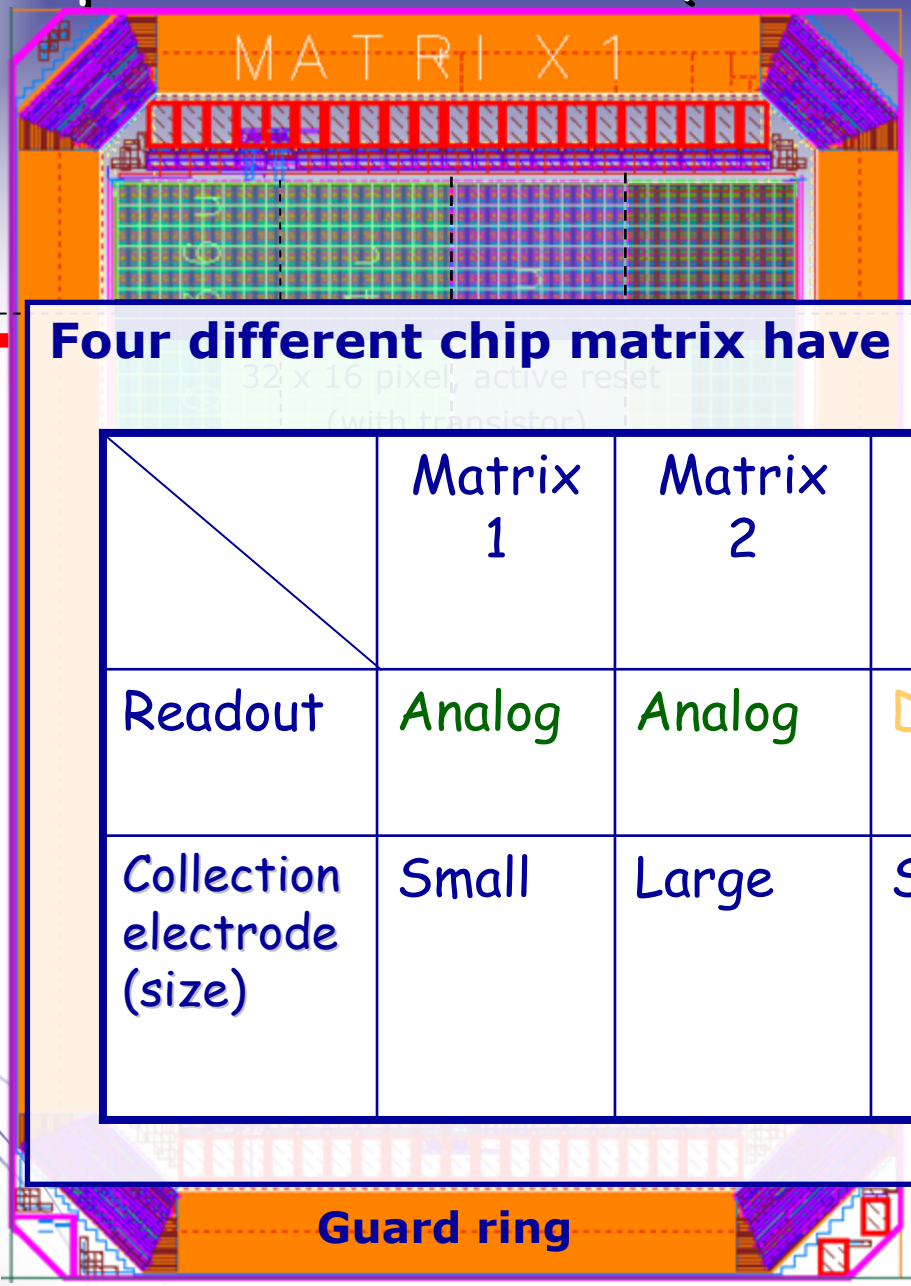
→ Use capacitive coupling into a classical integrator and shaper

→ Allows to be sensitive to sudden signals only.

→ Is relatively insensitive to leakage

→ More closer to final front end

Chip matrix submitted (overview)



Top chip part (32x6 pixels)

Top part with buffers to read analog signal as it is collected

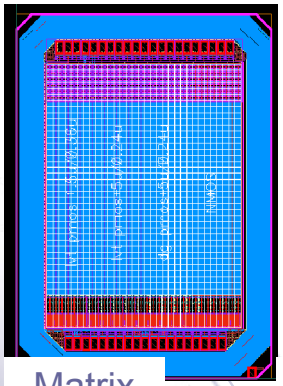
- **Four different chip matrix have been submitted:**

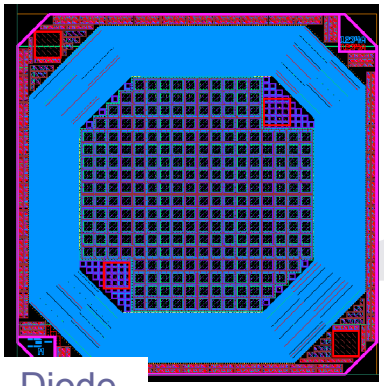
	Matrix 1	Matrix 2	Matrix 3	Matrix 4
Readout	Analog	Analog	Digital	Digital
Collection electrode (size)	Small	Large	Small	Large

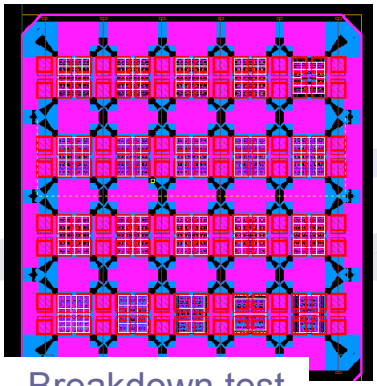
Guard ring structure to support the voltage

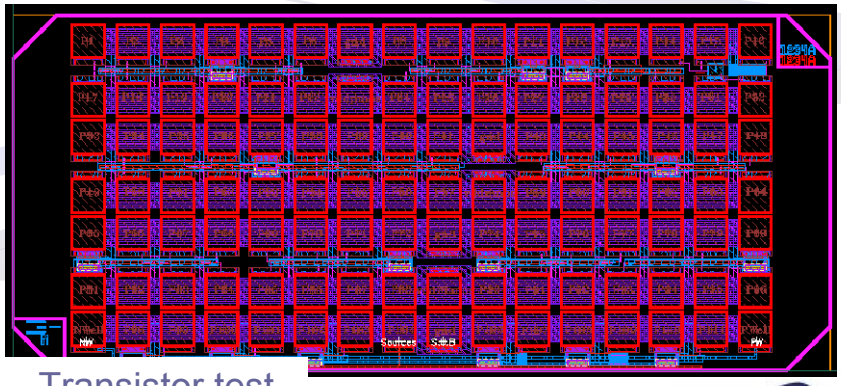
Asics submitted

- Submission for fabrication just finalized
  - Several issues: ESD, special layers and mask generation, guard rings
  - Still need to discuss some manufacturing details with the foundry
- 7 chips submitted :
  - 4 test matrices
  - 1 diode for radiation tolerance
  - 1 breakdown test structure
  - 1 transistor test: already submitted once in test submission
- Will require very significant testing effort for which we need to prepare (measurement setup, test cards…)


Matrix 1


Diode


Breakdown test


Transistor test

Conclusion

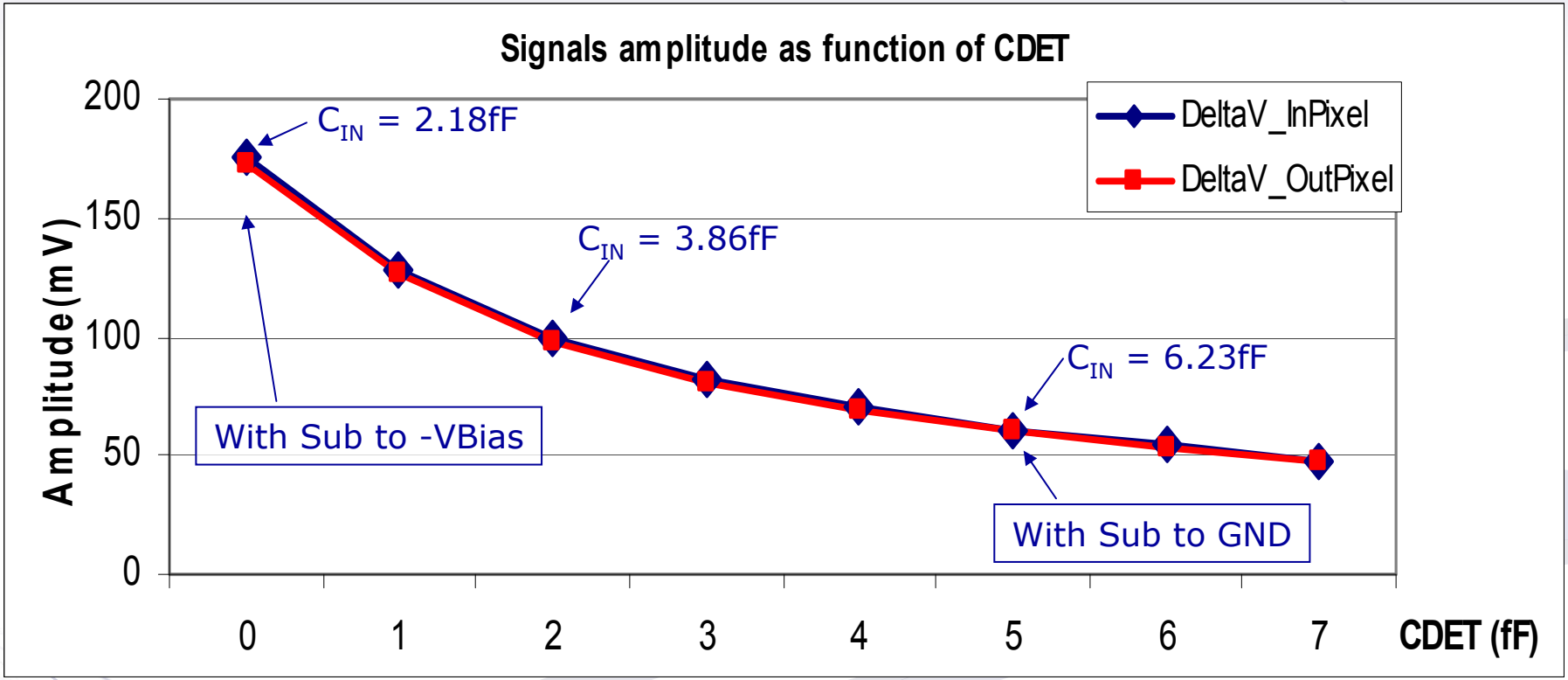
- Cooperative research effort established between **CERN**, **INFN** and **IReS** to investigate new type of monolithic sensors.
- First demonstrator of the proposed devices has been submitted to the foundry in March 2010, it includes:
  - Sensor diode, with different collection electrode and input transistor,
  - Two readout versions: sequential readout with analog storage, sequential readout with shaping,
  - Two Reset mechanism and test pulse capacitance for calibration & test
- Technique: commercial very deep submicron CMOS implemented on lightly doped substrates.
- In addition we are preparing standard test structures to evaluate the radiation tolerance of the transistors in the 90nm CMOS technology
- First experimental results expected half in 2010.

A particular thanks to
V. Manzari, A. Marchioro, M. Winter, …

Backup slides

Pixel simulation (C_{DET} effects)

- $C_{IN} = C_{DET} + C_{PEX} + C_{MOS}$
- C_{DET} value is not easy to evaluate, we will assume as "C_{DET} max value"
  → $C_{DET} = C_{area} + C_{perim.}$ (C_{area}, C_{perim} indicated in the CMOS9SF design manual for 1V)



For the simulation we will assume C_{DET} value = 2fF

Pixel charge resetting strategies

Two reset strategies: