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CMS RPC upgrade phase-II of new Link system

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The High-Luminosity Large Hadron Collider (HL-LHC) increases the rate of luminosity in proportion to the rate of the collisions occurring instantaneously. The HL-LHC produces more data and reveals the rare physical events for the purpose of examination. These features of the HL-LHC sets the high-speed transfer of the fast-incoming data to the next layer. The development of the FPGA technology has given support to high-speed data transfer systems. The significance of using high-speed serial transceivers is that these transceivers help exchange a large amount of data with no need to transmit the clock signal. Therefore, the process of clock recovery on the receiver side can be considered as an advantage of high-speed serial transceivers. The receiver clock data recovery circuits inside the gigabit data transceiver units recover both the clock and the data from the incoming data stream. The starting points of detecting the boundary of each bit from the incoming data stream and converting the serial streams into the parallel data have a significant impact on the phase of the recovered clock. Using the recovered clock and compensating for the phase difference allow us to have a synchronous clock and achieve fixed latency in the data taking system. In this work, the proposed architecture provides fixed and deterministic latency in each power-up by distributing the synchronous clock in the new link system for CMS RPCs and compensating for the phase difference between the receiver and the transmitter.

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