CMS RPC Upgrade Phase-II of new Link System

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- RPC Layer-1 trigger Architecture and

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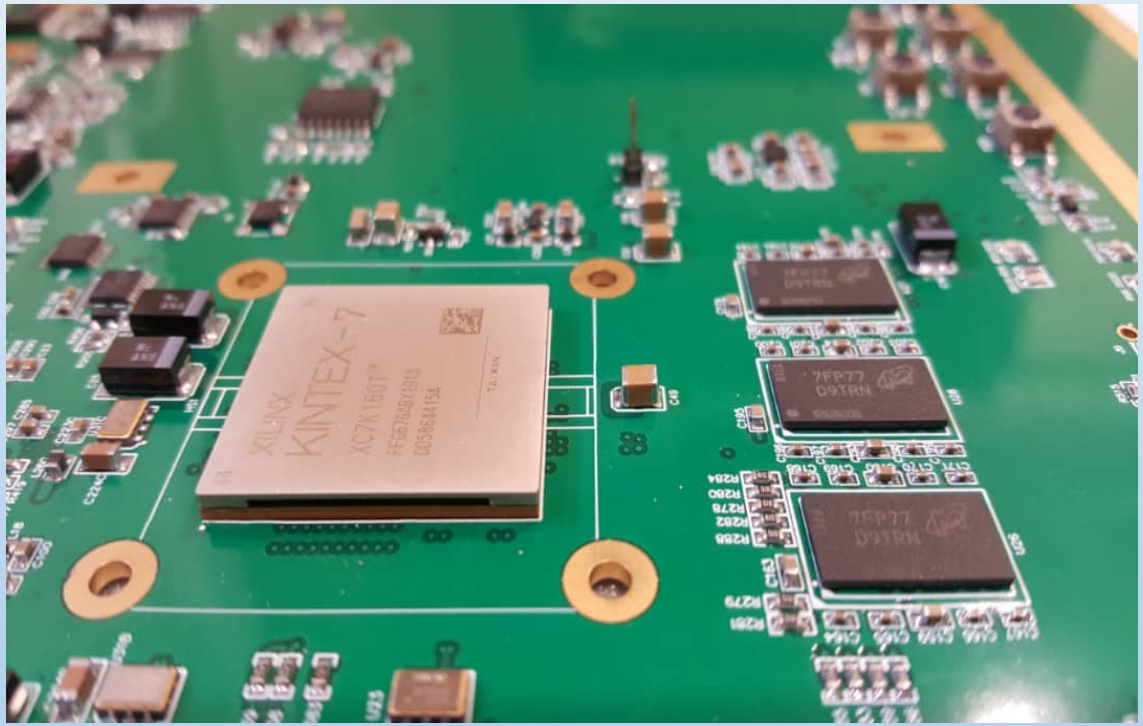
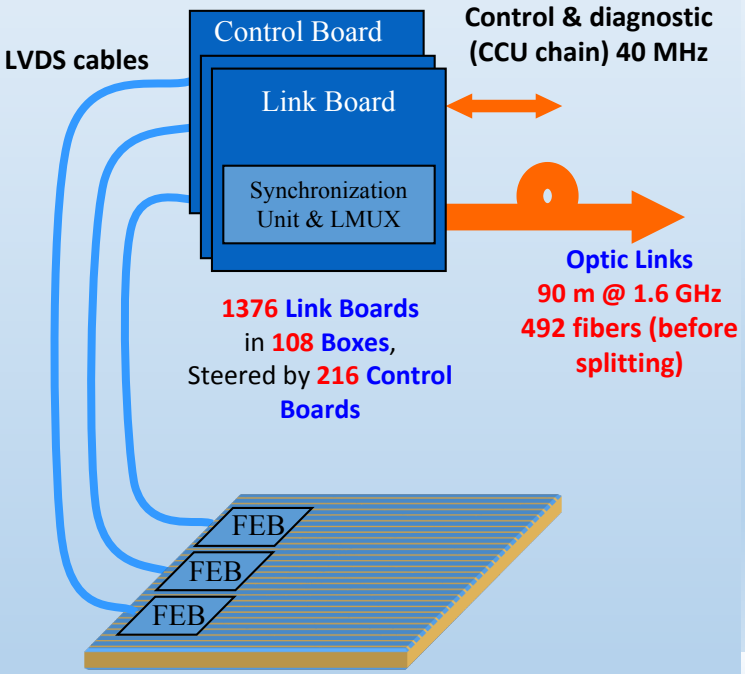
- Control, Diagnostic and Synchronization of New Link System using New Slow Controller
- Summary



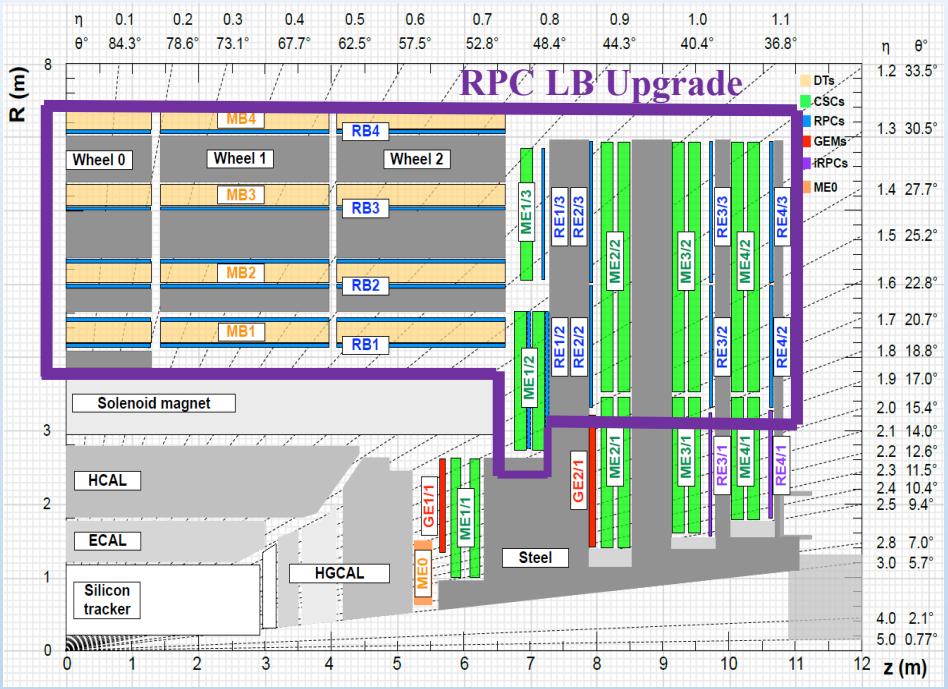
Link System Upgrade Motivation

Present Link Board System



Upgrade Motivation

- Despite the intrinsic resolution of the RPCs, the CMS trigger system is based in the 25 ns sampling.
- Data transmission speed is about 1.6 Gbps
- Control, diagnostic and monitoring of the Link system has been designed based on CCU ring (combination of copper cable and fiber optic), very susceptible to electromagnetic interference



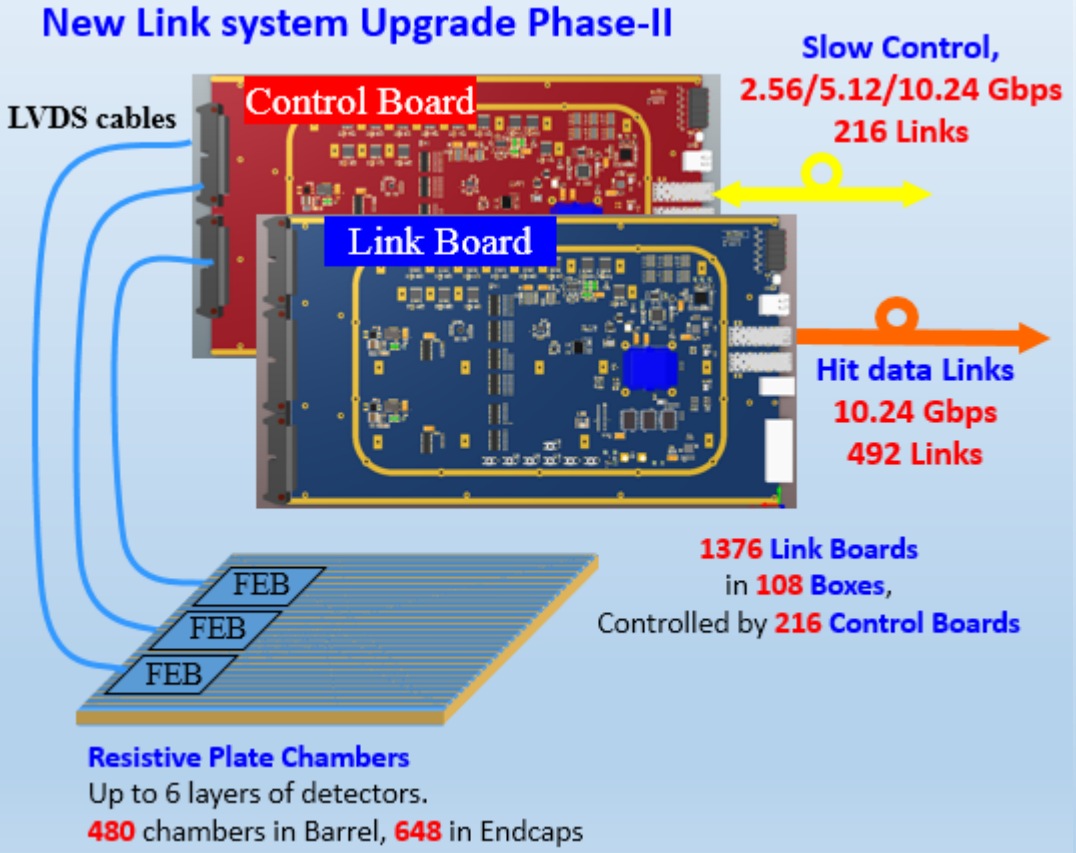
- CCU ring is not very fast, the bandwidth (40 MHz) share between 12 control boards
- Most radiation hard electronic components are obsoleted
- Electronic aging, presently the Link system at the end of LS2 is already 13 years old

New Link System Overview

New Link system Features :

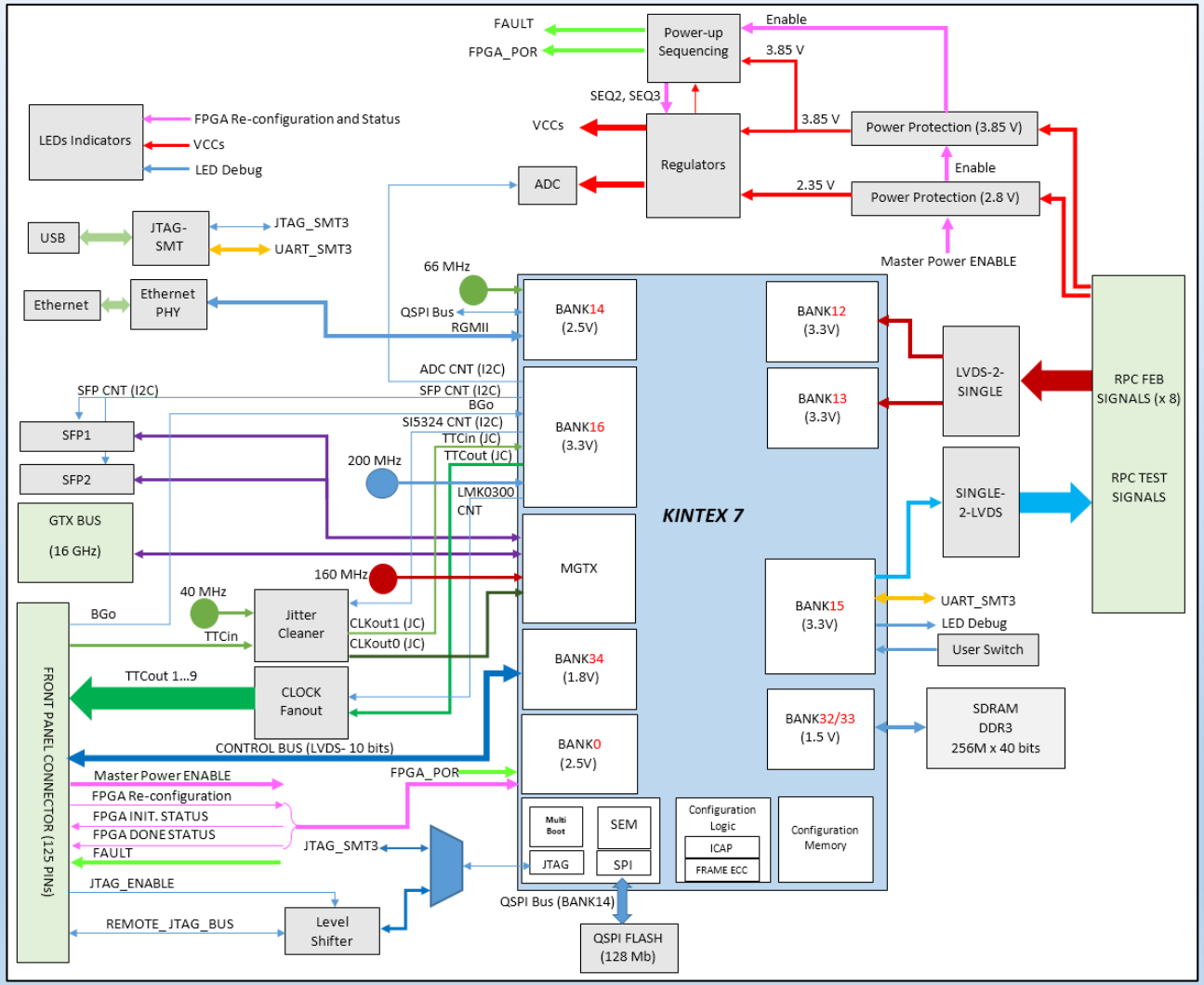
1. FPGAs are KINTEX-7, XC7K160T – Industrial Version
2. Muon hit time, TDC timing Resolution : 1.56 ns
3. Master Link board output data rate : 10.24 Gbps
4. Control Board communication with slow controller at 10.24 Gbps
5. Embedded internal buffer (DDR3) : 1.28 GByte
6. Radiation Mitigation: TMR + Internal Scrubbing
7. Scrub Rate of entire FPGA (Real time SEU detection and Correction) : 13ms (31,770 times faster than the rate of SEU at the Balcony)

- SEU at the Balcony : Every 413000 ms

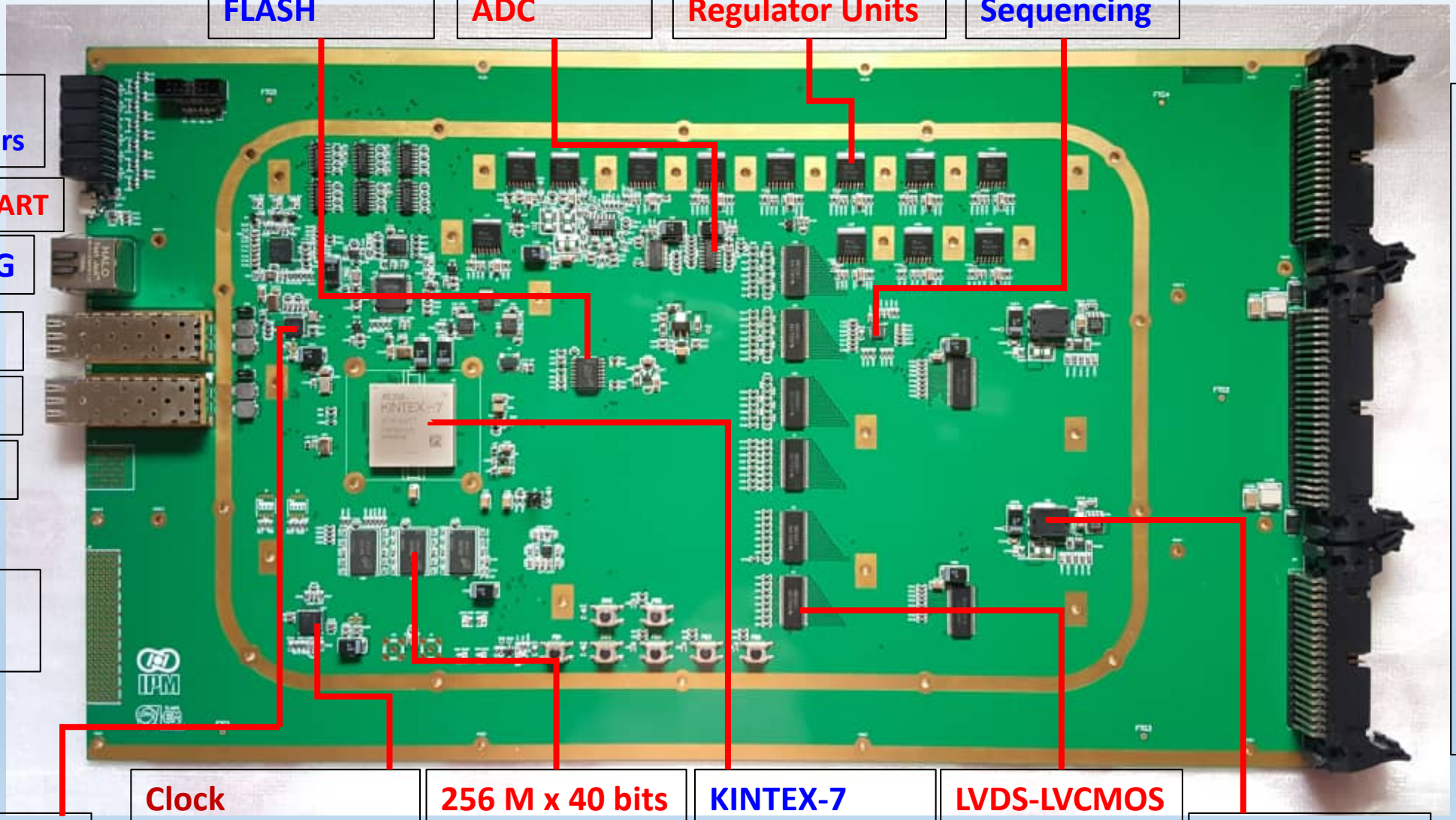


New Link Board Hardware Architecture

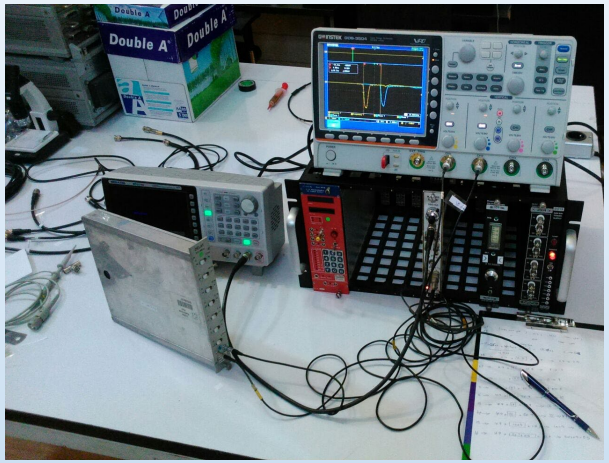
- **The design is based on the TDR baseline and on following specifications and components:**
  1. **FPGAs are KINTEX7, XC7K160T-2FFG676I.**
  2. **Fully support 10.3 Gbps data transmission. FPGA Chip is equipped with heat sink.**
  3. **High resolution TDCs (at the steps of 1.56 ns) implemented into the Kintex7 FPGA**
  4. **Two Redundant optical data transmission line at the data rate of 10.24 Gbps**
  5. **Ethernet link for the debugging and onboard JTAG programmer**
  6. **256 M x 40 bits of SDRAM-DDR3 for data buffering and debugging**
  7. **Data transmission with adjacent slave link boards through the SAMTEC back-plane type connector with bandwidth of 16 GHz and special front panel PCB board (Roger type).**
  8. **Radiation Mitigation is based on Triple Modular Redundancy (TMR) techniques and Soft Error Mitigation (SEM) IP core from Xilinx.**
  9. **Voltage Regulators selected from low dropout linear regulator families which has been tested already under radiation.**



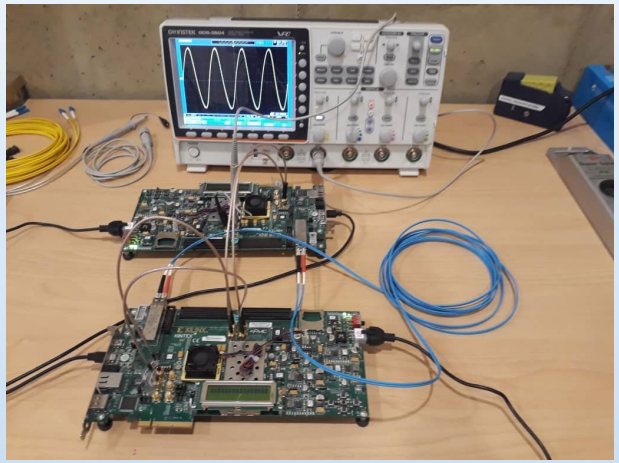
Hardware Prototype of New Link Board



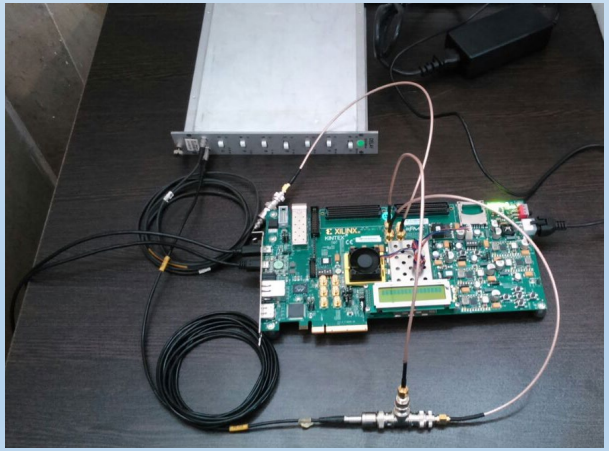
New Link System Firmware List



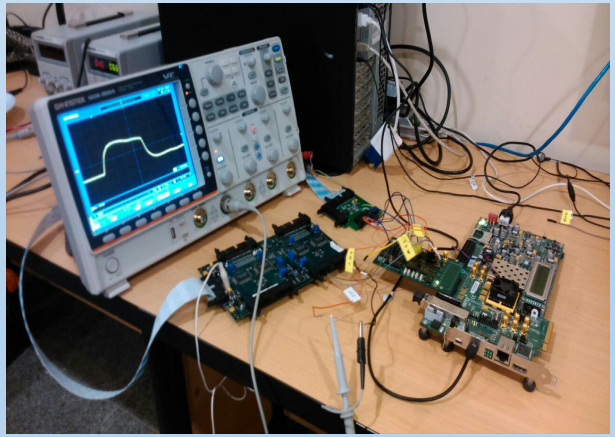
TDC Calibration test setup



Fixed Latency GTX @ 10.24 Gbps



TDC Performance measurement



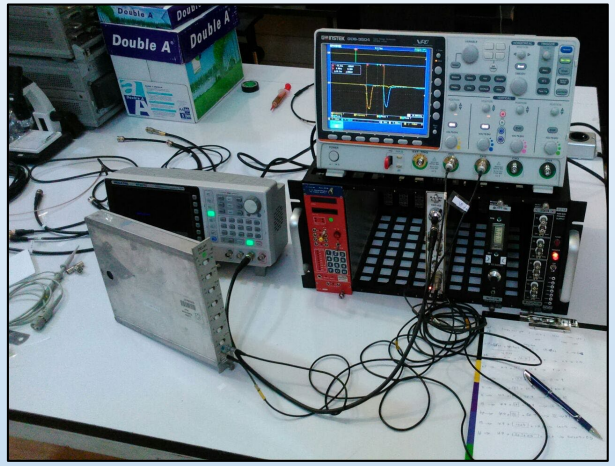
FEB Communication and Control

- ***New Link system Firmware***

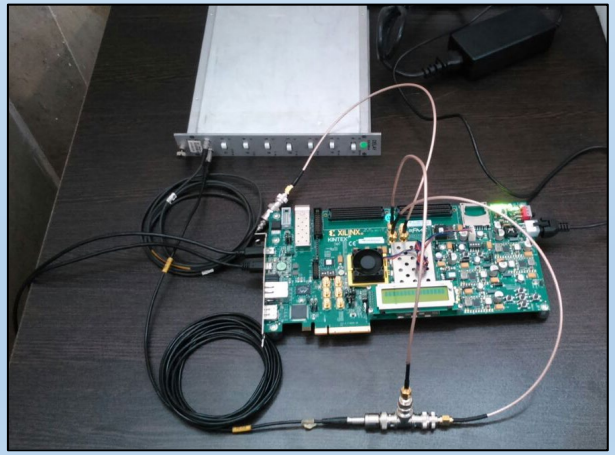
1. Control Software
2. TTC Generator
3. TX - LpGBT Protocol (Xilinx)
4. FEB Controller
5. TDC (1.56 ns)
6. TTC Decoder
7. Frame Generator
8. TTC Clock Recovery & Phase Shift
9. Multi Boot Remote Programming
10. Control/Diagnostic/ Histogramming (LB)
11. Ethernet LAN
12. DDR3 interface Controller
13. Jitter Cleaner (State Machine Controller)
14. Fixed Latency data transmission
15. Control/Diagnostic (CB)
16. Soft Error Mitigation Engine (SEM)
17. Triple Modular Redundancy (TMR)

Time to Digital Converter Performance

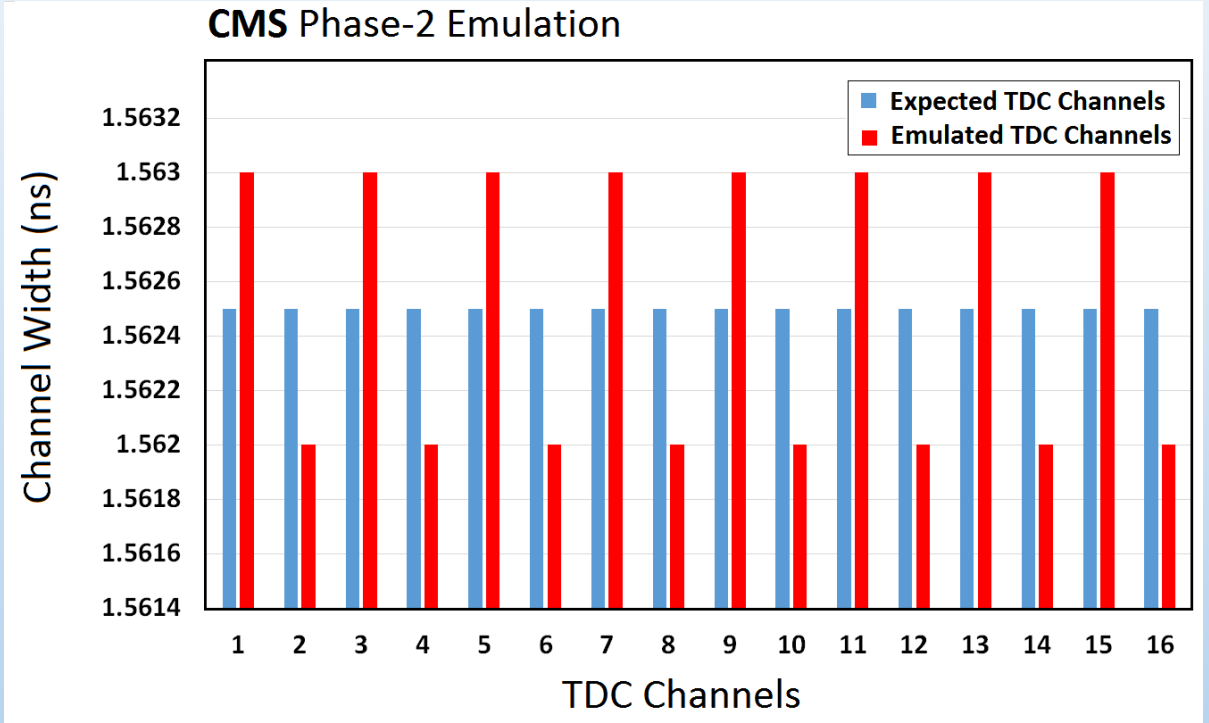
TDC 1.56 ns @ 160MHz / 640 MSPS



TDC Calibration test setup



TDC Performance measurement

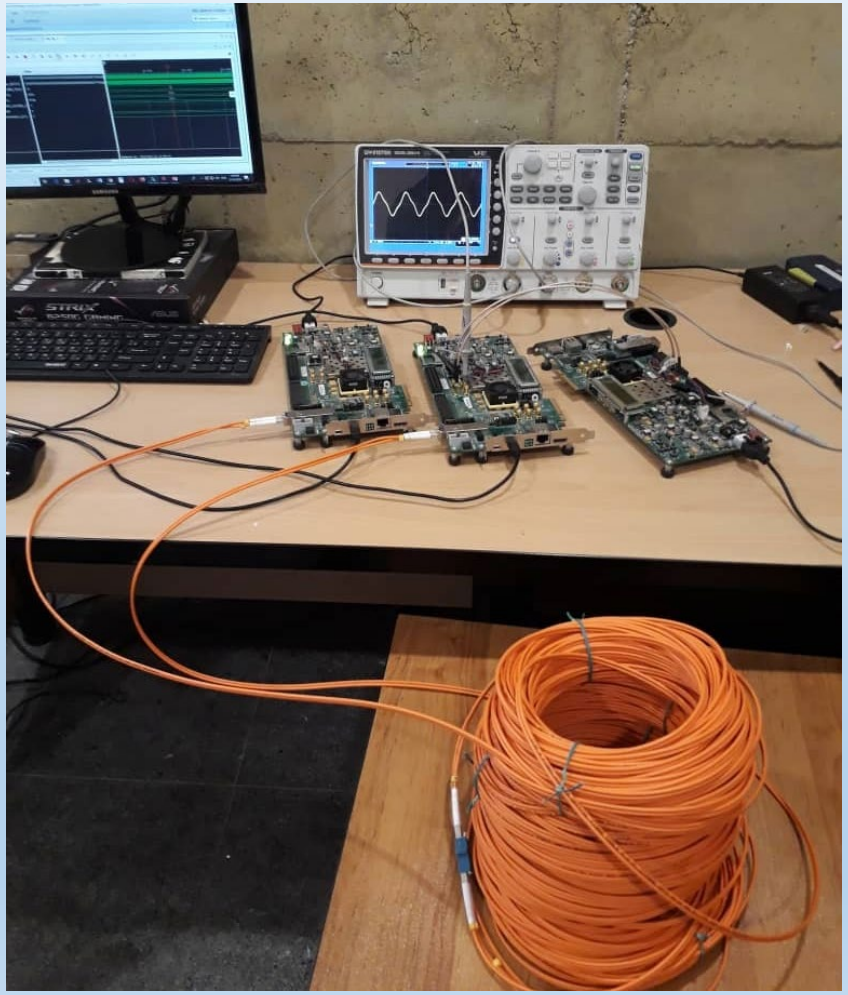


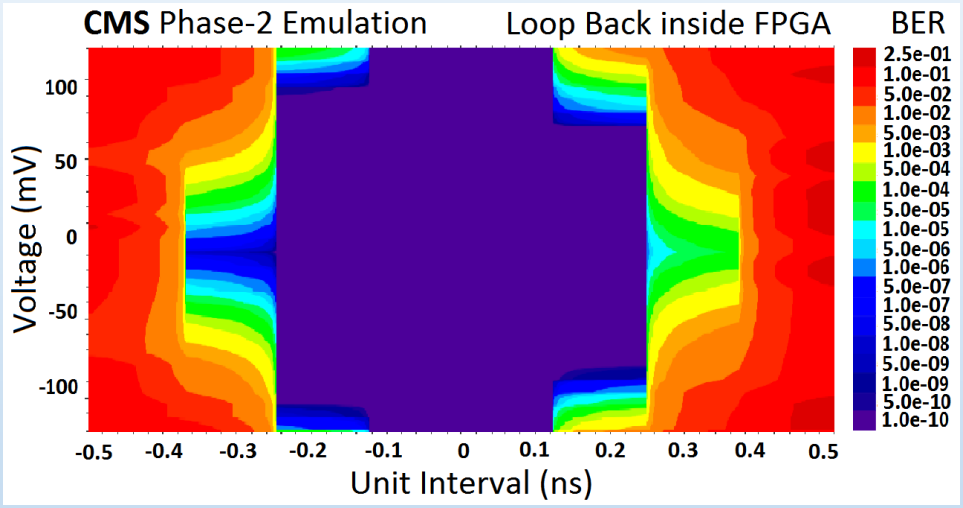
- ISERDES Based TDC
- FREQ. 160 MHz
- Sampling Rare 640 MSPS
- TDC Resolution 1.56 ns

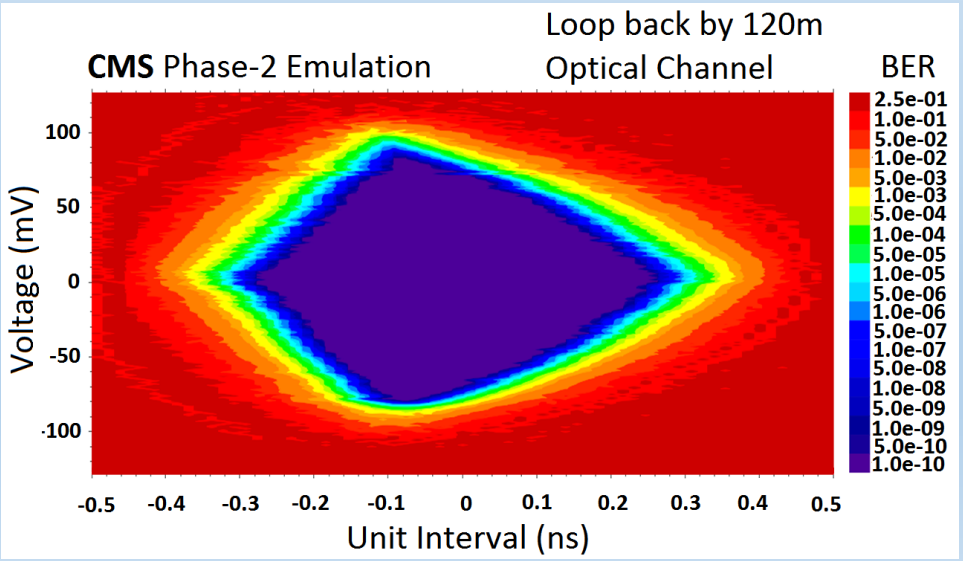
- DNL < ± 0.006 LSB
- INL_{max} < 0.01 LSB

High Speed Data Transmission – Optical Link

Fixed Latency GTX @ 10.24 Gbps



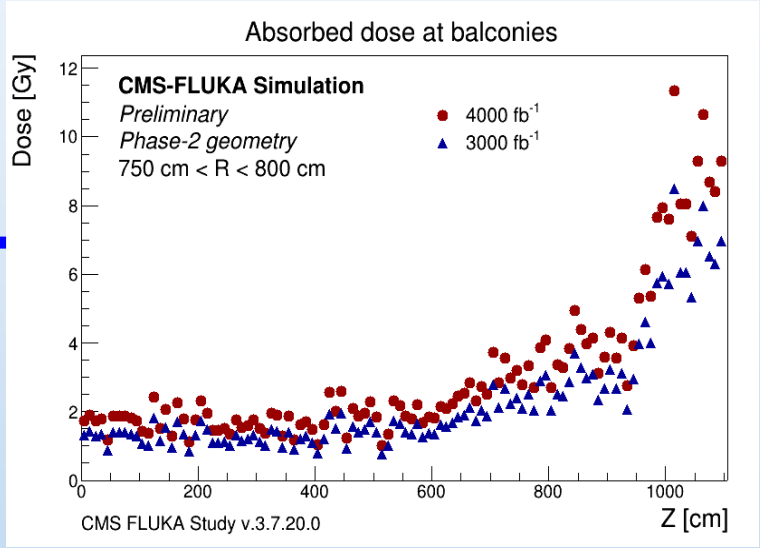




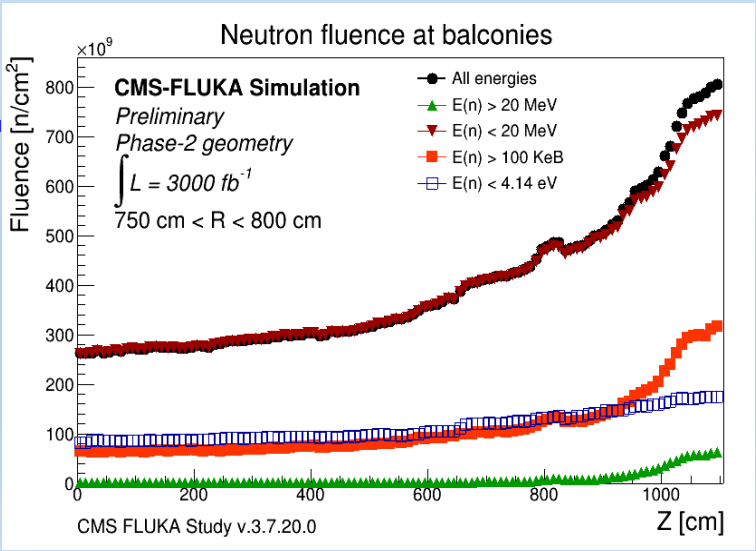
- (**Near-End**) Maximum achievable Opening eye for the Ideal Case (Loop back inside the FPGA1) is 55.56%
- (**Far-End**) Opening eye for the Real Case in which the data transmission will take by connecting two FPGAs through the 120 meters optical channel (OM2) is 50~55%.
- **Test Period is 48 hours and number of errors is Zero**

Radiation Consideration

- **The Link system will be installed on the Balcony of CMS (750 cm <R < 800 cm), where the rates are even lower than what we have at the periphery of the detector.**
- **Total Irradiation Dose** is **0.001-10 Gy** @ **3000 fb^{-1}**
- The new Link board components has been chosen from (Commercial-off-the-shelf) COTS which are validated for radiation at the level of **300 Gy**
- The FPGA TID **KINTEX-7 (XC7K160T)** is **3400-4500 Gy**



- **Neutron Flux** at the **CMS Balcony** is **1x10^{4} cm^{-2}s^{-1} @5 x 10^{34} cm^{-2}s^{-1}**
- **Neutron Fluence for 10 HL-LHC years is 1x10^{12} cm^{-2}**
- The Single Event upset (SEU) rate on **configuration memory** is **1 SEU every 413 sec.** and **1 SEU every 1695 sec. at Block RAM**
- **Scrub Time of entire FPGA (SEU detection and Correction) : 13 ms**
- **TMR and Configuration Scrubbing will mitigate the SEUs**

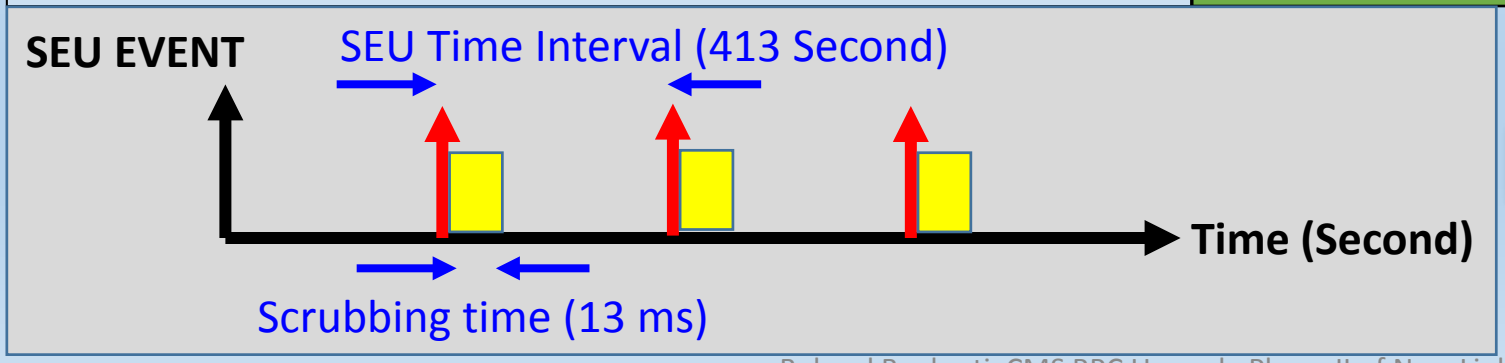


Radiation Consideration

Estimation of SEU on the KINTEX-7 XC7K160T Configuration and BRAM Memories

- *Number of Errors* = $\sigma_{CRAM} \times Flux \times T_{irrd} \times N_{CRAM}$
- σ_{CRAM} = Cross section of the Single Event upset of each bit at the configuration Memory ($cm^2\ bit^{-1}$)
- Flux = Number of Neutron pre square centimeter per second
- T_{irrd} = Irradiation Time
- N_{CRAM} = number of bits at the Configuration Memory

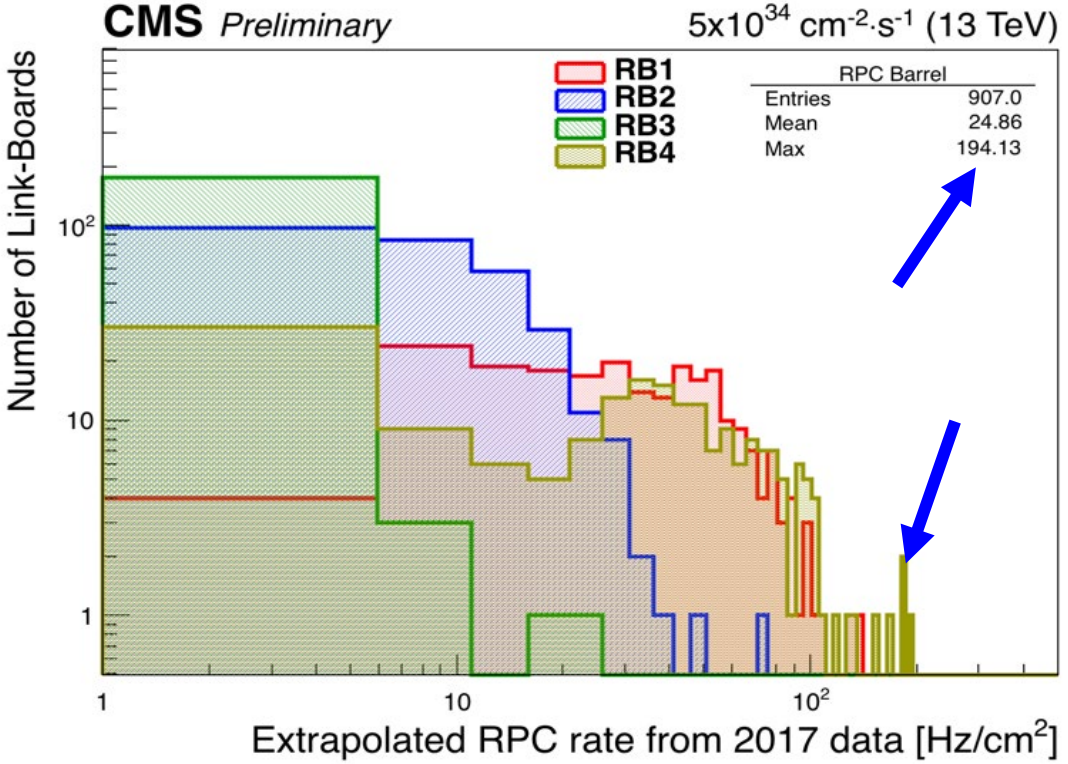
Integrated Errors due to SEU at the Configuration Memory of KINTEX-7 XC7K160T	Integrated Errors due to SEU at the BLOCK RAM Memory of KINTEX-7 XC7K160T
$\sigma_{CRAM} = 4.52 \times 10^{-15}\ cm^2\ bit^{-1}$ Flux = $1 \times 10^4\ cm^{-2}\ s^{-1}$ Time of Exposure = 1 sec N_{CRAM} = 53,540,576 bits	$\sigma_{BRAM} = 5.07 \times 10^{-15}\ cm^2\ bit^{-1}$ Flux = $1 \times 10^4\ cm^{-2}\ s^{-1}$ Time of Exposure = 1 sec N_{BRAM} = 11,700,000 bits
E_{CRAM} = 0.00242 at 1 second E_{CRAM} = 0.1452 at 1 minute E_{CRAM} = 8.712 at 1 hour	E_{BRAM} = 0.00059 at 1 second E_{BRAM} = 0.036 at 1 minute E_{BRAM} = 2.135 at 1 hour
1 SEU every 413 seconds	1 SEU every 1694 seconds



SEU Time Interval >> Scrubbing time

Hit Rate wrt Max expected Background Rate at HL-LHC

- Expected Max hit rate in Barrel in HL-LHC , safety factor 3: 600 cm^{-2} s^{-1}
- Biggest Strip surface area : 120 X 3 cm^2
- Average cluster size: -
- Number of Strip per chamber : 96
- Max Single hit in one LB per bx : 600 x (120 x 3) x 96 x 25 X 10^{-9}= 0.52 hit /LB x bx
- One Master Link Board collects hits of two adjacent Slave Link boards
- Max Single hit in one MLB per bx : 0.52 x 3 = 1.56 hit /LB x bx
- Size of hit information Package : 15 bits (Yellow box)
- MLB Max. Payload: 15 bits x 1.56 hits x 40 MHz = 0.936 Gbps
- *We foresee to send 232 bits/BX (for physics, already removed EOD and checksums) between MLB and RPC backend.*
- Maximum limit of single hits in one MLB = (one frame – overheads) / size of one hit = (256 – 46) / 15 = 14 hits

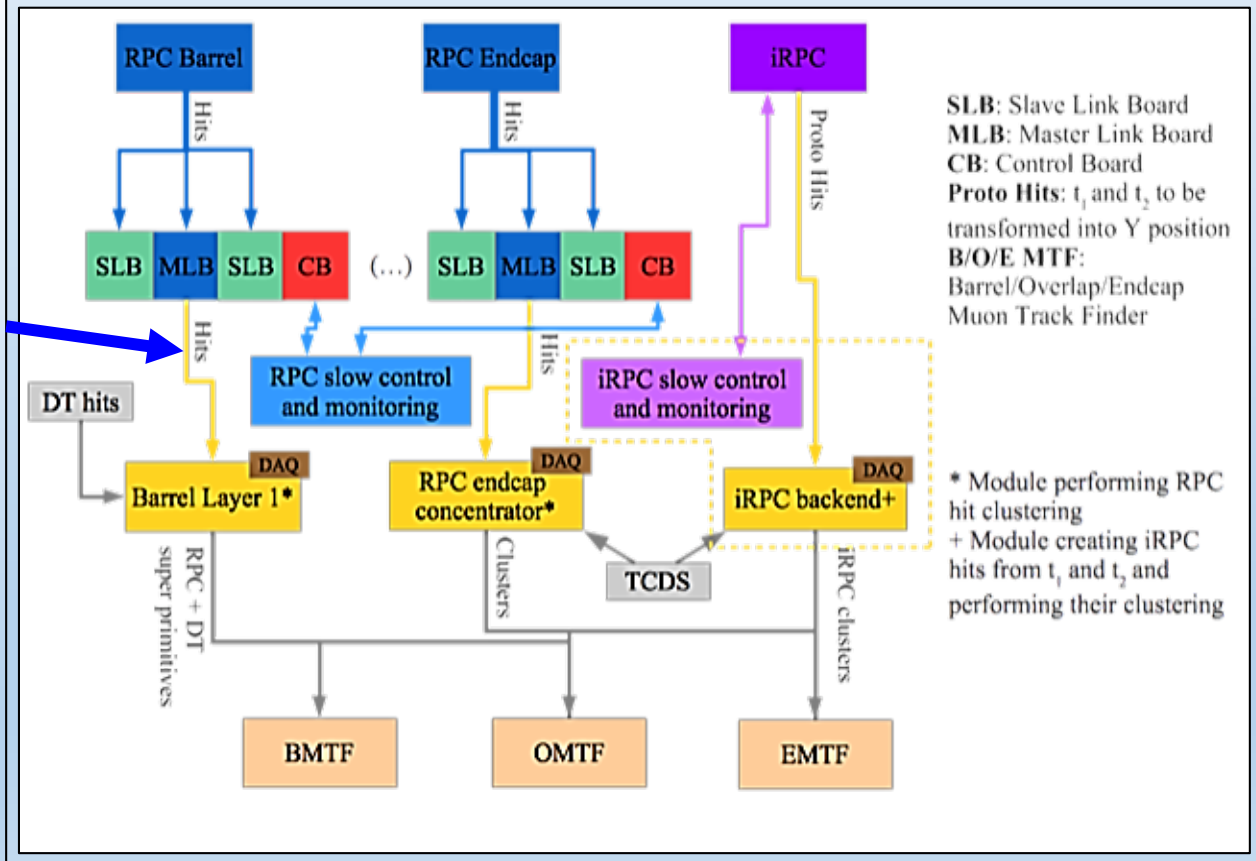


Items	Header + FEC	Number of Events (1… 14)	No. Strip (1..96)	Sub-bx	LB No. (0 … 8)	BCN	BC0	Partition	ID
Bit	24	4	7	4	4	12	1	3	2

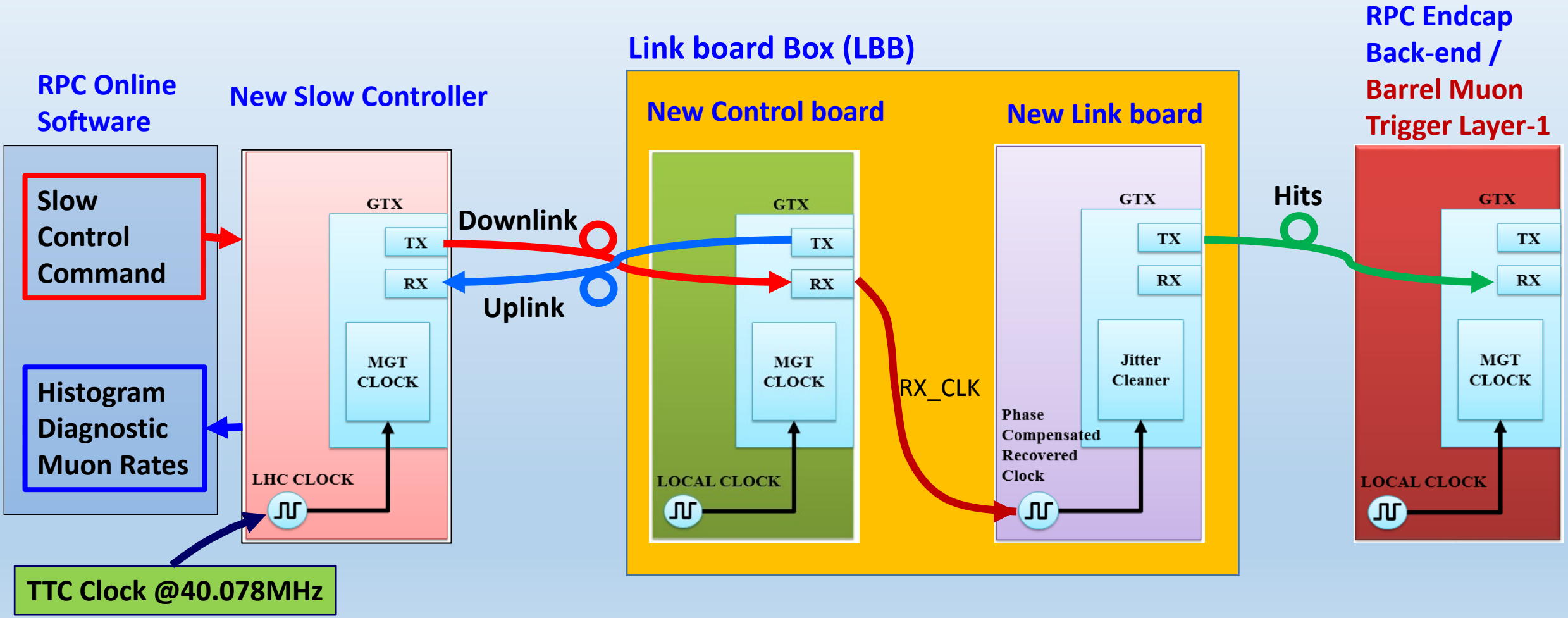
RPC Layer-1 Trigger Architecture and New Link system Hits Data Frame Format

Item	Header + FEC	Number of Hits (1..14)	No. Strip (1..96)	Sub-bx	LB No.	…	BCN	BC0	Partition delay	End of Data
Bit	24	4	7	4	4	…	12	1	3	2

- Each Frame has **256 bit** per each BX = 10.24 Gbps
- Data Frame format consists of **transceiver overheads**, **Number of hits**, **hit information package**, **timing information**, and a flag which shows status of transmission of current bunch cross in the sense that it is finished or not.
- **Transceiver overheads :** Header + FEC + End of data
- **Number of hits** shows the number of **hit information package** which exist inside the current frame information
- **Hit information Package** includes of the detail information of a hit such as **fired strip number** (1 to 96), timing information of a hit (**sub-bx**) which is a four bit number and shows the exact hitting time of fired strip with resolution of 1.56ns, and **the number of link board** as a location of fired strip corresponding to the RPC Chamber
- **Timing information** : using for synchronization and timing alignment of data transmission and contains a bunch cross number (12 bits) and bunch cross zero (BC0).
- **Partition delay:** In the rare physical events, it could be possible the number of hits will not fit inside one frame. In such cases, the reminder of hits information will be send on the consequent frames. The partition delay shows the number of consequent frames. In such frames, the number of bunch cross counter (BNC) is the same as last frame.



Control, Diagnostic and Synchronization of New Link System using New Slow Controller



New Slow Controller Functions

- **Downlink,** data direction from new Slow Controller to Control boards:
  - Number Links : 216 Downlinks (96 links Endcap CBs + 120 links Barrel CBs)
  - Link Protocol: LpGBT Protocol
  - Data Rate: 10.24/5.12/2.56 Gbps (All of this speeds are acceptable)
  - Fast trigger, Broadcast commands :
    - BC0, EC0, L1A, Hard Reset
  - TTC clocks (40.078 MHz)
  - Slow control Commands
    1. FEB Threshold setting (received from RPC online software)
    2. TTC fine skew adjustment (received from RPC online software)
    3. Open/Closed windows setting (received from RPC online software)
    4. FPGA configuration file (Remote Programming) (received from RPC online software)

- **Uplink,** data direction from Control boards to the new Slow Controller:
  - RPC strip hit Histogram
    - Counting Hits on every RPC strip
  - Timing Histograms
    - Counting Hits on all RPC strips in each Bunch Cross
  - Link System Status
    - Voltages, current, Temperature
    - Faults, SEU
    - Firmware Version Control

Summary

- Present Link system has been working well for more than 14 years (since 2006-2007)
- New Link system improves the muon hit time to 1.56 ns and using the high bandwidth of data transmission (10.24 Gbps) will increase the speed of data taking of RPC chambers
- In new link system, radiation mitigation is achieved by using the firmware TMR and internal scrubbing (SEM)
- The data transmission bandwidth of the new link system will cover the HL-LHC muon rates (with safety factor of 3)
- Muon hit date will send from link system through high speed data transmission optical link to the RPC Endcap back-end electronic and Barrel backend layer-1.
- Synchronization, control and diagnostic of the New link system will be done by using the new Slow Controller

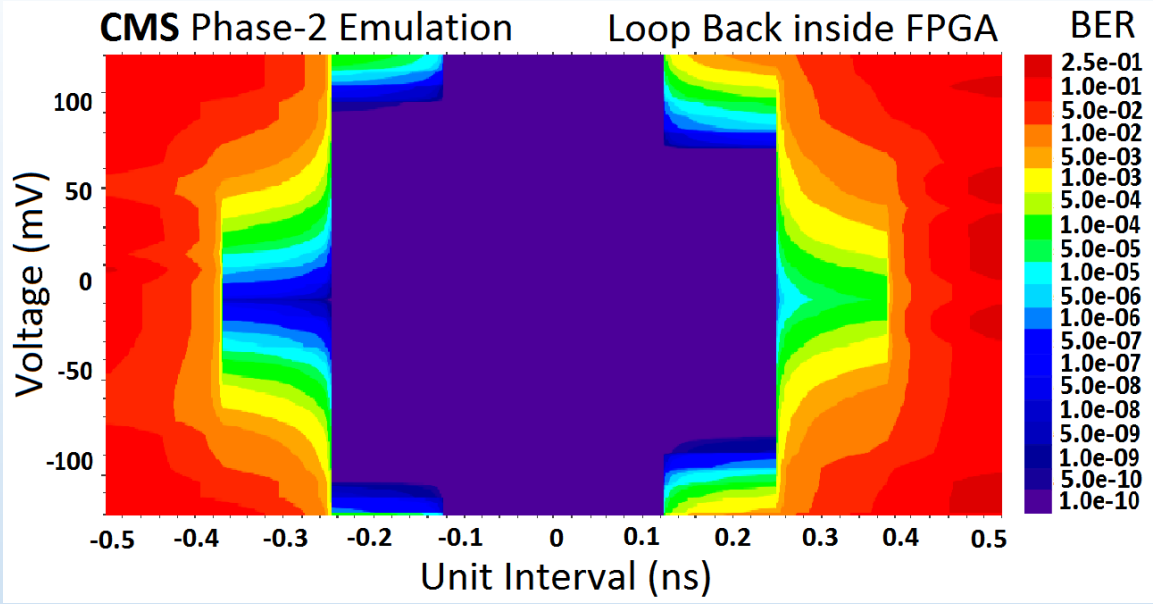
- **Thank you!**

High speed data transmission Performance @ 10.24 Gbps

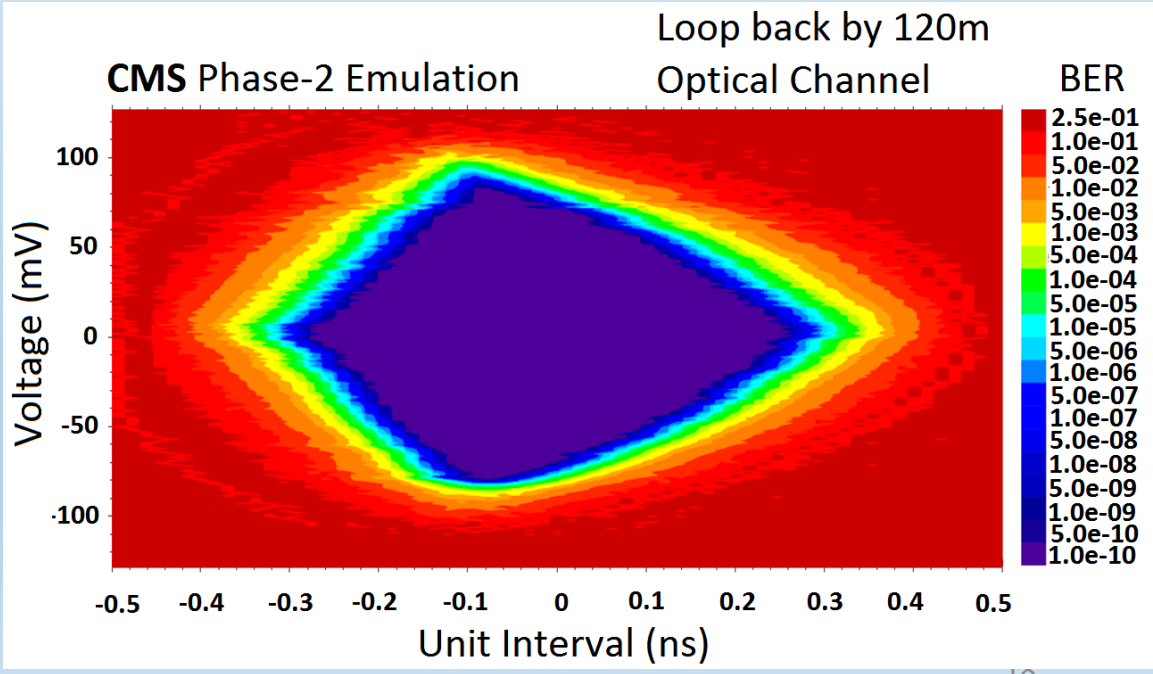
- Conceptually, we want the eye to be as “open” as possible, as a larger eye opening implies that we have more margin to the voltage and timing requirements. The eye must be **wide** enough to provide adequate time to satisfy the setup and hold requirement of the receiver, and have sufficient **height** to ensure that the voltage levels meet v_{ih} and v_{il} requirements in a system that may possess multiple sources of noise. This allows the receiver to resolve the input signals successfully into digital values.

- Maximum achievable Opening eye for the Ideal Case (Loop back inside the FPGA1) is 55.56%
  and the Opening eye for the Real Case in which the data transmission will take by connecting two FPGAs through the 120 meters optical channel is 50~55%.

- The Test Period is 48 hours and number of errors is Zero



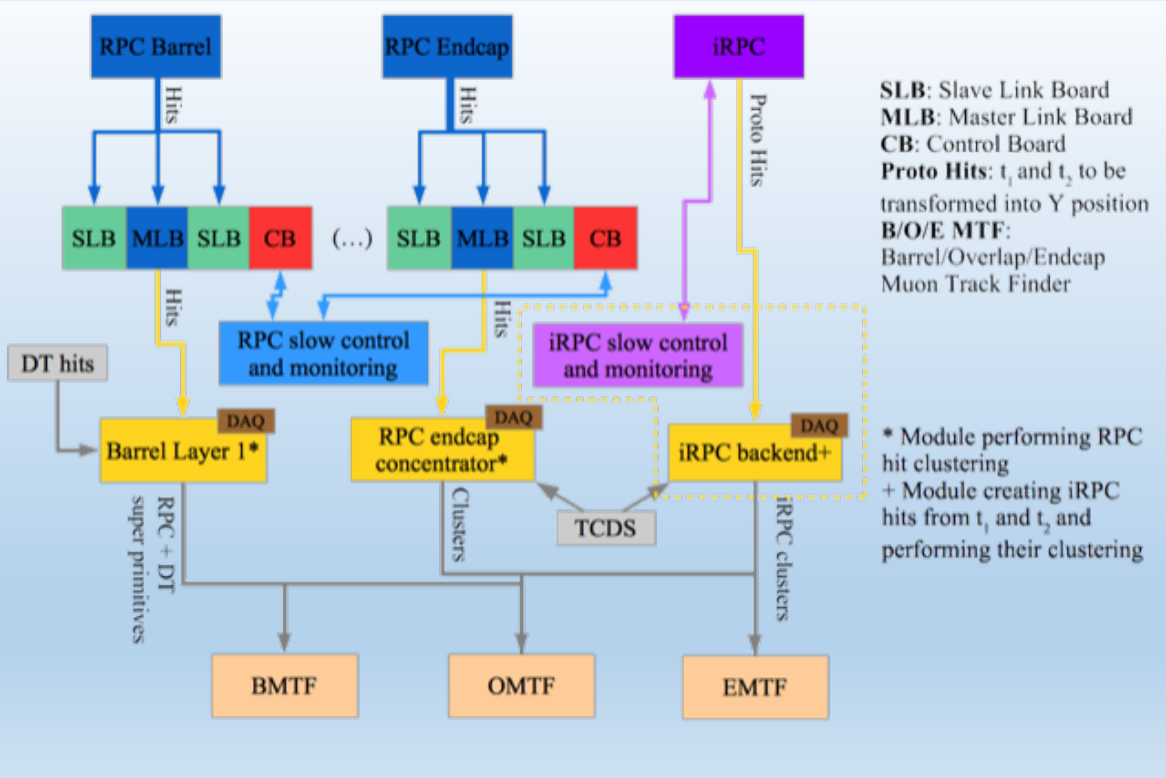
Opening eye – Ideal case



Opening eye – Real case

The RPC Architecture and L1T

	Link	Fiber	Type of Data	Max. Link Data Rate (Gbps)	Max. Payload per Link (Gbps)	Number of Links per sector	Max. Payload per Sector (Gbps)	Max. Payload (Gbps)
1- CB, Barrel	120	240	TTC, SC, Diag, Mon	2.56/ 5.12/ 10.24	-	-	-	-
2- CB, Endcap	96	192	TTC, SC, Diag, Mon	2.56/ 5.12/ 10.24	-	-	-	-
3- MLB, Barrel	300	300	Hit	10.24	1	5	5	300
4- MLB Endcap	192	192	Hit	10.24	0.63	2	1.26	121



Example-1

- Let assume that at BX = 23, three strips are fired as follow:
  - Hit-1 : Stripe No. 40, sub-bx = 1 , LB No. = 2
  - Hit-2 : Stripe No. 63, sub-bx = 16 , LB No. = 5
  - Hit-3 : Stripe No. 90, sub-bx = 7 , LB No. = 8

Item	Header + FEC 24 bits	Number of Hits (1..14) 4 bits	Strip No.(1..96) 7 bits	Sub-bx 4 bits	LB No. 4 bits	No. Strip (1..96) 7 bits	Sub-bx 4 bits	LB No. 4 bits	No. Strip (1..96) 7 bits	Sub-bx 4 bits	LB No. 4 bits	BCN 12 bits	BC0 1 bit	Partition delay 3 bits	End of Data 2bits
data	x	3	40	1	2	63	16	5	90	7	8	23	0	0	x

Example-2

- Let assume that at BX = 23, twenty strips are fired as follow:
  - Hit-1 : Stripe No. 40, sub-bx = 1 , LB No. = 2
  - ….
  - Hit-20 : Stripe No. 90, sub-bx = 7 , LB No. = 8

Item	Header + FEC 24 bits	Number of Hits (1..14) 4 bits	Strip No.(1..96) 7 bits	Sub-bx 4 bits	LB No. 4 bits	•••	No. Strip (1..96) 7 bits	Sub-bx 4 bits	LB No. 4 bits	BCN 12 bits	BC0 1 bit	Partition delay 3 bits	End of Data 2bits
data	x	14	40	1	2	…	x	x	x	23	0	0	x

Item	Header + FEC 24 bits	Number of Hits (1..14) 4 bits	Strip No.(1..96) 7 bits	Sub-bx 4 bits	LB No. 4 bits	•••	No. Strip (1..96) 7 bits	Sub-bx 4 bits	LB No. 4 bits	BCN 12 bits	BC0 1 bit	Partition delay 3 bits	End of Data 2bits
data	x	6	x	x	x	…	90	7	8	23	0	1	x

Slow Control, Downlink (BEE to CB)

- **Downlink, data direction from Back-end Electronics to Control boards:**
  - 216 Advanced links (96 links Endcap CBs + 120 links Barrel CBs)
  - LpGBT Protocol @ 10.24 Gbps

Item	Header + FEC [0..23]	L1A [24]	BC0 [25]	EC0 [26]	Hard Reset [27]	Command Type [28..30]	Command Value A [31..38]	Command Value B [39..54]	Command Value C [55..253]	End of Data [254, 255]
Bit	24	1	1	1	1	**3**	**8**	**16**	**199**	**2**

Command Types:

1. **TYPE0** : Operating Mode (Calibration, Link Board Setting, Control Board setting, Physics RUN, Standby)
2. **TYPE1** : FEB Parameter Setting / Verification
3. **TYPE2** : TTC fine skew adjustment
4. **TYPE3** : Coarse/Fine windows setting
5. **TYPE4** : FPGA Remote Programming
6. **TYPE5..TYPE7:** Reserved

Slow Control, Downlink (BEE to CB)

- **Downlink, data direction from Back-end Electronics to Control boards:**

Item	Header + FEC [0..23]	L1A [24]	BC0 [25]	EC0 [26]	Hard Reset [27]	Command Type [28..30]	Command Value A [31..38]	Command Value B [39..54]	Command Value C [55..253]	End of Data [254, 255]
Bit	24	1	1	1	1	**3**	**8**	**16**	**199**	**2**

Command Types:

TYPE0 : Operating Mode

Command Value A_L [31..34] (Target board)

Value A_L [31..34] = 0; CB
Value A_L [31..34] = 1; LB1
Value A_L [31..34] = 2; LB2
…
Value A_L [31..34] = 9; LB9

Command Value A_H [35..38] Command Value:

1. ***Value A_H [35..38] = 0;*** Calibration mode
2. ***Value A_H [35..38] = 1;*** Link Board Parameter Setting
3. ***Value A_H [35..38] = 2;*** Control Board Parameter setting
4. ***Value A_H [35..38] = 3;*** Physics RUN
5. ***Value A_H [35..38] = 4;*** Standby
6. ***Value A_H [35..38] = 5;*** Histogram
7. ***Value A_H [35..38] = 6;*** Diagnostic
8. ***Value A_H [35..38] = 7;*** Loopback
9. ***Value A_H [35..38] = 8;*** FEB Test
10. ***Value A_H [35..38] = 9..16 ;*** **Are Reserved**

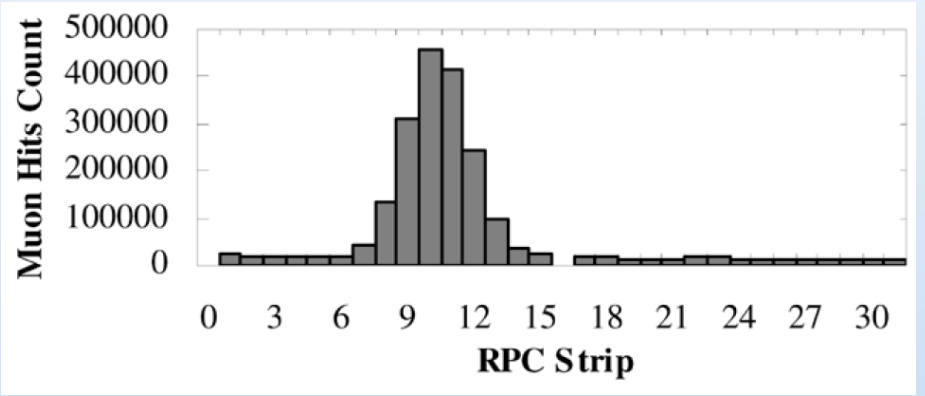
Slow Control, Uplink (CB to BEE)

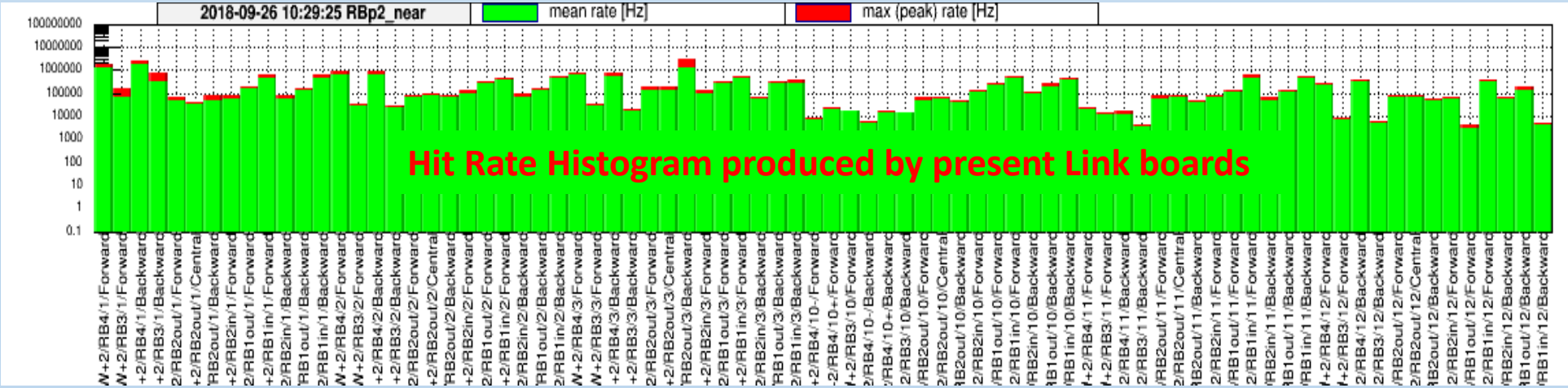
- **Uplink, data direction from Control boards to Back-end Electronics :**
  - **216 Uplinks (96 links Endcap CBs + 120 links Barrel CBs)**
  - **LpGBT Protocol**
  - **Downlink Speed: 10.24/5.12/2.56 Gbps (All of this speeds are acceptable)**
  - **FEC5**
  - **At any moment, a copy of received command from BEE and corresponding data or acknowledge from CB will send back to the BEE**

Item	Header + FEC [0..23]	L1A [24]	BC0 [25]	EC0 [26]	Hard Reset [27]	Command Type [28..30]	Command Value A [31..38]	Command Value B [39..54]	Command Value C [55..253]	End of Data [254, 255]
Bit	24	1	1	1	1	3	8	16	199	2

RPC strip hit Histogram

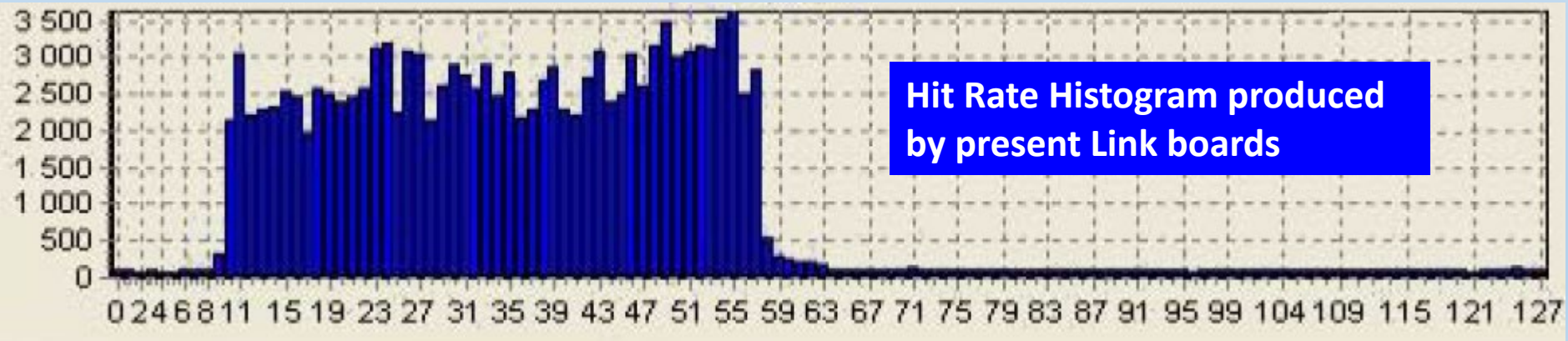
- **Counting Hits on every RPC strip**
  - On each LBs two **multichannel counters** have been implemented
  - Adjustable window and Full window
  - The buffer size of each Multichannel counter is 96 x 32 bits
  - In total at each CB more than 9 (LBs)x 2 (MCC) X 96 X 32 bits
    - **Total Buffer Size = 178176 bits ~ 180 kbits**
  - Reading from these buffers are not time critical





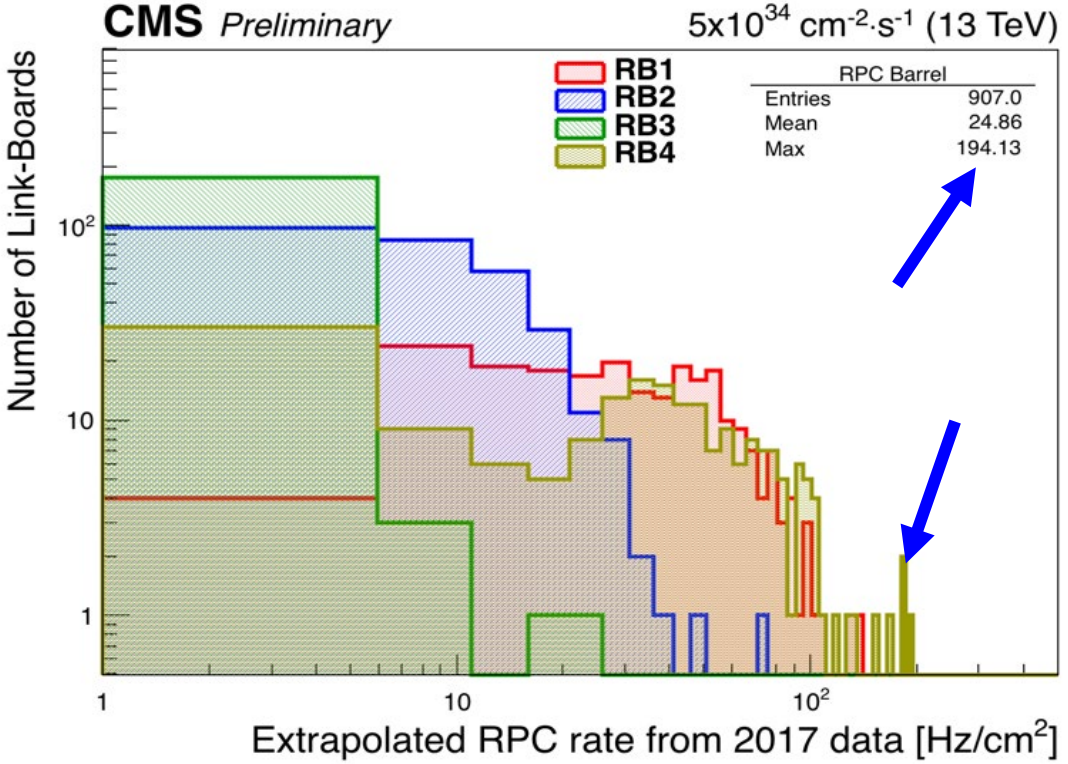
Timing Histograms

- **Counting Hits on all RPC strips in each Bunch Cross**
  - On each LBs one 32 bit counter has been implemented
  - At each BX, the content of last BX will store at the FIFO
  - The size of FIFO is 128 x 32 bits
  - In total at each CB timing histogram buffer
  - 9 (LBs)x 1 (Timing Histogram) X 128 X 32 bits
    - Total Buffer Size = 10368 bits ~ 10.4 kbits
  - Reading from these buffers are not time critical



MLB Single Hit Rate wrt Max expected Background Rate at HL-LHC in Barrel

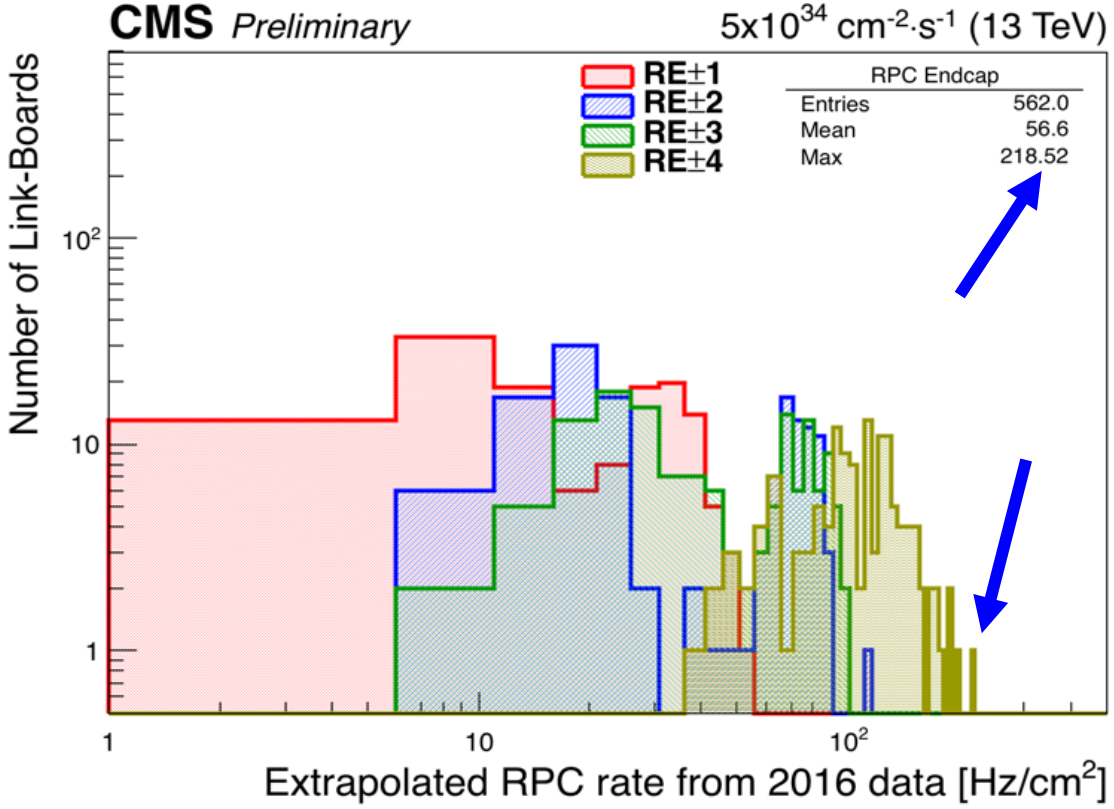
- Expected Max hit rate in Barrel in HL-LHC , safety factor 3: 600 cm^{-2} s^{-1}
- Biggest Strip surface area : 120 X 3 cm^2
- Average cluster size: -
- Number of Strip per chamber : 96
- Max Single hit in one LB per bx : 600 x (120 x 3) x 96 x 25 X 10^{-9}= 0.52 hit /LB x bx
- One Master Link Board collects hits of two adjacent Slave Link boards
- Max Single hit in one MLB per bx : 0.52 x 3 = 1.56 hit /LB x bx
- Size of hit information Package : 15 bits (Yellow box)
- MLB Max. Payload: 15 bits x 1.56 hits x 40 MHz = 0.936 Gbps
- *We foresee to send 232 bits/BX (for physics, already removed EOD and checksums) between MLB and RPC backend.*
- Maximum limit of single hits in one MLB = (one frame – overheads) / size of one hit = (256 – 46) / 15 = 14 hits



Items	Header + FEC	Number of Events (1… 14)	No. Strip (1..96)	Sub-bx	LB No. (0 … 8)	BCN	BC0	Partition	ID
Bit	24	4	7	4	4	12	1	3	2

MLB Single Hit Rate wrt Max Expected Background Rate at HL-LHC in Endcap

- Expected Max hit rate in Endcap in HL-LHC , safety factor 3: 700 cm^{-2} s^{-1}
- Biggest Strip surface area : 66 X 3.125 cm^2
- Average cluster size: -
- Number of Strip per chamber : 96
- Max Single hit in one LB per bx : 700 x (66 x 3.125) x 96 x 25 X 10^{-9} = 0.35 hit /LB x bx
- One Master Link Board collects hits of two adjacent Slave Link boards
- Max Single hit in one MLB per bx : 0.35 x 3 = 1.05 hit /LB x bx
- Size of event : 15 bits (Yellow box)
- MLB Max. Payload: 15 bits x 1.05 hits x 40 MHz = 0.63 Gbps
- *We foresee to send 232 bits/BX (for physics, already removed EOD and checksums) between CB and RPC backend.*
- Maximum limit of single hits in one CB = (one frame – overheads) / size of one hit = (256 – 46) / 15 = 14 hits



Items	Header + FEC	Number of Events (1… 14)	No. Strip (1..96)	Sub-bx	LB No. (0 … 8)	BCN	BC0	Partition	ID
Bit	24	4	7	4	4	12	1	3	2