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Development of high resolution TDC for RPC new link system

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In the CMS experiment, RPCs, which have an excellent intrinsic resolution within a few nanoseconds for double-gap chambers, are mainly used for accurate timing and fast triggering. This particularly allows for the identification of corresponding bunch crosses. However, since the data-taking chain and DAQ system record the hit time within 25 ns, the intrinsic time resolution of RPCs is thus not fully utilized. One of the main goals in upgrading the link system is to improve the timing resolution of the Muon hits at the level of RPC intrinsic resolution. To serve this goal, a 96-channel Time-to-Digital Converter (TDC) was implemented into a Xilinx Field-Programmable Gate Array (FPGA). The TDC was designed based on the combination of the logic elements with the uniform and solid digital Input Serializer and Deserializer (ISERDES) primitives inside the FPGA. Each TDC channel comprised of 16 bins where each bin had a time scale of one sixteenth of the 25 ns. The experimental results showed that there existed a 1.56 ns resolution for the implemented TDC channels, and that the non-linearity errors within the bins were well below 0.006 LSB and 0.01 LSB for the differential non-linearity and integral non-linearity, respectively.

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