Development of high resolution TDC for RPC new link system

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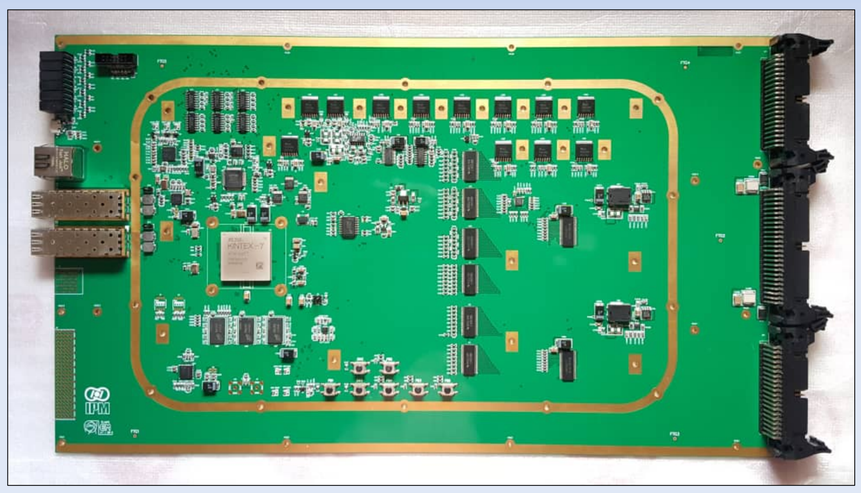
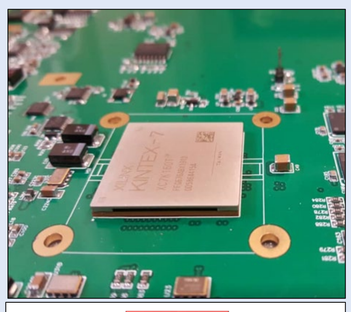
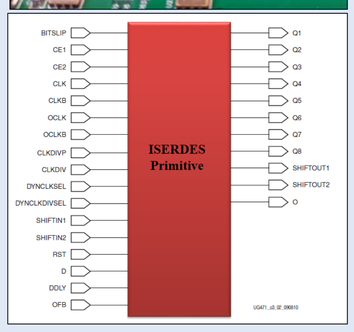
Abstract

In the CMS experiment, RPCs, which have an excellent intrinsic resolution within a few nanoseconds for double-gap chambers, are mainly used for accurate timing and fast triggering. This particularly allows for the identification of corresponding bunch crosses. However, since the data-taking chain and DAQ system record the hit time within 25 ns, the intrinsic time resolution of RPCs is thus not fully utilized. One of the main goals in upgrading the link system is to improve the timing resolution of the Muon hits at the level of RPC intrinsic resolution. To serve this goal, a 96-channel Time-to-Digital Converter (TDC) was implemented into a Xilinx Field-Programmable Gate Array (FPGA). The TDC was designed based on the combination of the logic elements with the uniform and solid digital Input Serializer and Deserializer (ISERDES) primitives inside the FPGA. Each TDC channel comprised of 16 bins where each bin had a time scale of one sixteenth of the 25 ns. The experimental results showed that there existed a 1.56 ns resolution for the implemented TDC channels, and that the non-linearity errors within the bins were well below 0.006 LSB and 0.01 LSB for the differential non-linearity and integral non-linearity, respectively.



Details of the design





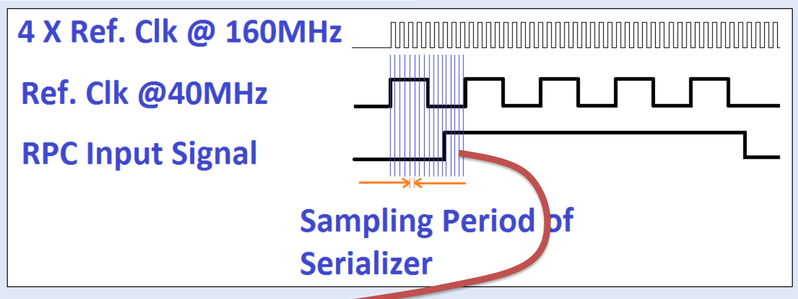
The Time-to-Digital Converter (TDC)

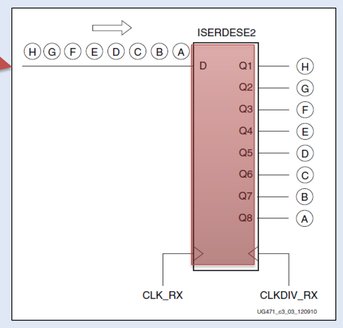
The main block element inside the TDC of the new link system is the Input Serializer and de-Serializer which is known as ISERDES primitive.

The ISERDESE in 7 series FPGAs is a dedicated serial-to-parallel converter with specific clocking and logic features designed to facilitate the implementation of high-speed source synchronous applications. The ISERDESE avoids the additional timing complexities encountered when designing deserializers in the FPGA fabric.

The ISERDES could sets and works at four different clocking mode: **1) Networking Interface, 2) Memory Interface, 3) Memory QDR interface and 4) Oversampling Interface**.

Among all of these mode, the **Oversampling mode** is just need lowest frequency and it could be digitizing the incoming signals at four times of its input reference clock.

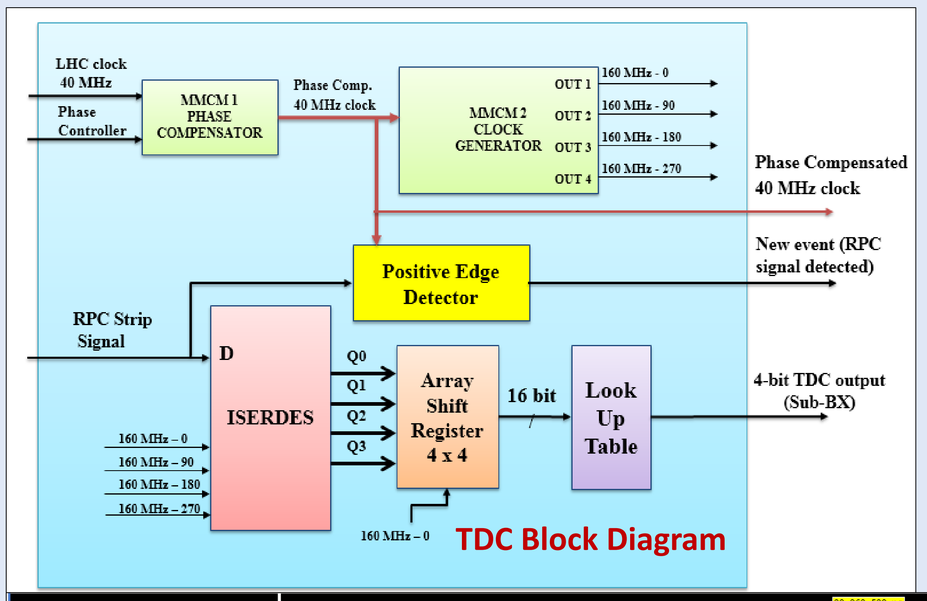


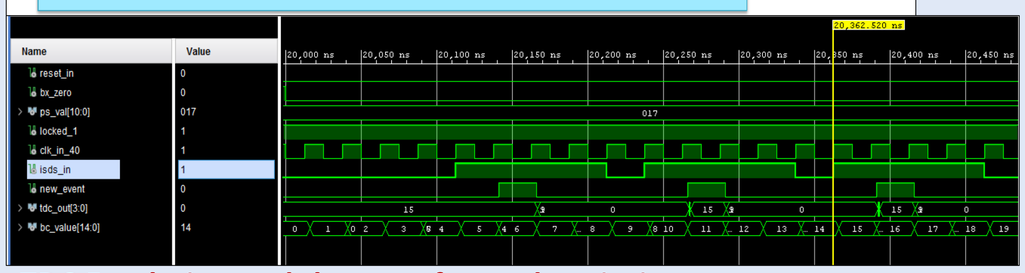


TDC sampling rate and time Resolution

The incoming RPC signals is digitized by using the ISERDES primitive inside the FPGA. The clock source of digitization comes from of the main LHC clock at the frequency of 40 MHz. The ISERDES could works at four different modes. We set its mode at **oversampling mode** just to reduce the input clock frequency which lead to reducing the timing constraint at the chip level. In this mode, the ISERDES needs four input clocks with four specific phase differences. These input clocks have been provided by the Mixed Mode Clock Management Unit (MMCM) inside the FPGA at the frequency of 160 MHz. Therefore, the ISERDES could digitized the incoming signals at the rate of four times of input clocks (**640 MSPS**).

In this way the sampling rate of the TDC core sets to the 640 MSPS which is corresponding to the 1.56 ns sampling time. It worth noticing that the sampling rate of the digitizer specify the time resolution of the TDC channels. In our case, the time resolution of each TDC channel will be the same as sampling time of serial digitizer at **1.56 ns**.



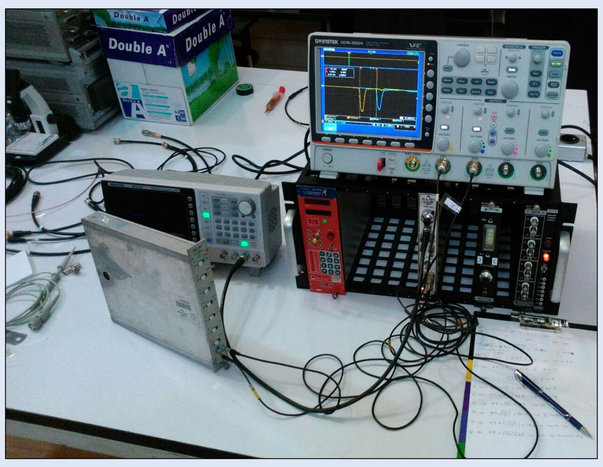


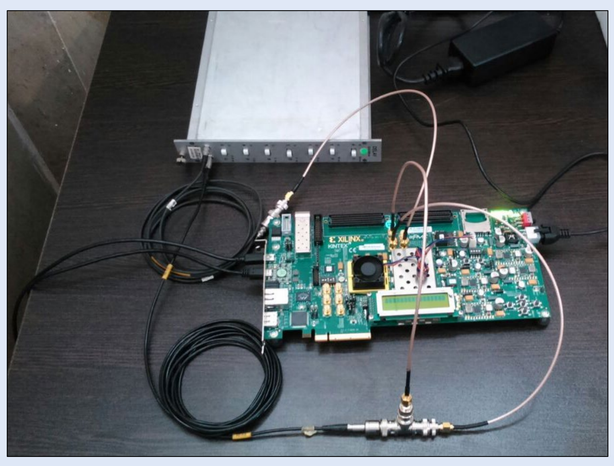
TDC Emulation and the waveforms description

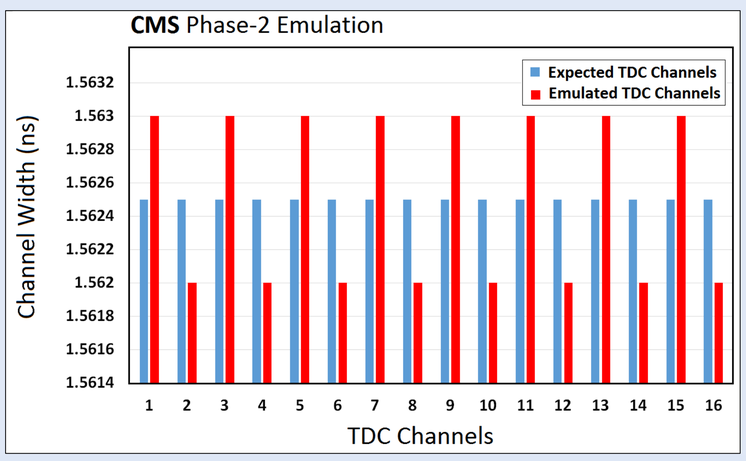
1) reset_n: Global Reset, **2) bx_zero:** Bunch counter reset, **3) ps_value[10:0]**: Clock Phase shift, **4) locked_1:** Mixed mode clock management (MMCM) stabled and locked, **5) Clock_in_40:** Reference clock 40 MHz, **6) isds_in:** TDC (ISERDES) input, **7) new event:** New Event detected, **8) tdc_out[3:0]**: TDC Output data is ready, **9) bc_value[14:0]:** Bunch Crossing Counter (BCN)

To check and justify the behavior and functionality of the TDC, nine important signals of the final TDC's firmware have been chosen for emulation. The **"reset_n"** is used to reset the entire FPGA digital resources. The **"bx_zero"** signal is used to reset the Bunch Crossing Counter (BCC) inside the FPGA. The **"ps_value[10:0]"** is a 11-bit number which is used to insert the phase shift value into the TDC core. The frequency locked state of the MMCM is shown by the **Locked_1 signal**. The **clock_in_40** is the input reference clock (LHC 40MHz) of the TDC. The input port of the TDC is marked by the **isds_in** signal. The stimulus RPC signals is feed into this port. Whenever, the rising edge of input signal detected by the TDC, the **new event** signal will be set to one. After that the TDC output value which is a number between 0 to 15 will set at the **tdc_out[3:0]** signal. The content of bunch cross counter is set on the **bc_value[14:0]** signal.

Tests and Results







- The Time to Digital converter (TDC) is used for measuring the Muon hit time by dividing one bunch crossing to 16 equal channels and check to see that in which channel the rising edge of RPC signal will fit. Therefore, all TDC channels should be the same size which is known as channels uniformity.
- In order to check the TDC channels uniformity, a test setup has been prepared. In the test setup, the reference signal which is generated by the evaluation board is sent to the programmable delay line module to make an specific delay with respect to the reference signal. Then, the delayed signal is applied to the TDC input channel to check the TDC behavior and its channel resolution. As the plot shows, expected channel size versus the measured value of TDC after post-implementation into the FPGA shows the time resolution of 1.56 ns for all sixteen channels. In this way, it will be expect that the TDC resolution for all sixteen channels are the same and uniform.

Conclusion

In this work, a New version of Time-to-Digital Converter (TDC) has been proposed and implemented into the Kintex7 FPGA. The main core of the TDC is a high speed Serializer and de-Serializer (ISERDES) which was fabricated in the FPGA by the factory. Based on this idea, the clocking mode of ISERDES is set to the oversampling mode to reduce the complexity of timing constraint, increase the overall sampling rate and reduce the power consumption of TDC. The final emulation shows the timing resolution of all TDC channels is uniformed and fixed at 1.56 ns.