# Front-End electronics for CMS iRPC detectors



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## Outline

# Introduction

- Motivation and Goals of Research & Development
  - CERN CMS RPC upgrade project
  - Rate Simulation

# Prototype of iRPC

- Layout of improved Resistive Plate Chamber
- RETURN & COAX redout PCB-strip panels
- Front-End Electronic: ADC and TDC

# **Test of iRPC**

- Trigger for study perfomence of chambers
- Description of the tests for prototypes
- Output Data from iRPC
- Cluster Size and Clustering Algorithm
- Study of time resolution
- Efficiency study
- Trigger Setup in GIF++
- GIF++: Study of rate capability

# Summary

## **CMS iRPC Upgrade Project**





- improve on the То muon detector performance.
- To improve on the muon trigger efficiency at high  $1.8 < |\eta| < 2.4$



### iRPC should be able to withstand high particle rates with safety factor: 2kHz\*cm<sup>-2</sup>





#### RPC Expected hit rate in RE4/1

### Layout of improved Resistive Plate Chamber





Determine position along a strip of the hit with a resolution given essentially by the readout timing.

**Time Difference of Arrival Method** 



## **RETURN & COAX redout of PCB-strip panels**

**Solution COAX** Connect with coaxial cables. Cable impedance = 50  $\Omega$ .. **Solution RETURN** Connect with a return line within PCB (same impedance 45  $\Omega$ ).



To minimize signal reflections, the stripline impedance must be controlled up to the asic. 3 methods were used to measure strip impedance :

· Direct measurement of line parameters with a RLC meter (at 2MHz)

Side	C <sub>p</sub> (pF)	G <sub>p</sub> (µS)	L <sub>s</sub> (nH)	R <sub>s</sub> (mΩ)	Z <sub>c</sub> (Ω)
Wide	244	934	482	467	43,5
Narrow	244	934	487	461	44

· Direct measurement with potentiometric line adaptation





### ASIC PETIROC: Analog Digital Converter

![](_page_5_Figure_2.jpeg)

The Front-End Electronics Board (FEB) that hosts one PETIROC ASIC and the FPGA that includes the TDC and the schematics of the PETIROC ASIC

![](_page_5_Figure_4.jpeg)

![](_page_5_Figure_5.jpeg)

![](_page_5_Figure_6.jpeg)

### FPGA Cyclone: Titme Digital Converter

Block diagram of the time-to-digital converter implemented in a single FPGA device.

![](_page_5_Figure_9.jpeg)

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# Trigger for study perfomence of chambers

![](_page_6_Figure_1.jpeg)

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![](_page_6_Figure_2.jpeg)

### **Output data from iRPC**

![](_page_7_Figure_1.jpeg)

### **Cluster Size and Clustering Algorithm**

![](_page_8_Figure_1.jpeg)

### Time Resolution along the strip and absolute time resolution

![](_page_9_Figure_1.jpeg)

# Trigger Setup in GIF++

![](_page_10_Figure_1.jpeg)

![](_page_10_Figure_2.jpeg)

![](_page_10_Figure_3.jpeg)

### **Efficiency study**

![](_page_11_Figure_1.jpeg)

![](_page_11_Figure_2.jpeg)

**EFFICIENCY** ε: Muon Efficiency;

![](_page_11_Figure_4.jpeg)

*N*<sub>trig</sub>: Number of triggers; *N*: Number of events for which at least a strip is fired (both ends);

 $N_{bkg}$ : Estimated by counting events for which at least a strip is fired (both ends) in a time interval of the same length but uncorrelated with the trigger.

#### **HIGH VOLTAGE EFFECTIVE**

Effective HV takes into account the change in pressure and temperature with respect to an HV reference value  $V_0$  at given pressure  $P_0$  and temperature  $T_0$ .

$$HV_{app} = \beta HV_{eff} = HV_{eff} \left( (1 - \alpha) + \alpha \frac{P}{P_0} \frac{T_0}{T} \right)$$

14 TBq 137Cesium is used in GIF++ with different attenuation coefficients is used to obtain different gamma irradiation levels.

To test our chambers a rate of up to 2 kHz·cm<sup>-2</sup> needs to be seen in our chamber.

![](_page_12_Figure_3.jpeg)

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# FEBv0 tested in 2018 (Cosmic, GIF++, H2line)

![](_page_13_Picture_2.jpeg)

A board that contains:

- > 1 PETIROC2A ASIC + FPGA CYCLONE 2
- Ethernet-based communication was conceived to read out the strips FR4 PCBv.0 (44 strips) THR=~80fC with DeadTime=10ns

Efficiency at ~2kHz cm<sup>-2</sup> of background 95% Resolution: Along strip ~180ps;

Absolute ~370ps

# FEBv1 is testing from spring 2019 (Cosmic, GIF++)

![](_page_13_Picture_9.jpeg)

This was intended to come closer to the final board to be compatible with CMS DAQ: > 2 petiroc2A(B) + FPGA CYCLONE V

Ethernet-based communication is used to read out the strips FR4 PCBv.1 (48 strips)

THR=~50fC with DeadTime=10ns

### Summary of test for only FEBv1.1 in GIF++

This study can only be considered in terms of the behavior of electronics because level of **background rate on study area ~10 time smaller than average value of rate**.

![](_page_14_Figure_2.jpeg)

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- A method was proposed for measuring the efficiency of the detector when using signals from two ends of the strip.
- A new clustering algorithm using time information was proposed and successfully tested.
- The linearity of the TOA time measurements and the time resolution of the TOA are verified on CERN SPS-H2 beamline tests. Along strip resolution ~180ps.
- Calculated absolute time resolution ~370ps for a 2-gap chamber.
- Measurements of the detector characteristics equipped with FEBv0 were carried out at the required rate of 2kHz\*cm<sup>-2</sup> of the background. The efficiency of more than 95% was obtained. Also, we showed that FEBv1 (only FEBs performance study) has the same characteristics as FEBv0.

![](_page_16_Picture_0.jpeg)

# **Thank for Your Attention!**

# Any questions:

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# **Additional material**

# Trigger Setup in GIF++

![](_page_19_Figure_1.jpeg)

Resistive plate chambers (RPC) are fast gaseous detectors that provide a muon trigger system

### Two parallel plates:

positively-charged anode negatively-charged cathode both made of a very high resistivity and separated by a gas volume.

![](_page_20_Picture_4.jpeg)

### Gas mix: 95.2% C2H2F4, 4.5% i-C4H10, and 0.3% SF6

For applications where high background rates are expected, chambers have to be operated in avalanche mode in order to keep the total produced charge low with benefits in terms of aging and rate capability. This is usually obtained with suitable gas mixtures that prevents the transition from avalanche to streamer modes keeping the detection efficiency.

![](_page_20_Figure_7.jpeg)

The thinner gap in the double gap RPC detector & comparison between iRPC and RPC

### 1.4mm GAPs

![](_page_20_Figure_10.jpeg)

Figure 1.18: Efficiency (left) and average cluster size (right) at the working voltage, as a function of the cluster rate for the 1.4 mm double-gap RPC. The data were measured at the fixed threshold of  $300 \ \mu$ V.

### **Electronic Petiroc: Noise**

![](_page_21_Figure_1.jpeg)

6.6 0

```
EFFICIENCY
```

 $\varepsilon = \frac{\frac{N}{N_{trig}} - \frac{N_{bkg}}{N_{trig}}}{1 - \frac{N_{bkg}}{N_{trig}}}$ 

ε: Muon Efficiency;
N<sub>trig</sub>: Number of triggers;
N: Number of events for which at least a strip is fired (both ends);

 $N_{bkg}$ : Estimated by counting events for which at least a strip is fired (both ends) in a time interval of the same length but uncorrelated with the trigger.

 $P = P_mu + P_bkg - P_mu$ .  $P_bkg$  (this is the probability formula when you have sets that are not independent or disjoint) where P = N/Ntrig,  $P_mu$  is the efficiency and  $P_bkg = N_bkg/Ntrig$  with  $N_bkg$  is estimated using a time interval with the same length but placed at a time uncorrelated with the muon trigger.

From above the exact formula is then: P\_mu = (P-P\_bkg)/(1-P\_bkg)

## **Description**

In the beginning, we had a problem with firmware for new FEBs that allows us to work about 100fC threshold. For this configuration, we did a study of efficiency for two different positions. The results of this study are the loss of signal from propagation that could be shown with the degradation of efficiency for LR.

In this case, we decided to keep a worse position for all the next steps.

![](_page_23_Figure_4.jpeg)

![](_page_23_Figure_5.jpeg)

### **PETIROC2B**

A new version of PETIROC was conceived and produced with the aim to reduce the threshold while keeping a good timing.

Retriggering problems are solved by using a combination of **Raz\_ch** and **Val\_ev** signals at **Ivl 50fC**.

Val evt = 5+5 ns

Raz chn= 5 ns

![](_page_24_Figure_4.jpeg)

![](_page_24_Figure_5.jpeg)

### **Examples of Re-triggering**

### **Rate defenition**

 $\begin{aligned} hitRate &= \frac{numberOfHits}{surface * time}, where \\ numberOfHits - number of triggered channels of FEBs of one run; \\ sufrace - active PCB zone; \\ time - collection time : (timeWindow * numberOfEvents). \end{aligned}$ 

$$RATE_{HVeff} = \frac{ClusterRate}{efficiency_{HVeff}}$$

$$cluster Rate = \frac{numberOfClusters}{surface * time}, where$$
$$numberOfClusters - number of clusters of one run;$$
$$sufrace - active \ PCB \ zone;$$
$$time - collection \ time : \ (timeWindow * numberOfEvents).$$

![](_page_25_Figure_4.jpeg)

1000&trigsThr\_1&window\_-4000.00\_0.00ns&LRtimeProfile

![](_page_25_Figure_6.jpeg)

# **Cluster Algorithm**

![](_page_26_Figure_1.jpeg)

## Petiroc2C

### PETIROC2 : Trigger logic

![](_page_27_Figure_2.jpeg)

- Trigger is latched in RS cell
- · Reset of this latch is common to all channels and create retriggering

PETIROC2C : Trigger logic

![](_page_27_Figure_6.jpeg)

- · Reset of this latch is individual
  - · This local reset might solve the issue as only 1 ch has its logic toggling
  - Width of the pulse is now constant and provided by  $\Delta t$

### **Schamatic of Finnal FEB**

![](_page_28_Picture_1.jpeg)

# Schematic and Layout Status William Tromeur

![](_page_28_Figure_3.jpeg)

**TDC** measurements principle

![](_page_29_Figure_2.jpeg)

# **GIF++ Setup for efficiency tests (Photo)**

![](_page_30_Picture_1.jpeg)

![](_page_31_Picture_1.jpeg)

![](_page_32_Picture_1.jpeg)