improved-RPC for CMS Muon system upgrade for HL-LHC

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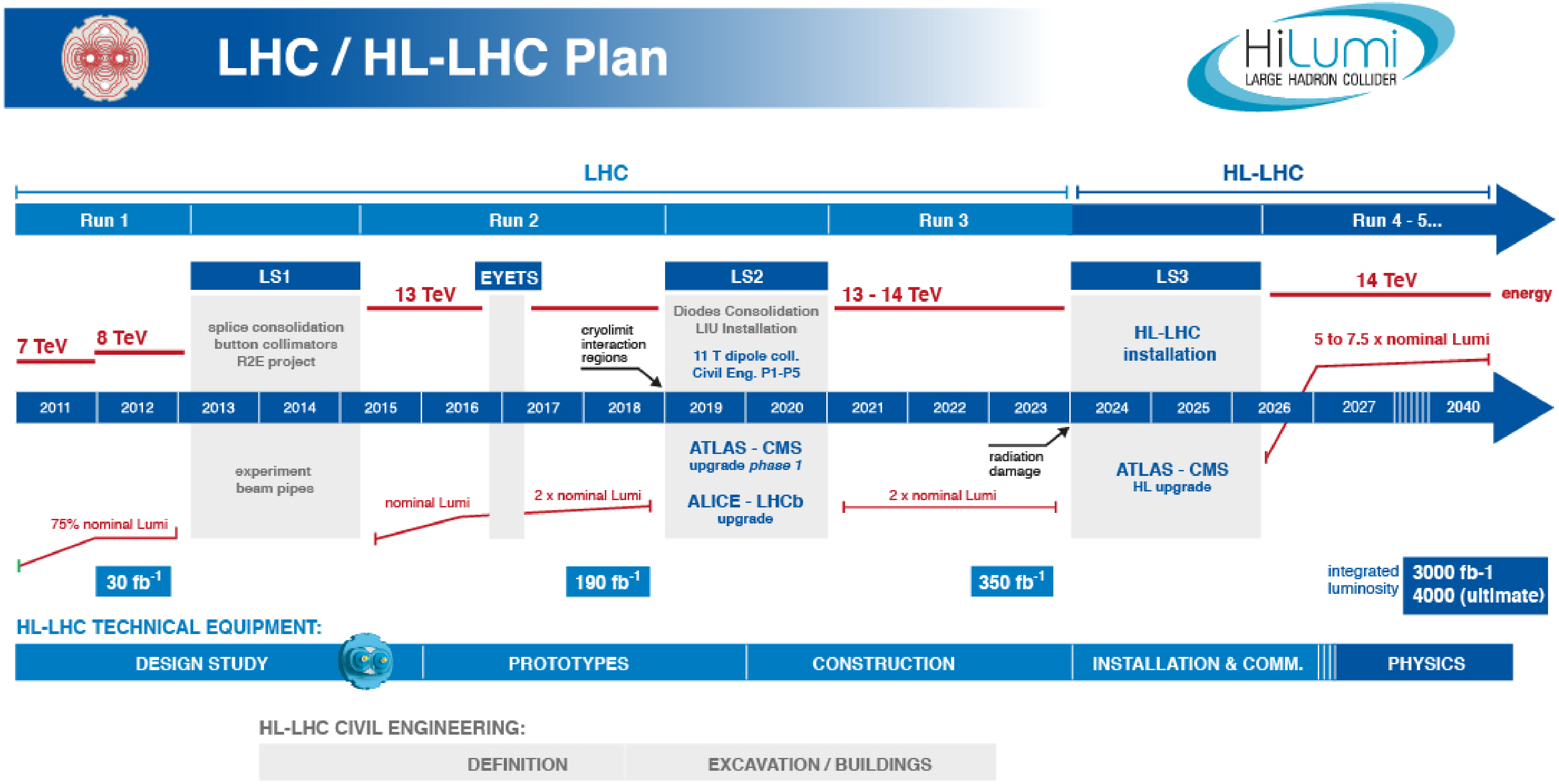
Outline of the Talk

- CMS-RPC upgrade during Phase-II
- Motivation for improved-RPC (iRPC)
- iRPC design and specification
- Background rate study of iRPC
- iRPC performance at GIF++
- Optimization of Resistivity of Graphite
- Summary and Conclusion

HL-LHC Plan and Challenges

HL-LHC Phase:

- Luminosity increase 5 times more than nominal value: $5x10^{34}cm^{-2}s^{-1}$
- Harsher background rate, more pile-up
- Extension of the muon coverage upto $|\eta| = 2.4$ to increase redundancy in high eta region



**** The scheduled is changed a little bit in january, adding one more year to Run III.**

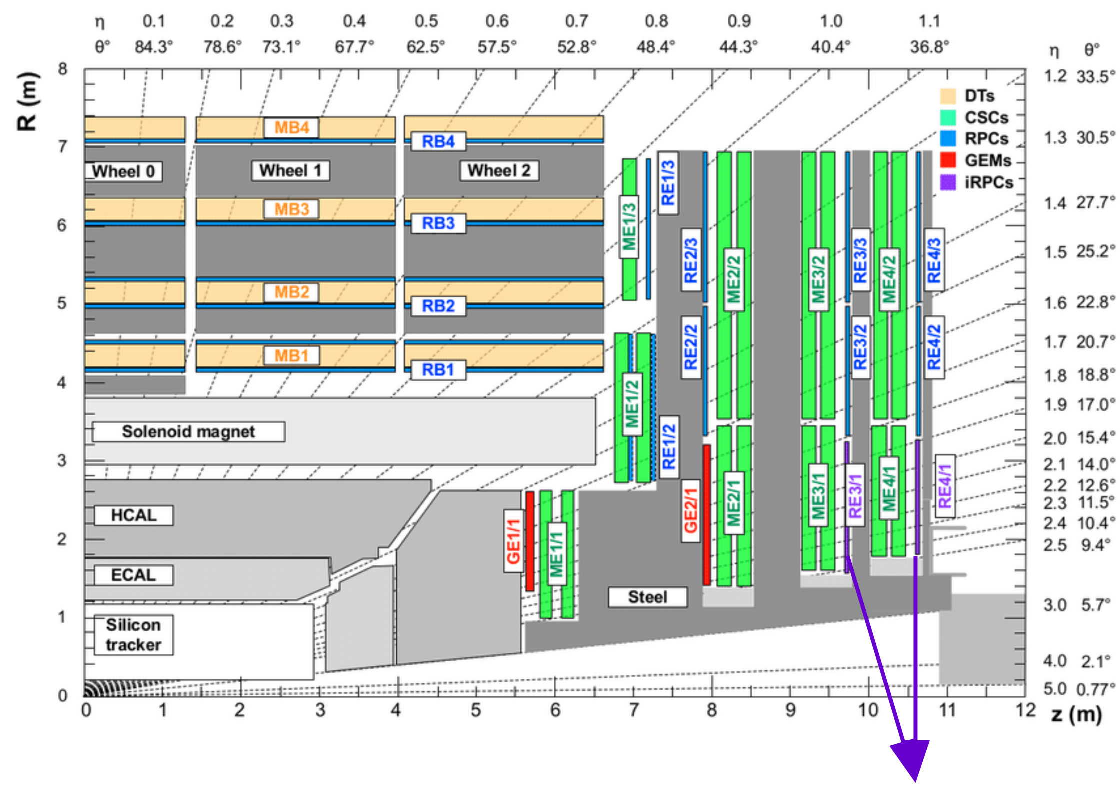
Phase-II upgrade for CMS-RPC

Present CMS-RPC system:

- 1056 RPCs – 480 (barrel) + 576 (endcap)
- Pseudorapidity coverage upto $|\eta| < 1.8$

HL-LHC Phase for CMS-RPC:

- Increase redundancy in high eta region in station 3 and 4 by installing 72 improved-RPC (iRPC)
- iRPC chambers and backend electronics will be installed before LS3 in the technical stops
- Longevity of present RPC system**



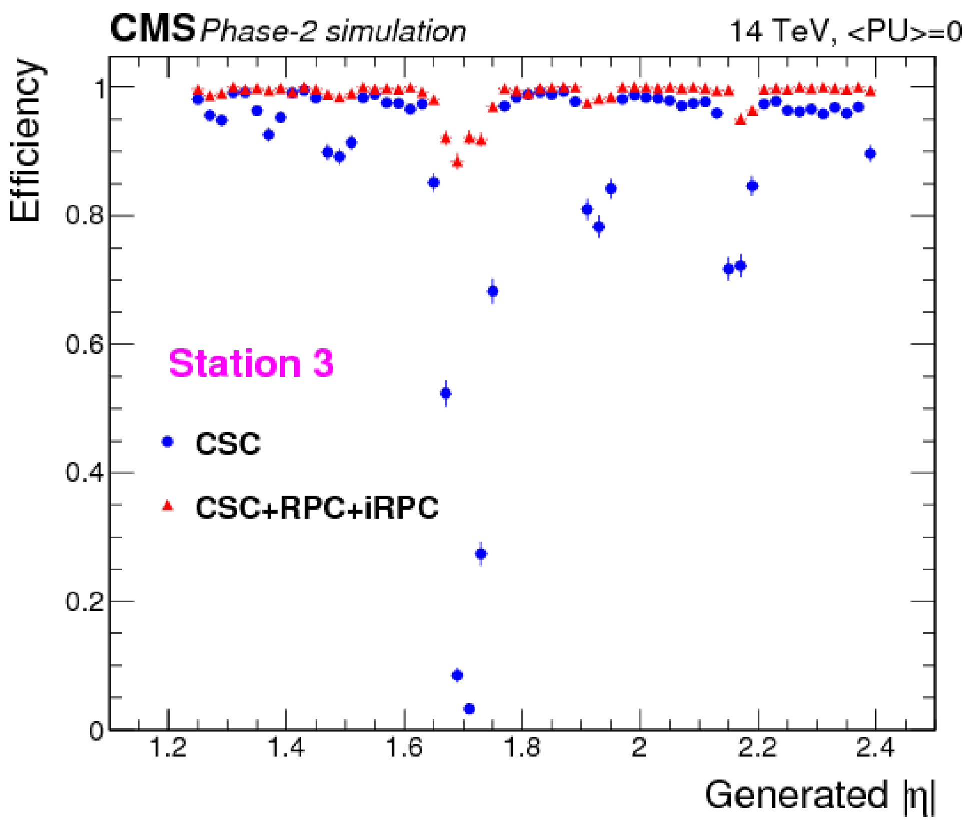
improved-RPC

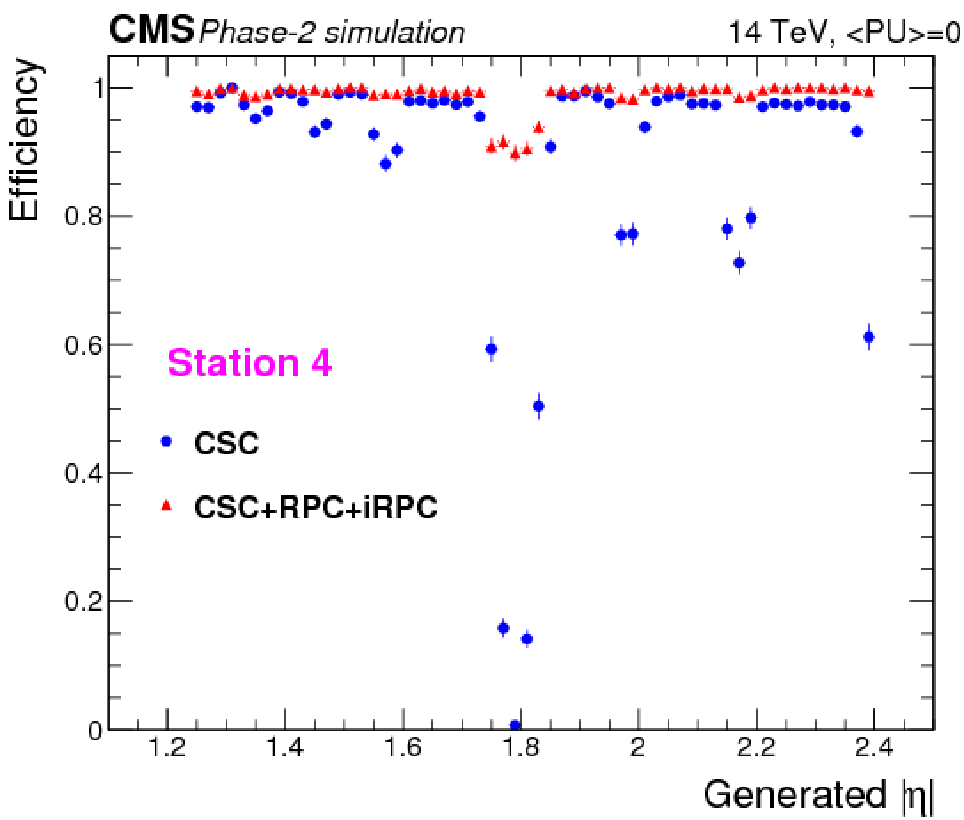
** See Reham's talk on Longevity study of present RPC system.

✯ During HL-LHC, the maximum expected background rate will be much high and improved-RPC have better detector performance ensuring high rate capability ~2 kHz/cm^2 (with safety factor of 3).

Motivation for improved-RPC in Endcap Region

- With the installation of improved-RPC in high-eta region, the trigger primitive efficiency is improved and is clearly visible in station 3 and 4.



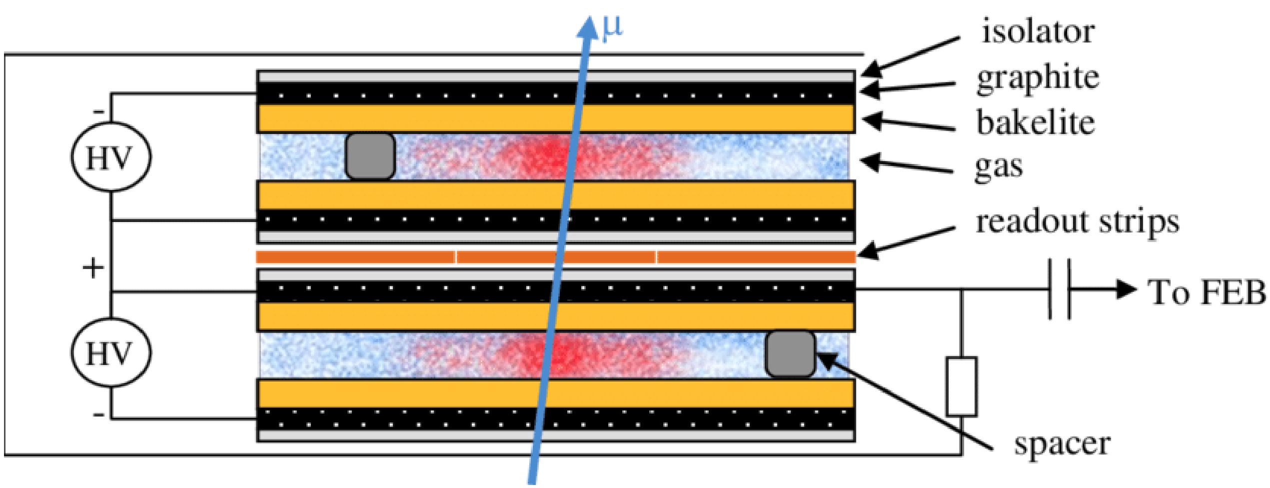


** More details in Brieuc's talk on RPC system in the CMS Level-1 Muon Trigger

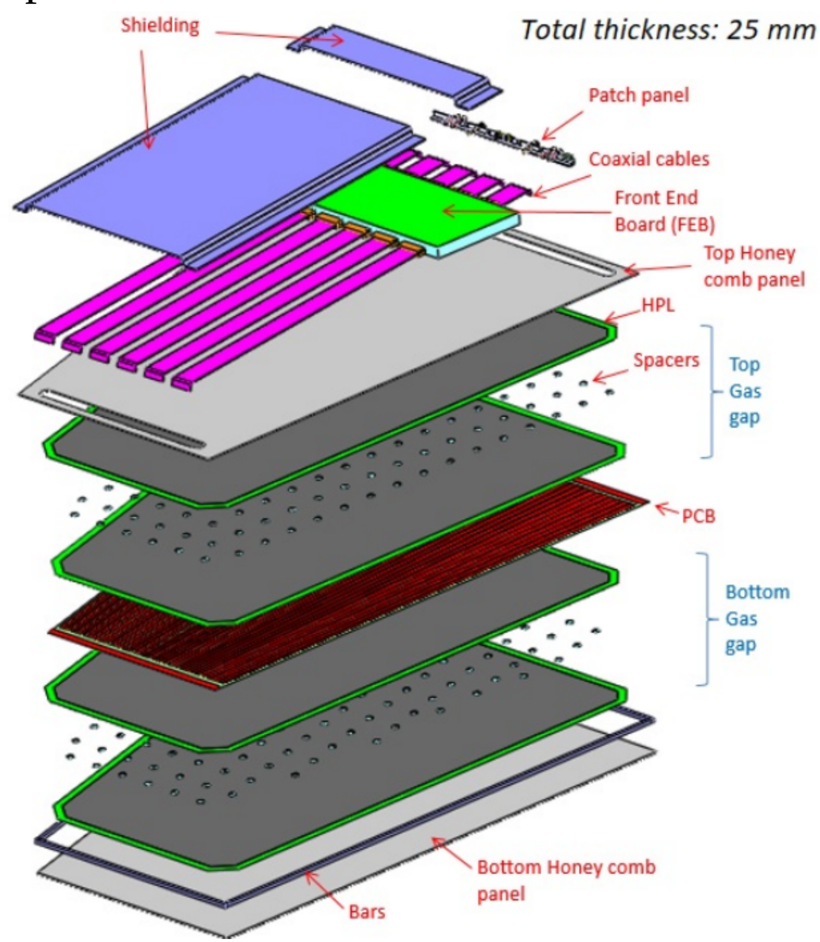
improved-RPC design and specifications

To increase the RPC rate capability, various factors have been helpful:

- Resistivity and thickness of the electrodes
- Gas gap thickness
- New front-end electronics
- Readout double coordinate – **XY position (2D sensitivity)**
- strips are readout from both ends (2D)



Double gap RPC design



iRPC design including the readout electronics

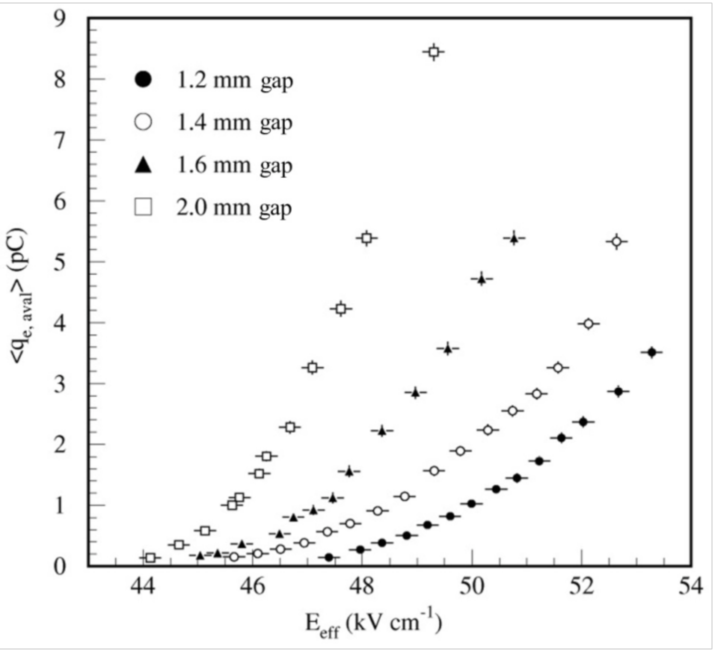
iRPC design and specifications – contd. 2

- HPL Resistivity: 0.9-3 x 10^{10} Ωcm

- Electrodes thickess: 1.4mm
  - Reduce the recovery time
  - Increase in efficiency of extracting the pickup charge from the avalanche charge.

- Gas Gap thickness: 1.4mm
  - Reduce the fast growth of pickup charge of the ionization avalanches and lower the operational high voltage making system more robust than before – less chance of aging.

- Electronic Threshold
  - 50fC – Lower threshold electronic helps to provide better sensitivity to reduce charge



iRPC requirements for HL-LHC		
Specification	**RPC**	**iRPC**
|η| coverage	0-1.8	1.9-2.4
Max. expected rate (safety factor 3 included)	600 Hz/cm^2	2 kHz/cm^2
Max. Integrated charge (safety factor 3 included)	~ 0.8 C/cm^2	~ 1 C/cm^2
High Pressure Laminate thickness	2 mm	1.4 mm
Number and thickness of gas gap	2 and 2 mm	2 and 1.4 mm
Resistivity (Ωcm)	1 - 6 x 10^{10}	0.9 - 3 x 10^{10}
Charge threshold	150 fC	50 fC

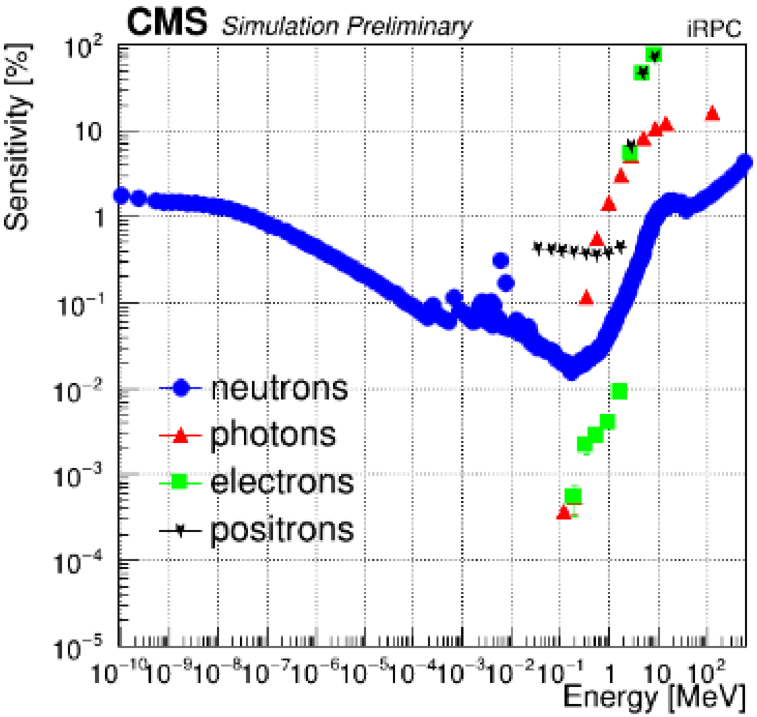
All these specifications are helpful in increasing the rate capability by a factor of ~3.

iRPC sensitivity

- Since the geometry is new, so we developed a new sensitivity of the detector using **Geant4 simulation toolkit.**

- The detector response to background particles, known as Sensitivity S(E) is defined

$$S(E) = \frac{N_{HIT}}{N_{BG}}(E)$$



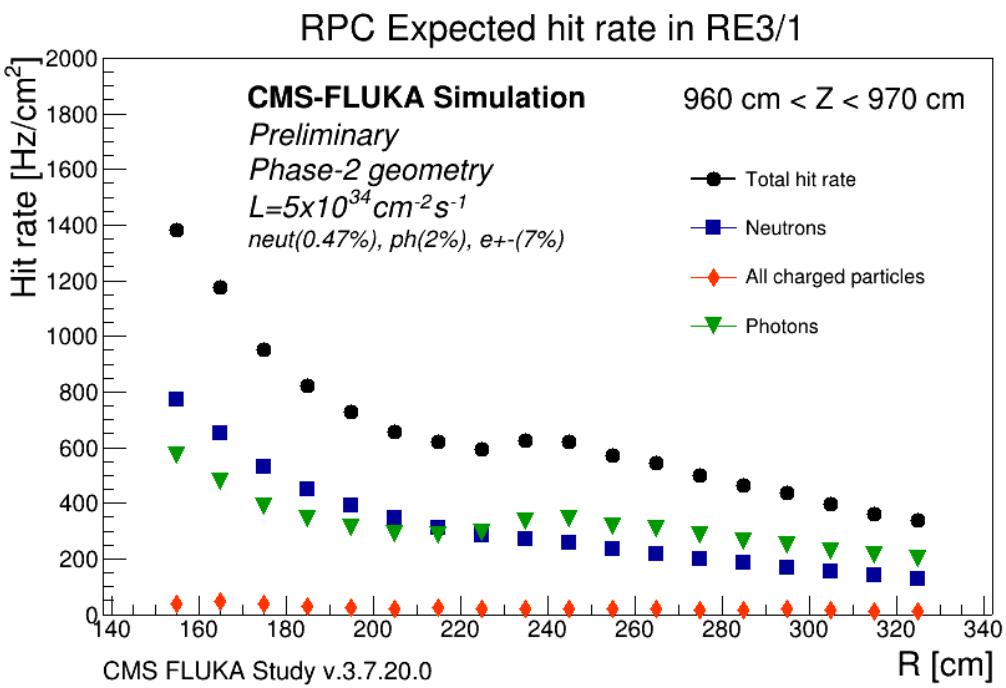
- Sensitivity is a function of energy of different particles because at different energies, different processes are responsible for production of secondary ionisation.

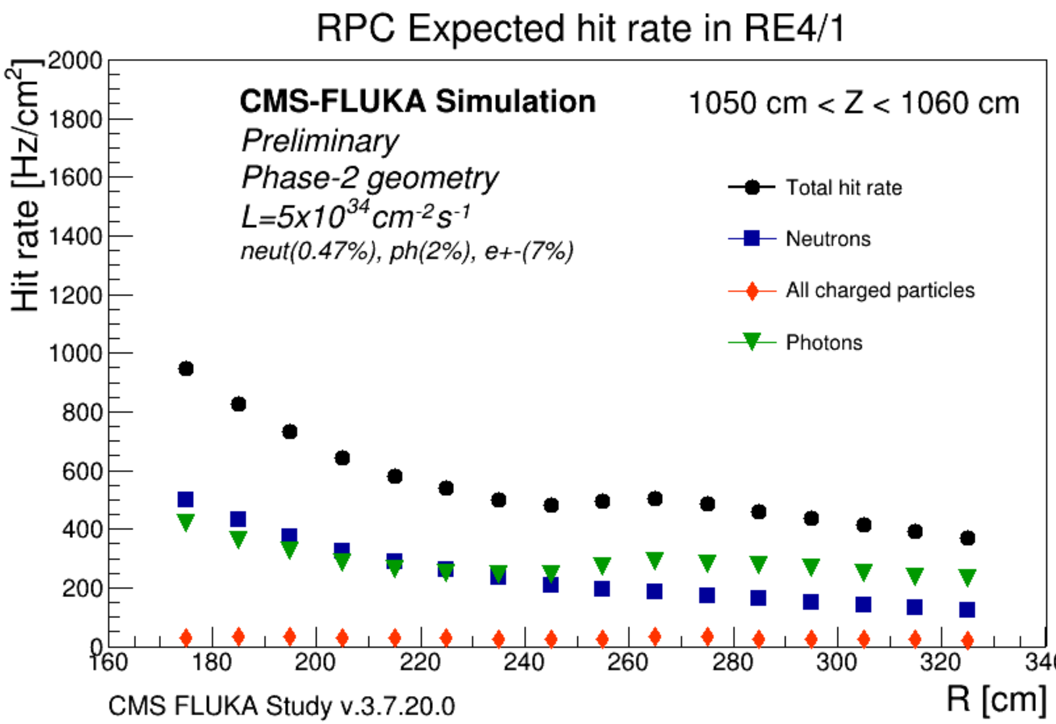
- iRPC sensitivity studied with different particles that compose the CMS background at the expected HL-LHC spectra.

Background rate study of iRPC at HL-LHC

- **Hit rate R(E) = Φ^{CMS}_{bkg}(E) x S(E)**

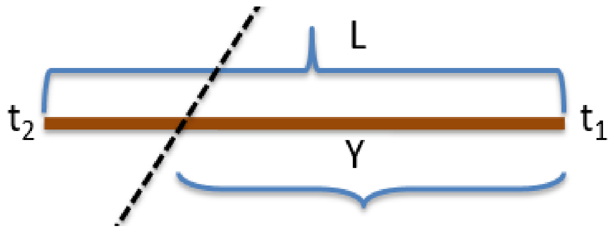
  Φ(E) -> incident particles flux estimated using **FLUKA simulation**, and S(E) is the detector sensitivity using **Geant4 simulation.**





- MC simulation of the background rate expected in the endcap RE3/1 and RE4/1 station during HL-LHC as a function of the distance (R) from the center of the CMS beam pipe

GIF++: Study of Rate Capability (2018)



$$Y = L/2 - v * (t_2 - t_1)/2$$

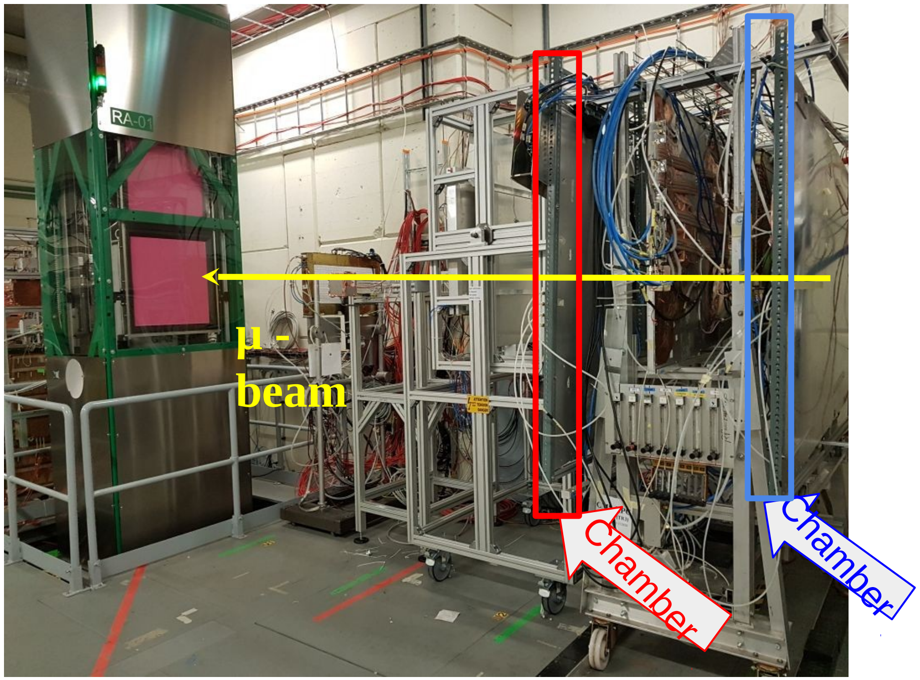
A board that contains:

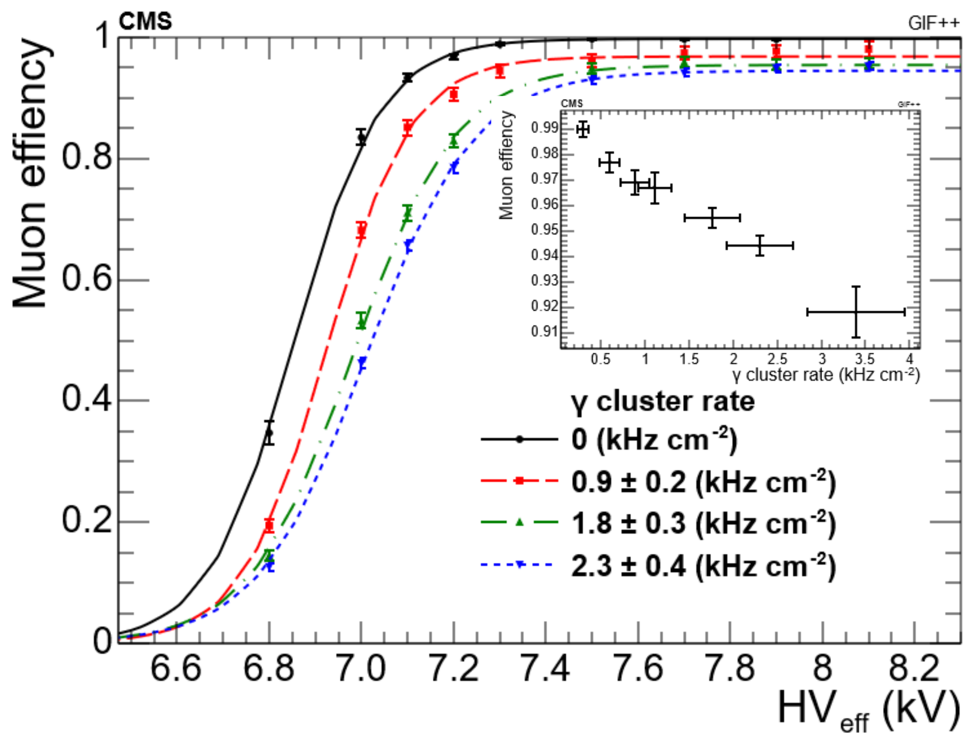
- **1 PETIROC2A ASIC + FPGA CYCLONE2**
- **Threshold ~80fC** Ethernet-based communication was conceived to read out the strips **FR4** 44 strips

Efficiency at **~2kHz cm^{-2}** of background **95%**

Absolute time resolution of prototype: **~400ps**

- 14 TBq ^{137}Cs used in GIF++ with different attenuation coefficients is used to obtain different gamma irradiation levels.
- Chamber at a rate of up to **2 kHz·cm^{-2}** is tested.





Optimisation of Graphite Resistivity

- One the important parameters for the performance of the RPC trigger is the surface resistivity of the electrodes which influence directly the cluster size.

- Present RPC system has : RE4 – 150 kΩ and RE2/3 - ~ 100 kΩ

Measurement study on iRPC:
- iRPC (1.4 mm) chamber has been tested for two graphite resistivity regions
- **600 kΩ (High Resistivity) ; 50 kΩ (Low Resistivity)**

- Study has been performed with INFN – Rome Tor Vergata Electronics to check the effect on cluster size with cosmics.

- Chamber is equipped with PCB strip plane in both graphite resistivity regions (5 mm strip width).

Link to Rome- Tor Vergata Electronics Paper: https://iopscience.iop.org/article/10.1088/1748-0221/14/09/C09023

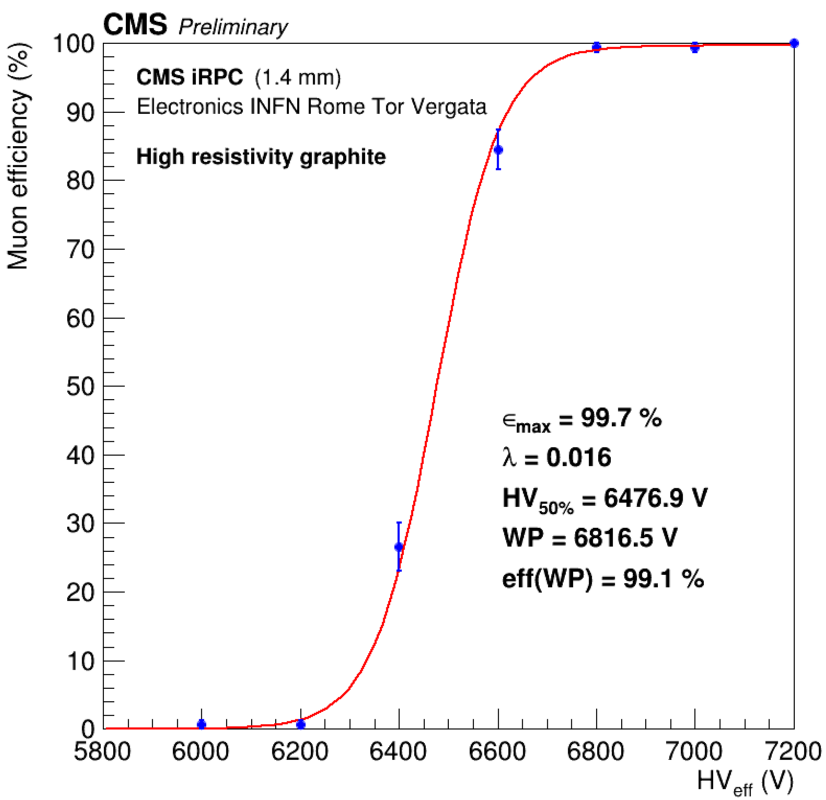
Muon Efficiency for high and low Resistivity Graphite

- The working point is defined by fitting the efficiency curve with the following sigmoid formula:
  - $$\varepsilon = \frac{\varepsilon_{max}}{1 + e^{-\lambda\,(HV_{eff} - HV_{50\%})}}$$
- The working point voltage is then defined as:

WP = ln(19)/λ + HV(50%) + 150 V

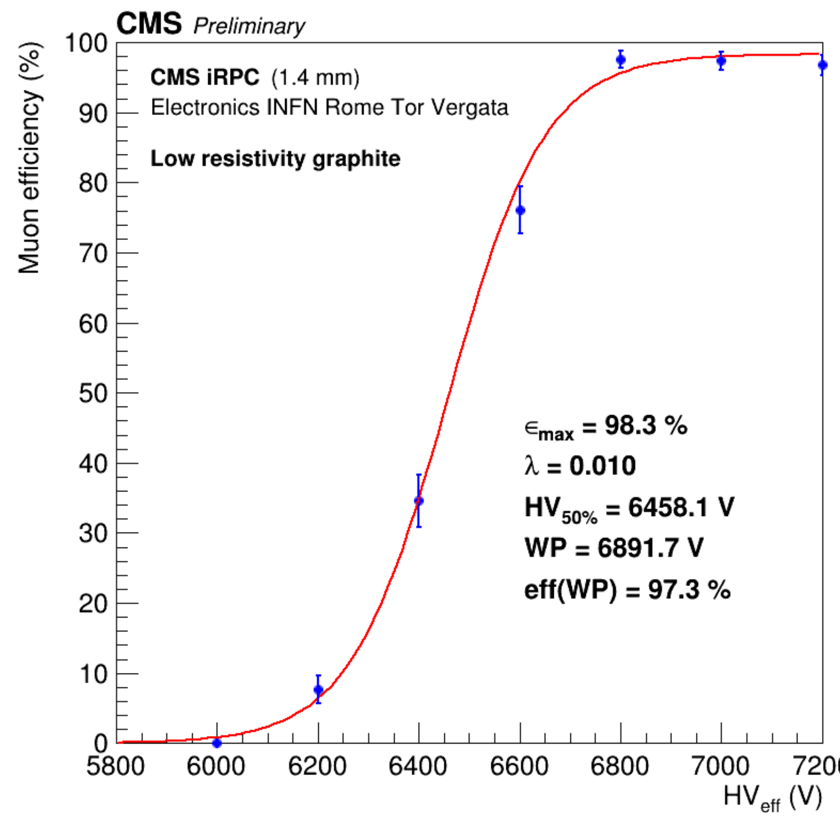
High Resisitivity Graphite : 600 kΩ

Working point - 6.82 kV ; Efficiency - 99.1 %.



Low Resisitivity Graphite : 50 kΩ

Working point - 6.89 kV ; Efficiency - 97.3 %.



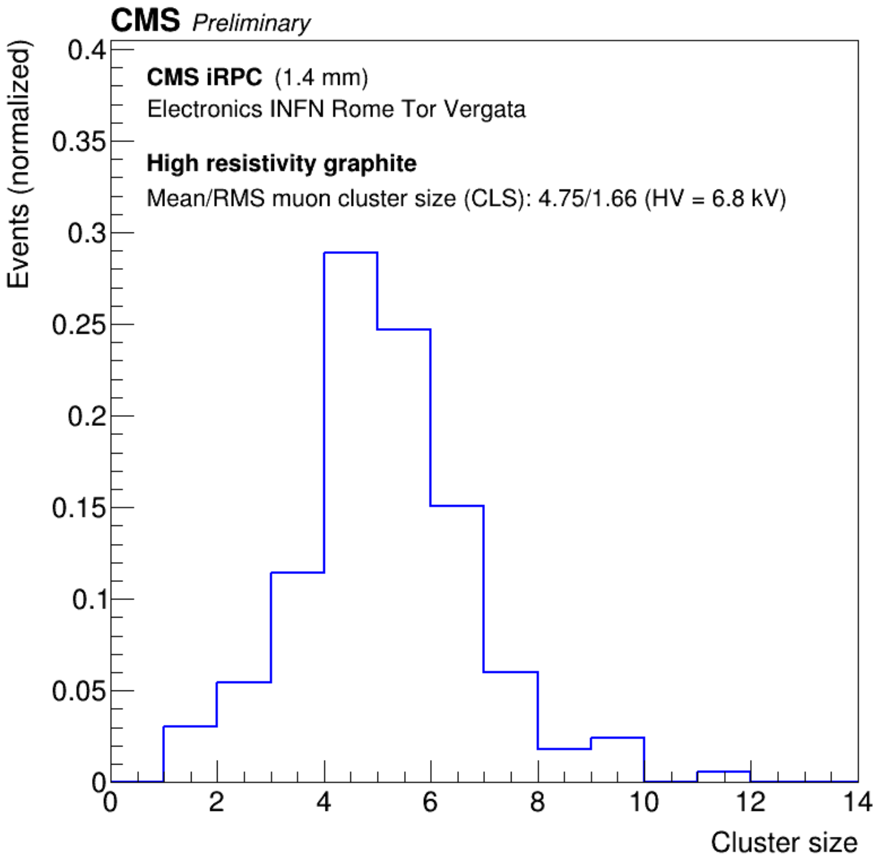
** More details in Sabino’s talk on iRPC Rome-Electronics

Muon Cluster Size for high and low Resistivity Graphite

- For high resistivity graphite, muon cluster size is low with narrower cluster size distribution as comapred to low resistivity graphite.
- We expect this behaviour because of difference in graphite resistivity, directly influencing cluster size through cross talk by the capacitive coupling of the strips.

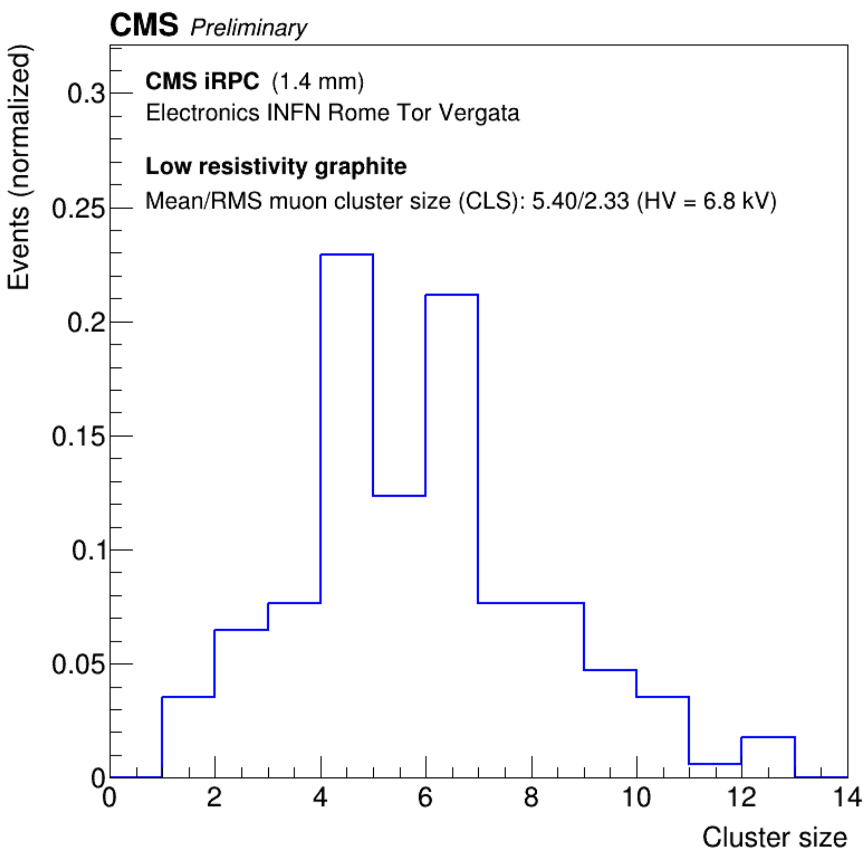
High Resisitivity Graphite : 600 kΩ

Mean Cluster Size - 4.75 ; RMS – 1.66



Low Resisitivity Graphite : 50 kΩ

Mean Cluster Size – 5.40 ; RMS – 2.33



- **High resistivity graphite is chosen over low because of the small muon cluster size.**

** More details in Sabino’s talk on iRPC Rome-Electronics

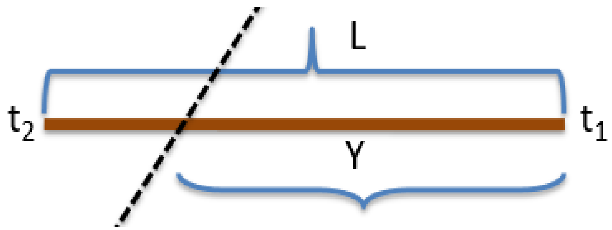
Conclusion

- To cope with higher backgrounds rate at high $|\eta|$ region, iRPCs are proposed to be installed before LS3 in the techincal stops.
- 1.4 mm electrode and gas gap thickness improve the rate capability and also reduce the chance of aging effect.
- The estimation of the background hit rate expected during HL-LHC in the RE3/1 and RE4/1 stations has been done and the expected average hit rate will be ≈ 2 kHz/cm^2 including a safety factor three.
- A prototype of iRPC have been successfully tested at GIF++, efficiency of more than 95% at the rate of 2 kHz/cm^2 was measured.
- High and low resistivity graphite measurements has been performed on dedicated chamber and high graphite resistivity shows a lower muon cluster size with a narrower cluster size distribution.


THANK YOU
FOR YOUR
ATTENTION

BACK UP

GIF++: Study of rate capability (2018)



$$Y = L/2 - v * (t_2 - t_1)/2$$

A board that contains:

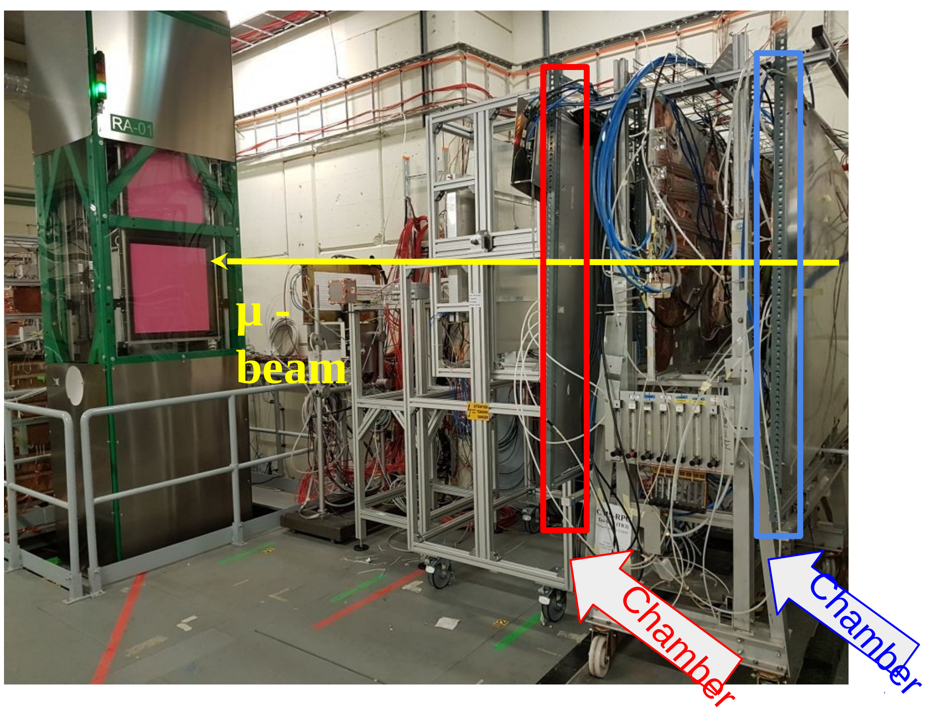
- **1 PETIROC2A ASIC + FPGA CYCLONE2 Threshold ~80fC** Ethernet-based communication was conceived to read out the strips **FR4** 44 strips

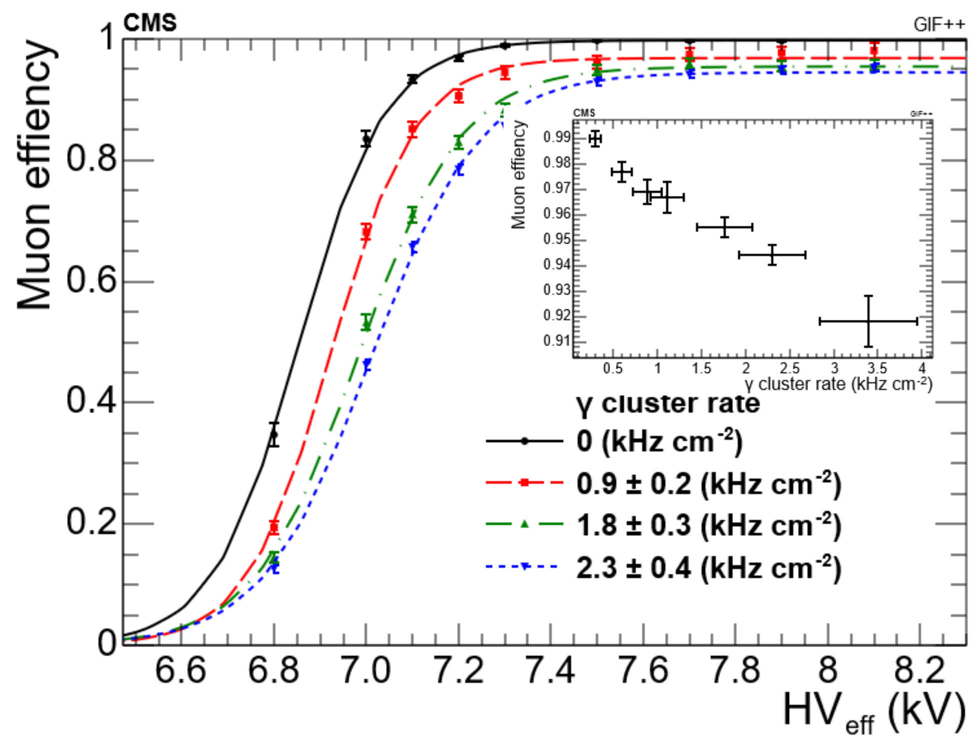
Efficiency at **~2kHz cm^{-2}** of background **95%**

Absolute time resolution of prototype: **~400ps**

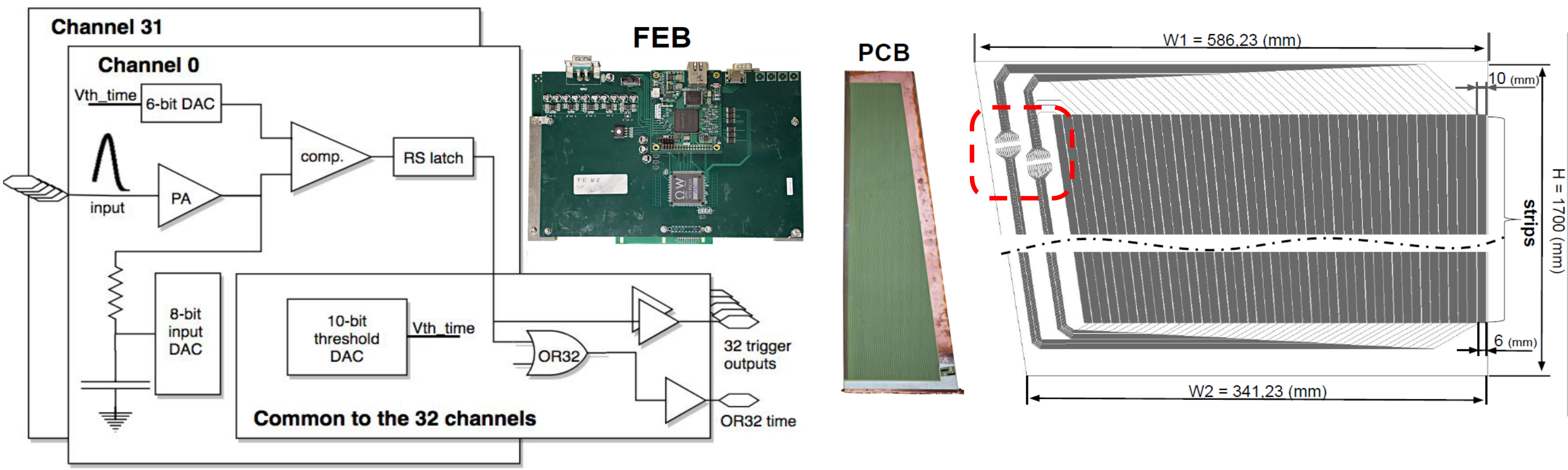
14 TBq 137Cesium is used in GIF++ with different attenuation coefficients is used to obtain different gamma irradiation levels.

To test our chambers a rate of up to **2 kHz·cm^{-2}** needs to be **seen** in our chamber.





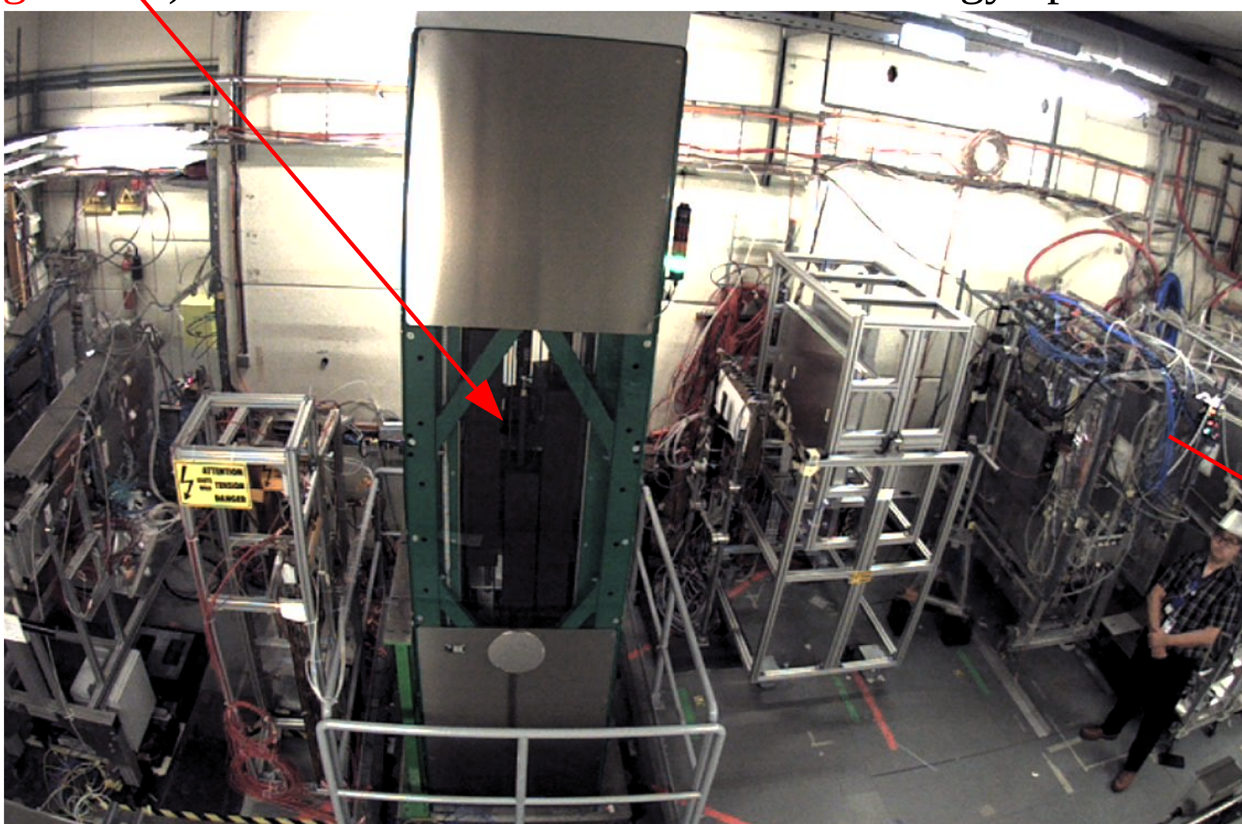
GIF++ Setup for efficiency tests (Photo)



The Front-End Electronics Board (FEB) that hosts one PETIROC ASIC and the FPGA that includes the TDC and the schematics of the PETIROC ASIC [3]. (left) Photograph and dimensions of a prototype pickup-strip PCB. (right)

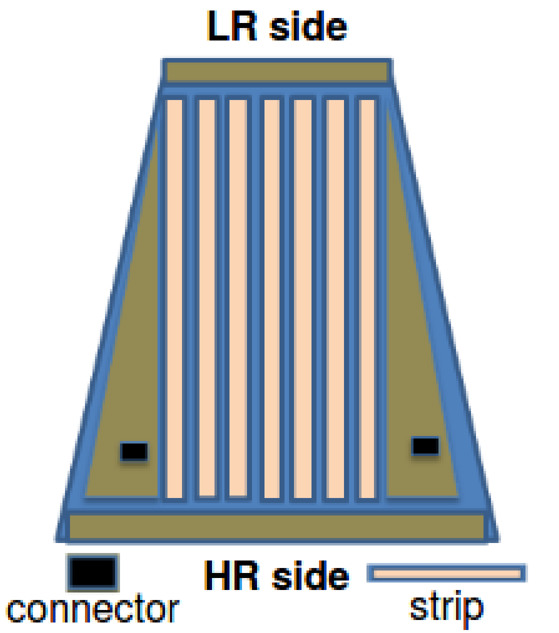
GIF++ test facility for improved-RPC

- ❖ **GIF++ is a facility that allows to test real size detectors in a similar background condition as in CMS.**
- ❖ 14 TBq ^{137}Cs source (662 keV gammas)
- ❖ Gamma filters:
  Systems of movable attenuators allows to test the detectors in different irradiation conditions
- ❖ Muon beam
  ↦ Energy up to 150 GeV, 10^4 muons/spill.



iRPC trolley

PCB layout of strip readout panels for iRPC



Front End electronics: ** Dedicated talk by Konstantin Shchablo

- ASIC PETIROC, based on SiGe technology
- fast premplifier with overall bandwidth of 1 Ghz

Return strip PCB and the measured impedance

Integrated return-strip scheme “3”-layer PCB with strips and return-strips with the same impedance.

PCB with 48 (v1) or 44 (v0) strips to instrument half an iRPC chamber with connectors placed on the high eta region:

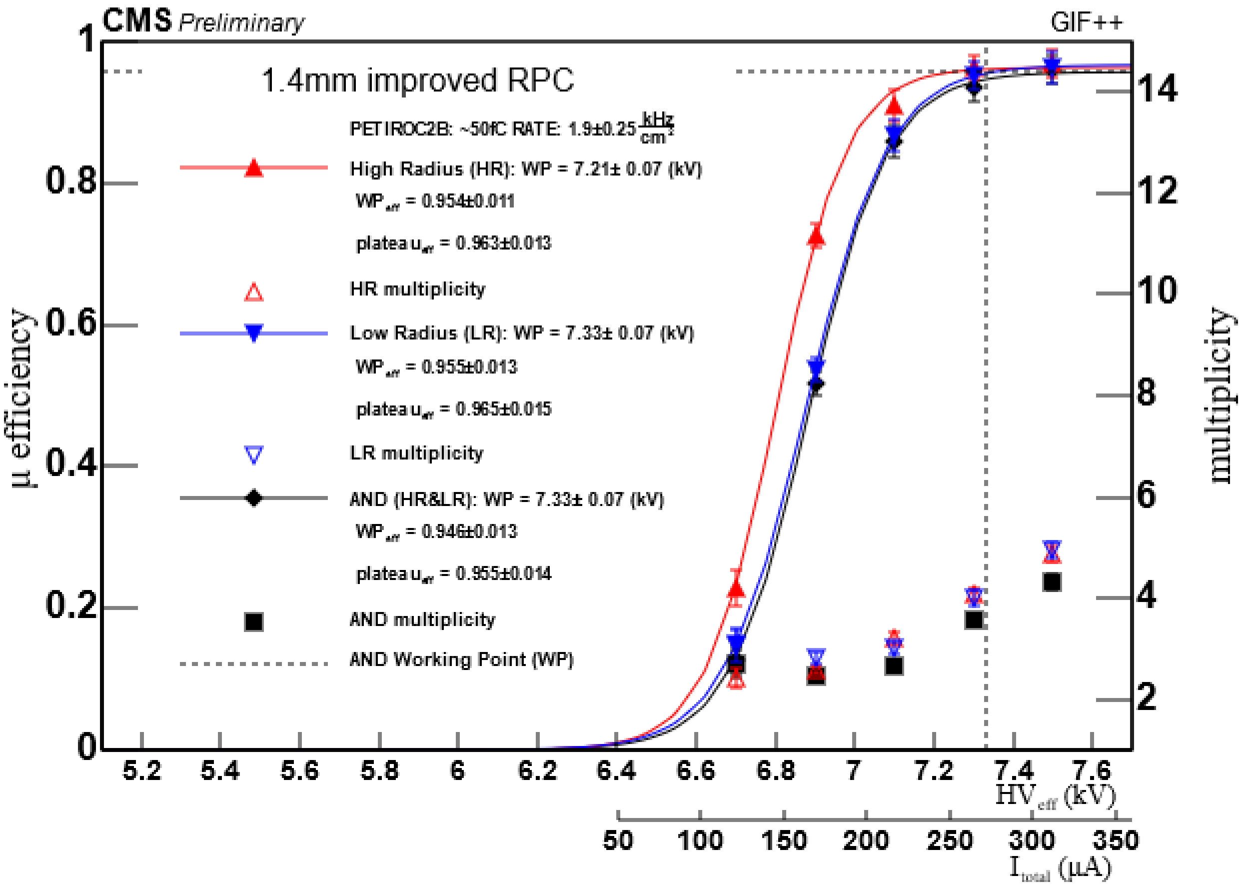
1.) minimize the impact of radiation

2.) take into acounf integration issues.

** More details for Petiroc Electronic in Konstantin Slides .

Performance of iRPC at GIF++

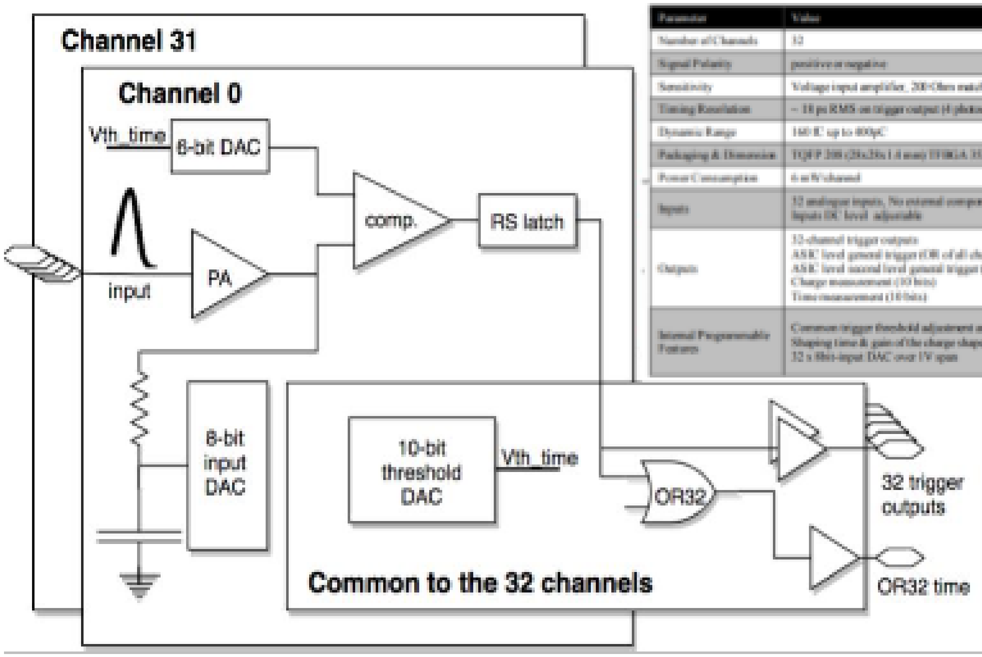
- iRPC validated at GIF++ with background rate at ~ 2 kHz/cm².



➢ Efficiency of more than 95% is obtained.

Front end electronics: TDC and ADC

ASIC PETIROC: Analog Digital Converter

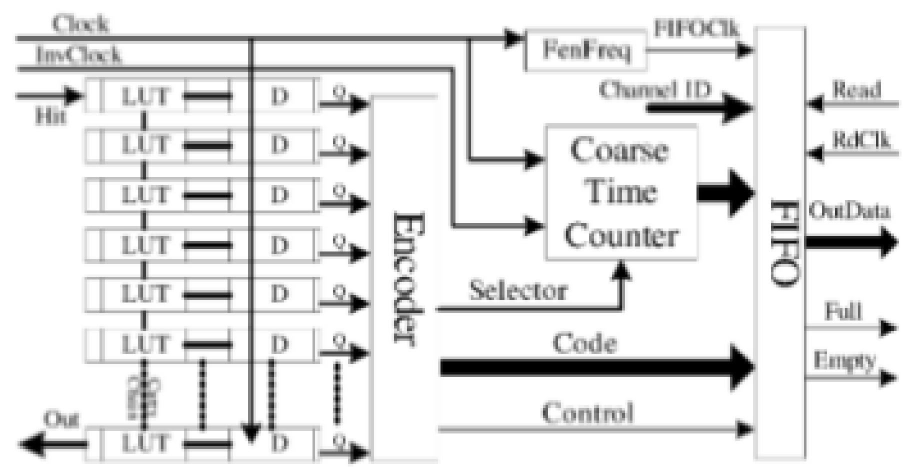


Parameter	Value
Number of Channels	32
Signal Polarity	positive or negative
Sensitivity	Voltage input amplifier, 50 Ohm matching
Timing Resolution	~ 18 ps RMS on trigger output (4 photoelectrons injected)
Dynamic Range	160 fC up to 400pC
Packaging & Dimension	TQFP 208 (28x28x1.4 mm) TFBGA 353 (12x12x1.2mm)
Power Consumption	6 mW/channel
Inputs	32 analogue inputs, No external component required Inputs DC level adjustable
Outputs	32-channel trigger outputs ASIC level general trigger (OR of all channel) ASIC level second level general trigger (OR of all channels) Charge measurement (10 bits) Time measurement (10 bits)
Internal Programmable Features	Common trigger threshold adjustment and 6bit-DAC/channel Shaping time & gain of the charge shaper 32 x 8bit-input DAC over 1V span

The Front-End Electronics Board (FEB) that hosts one PETIROC ASIC and the FPGA that includes the TDC and the schematics of the PETIROC ASIC

FPGA Cyclone: Titme Digital Converter

$$T_{\text{out}} = T_{\text{coarse}} + T_{\text{fine}}$$



Block diagram of the time-to-digital converter implemented in a single FPGA device.

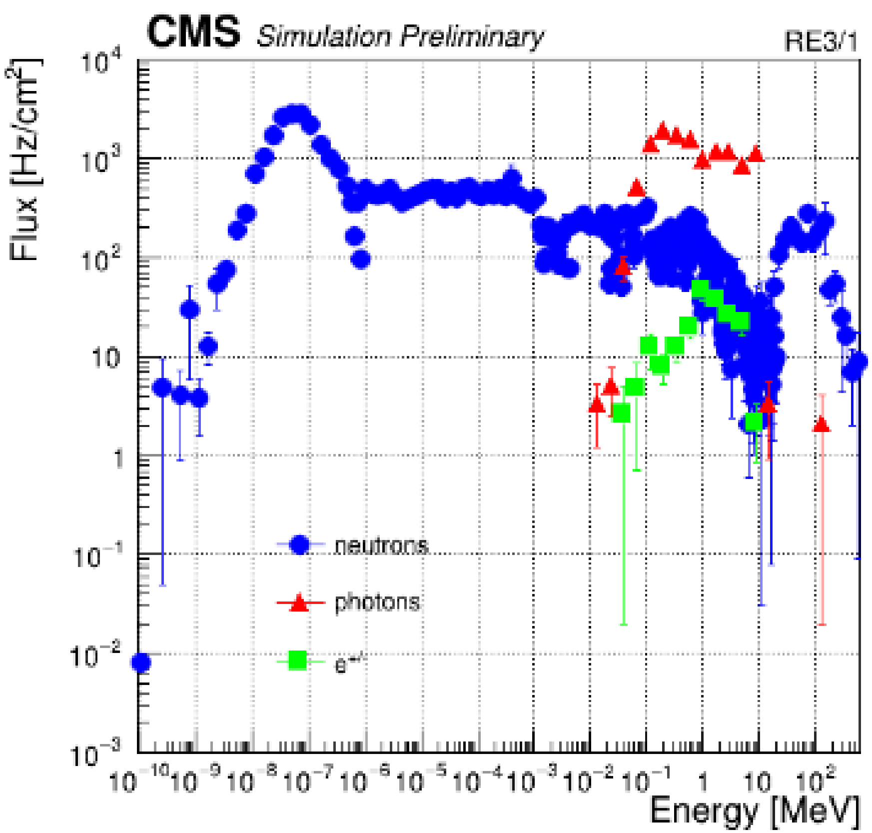
Electronics Calibration on full size prototype

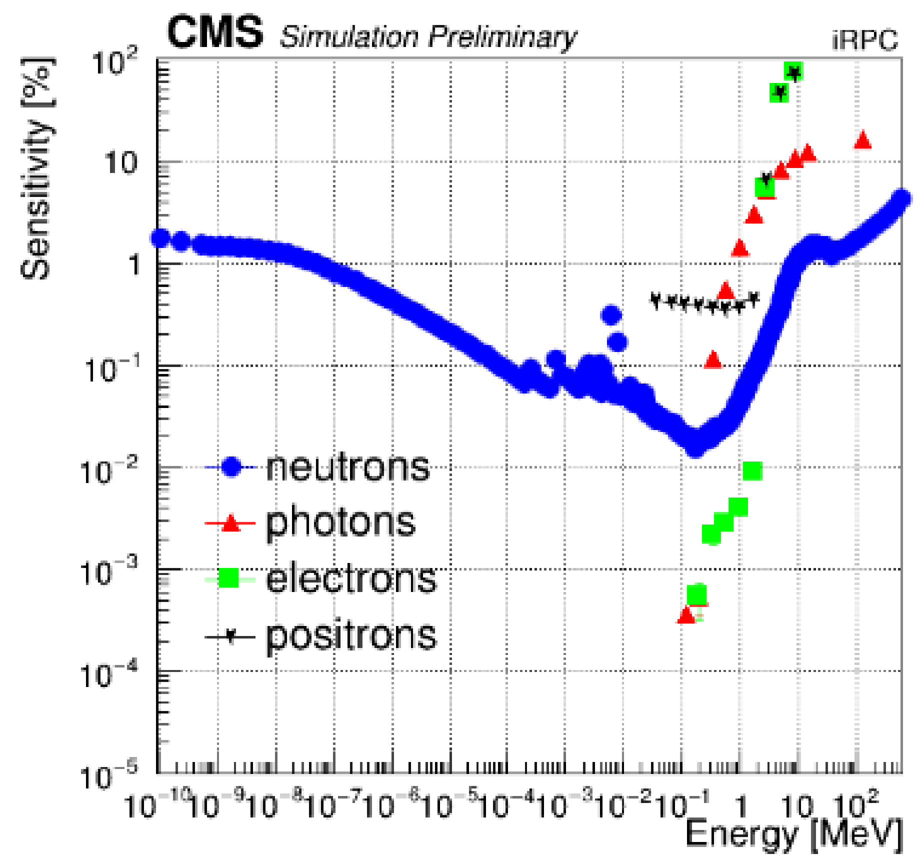
- Baseline of this new front-end electronic is: **PETIROC ASIC + TDC**.
  - 32-channel ASIC using fast preamplifier in SiGe technology.
  - overall 1 GHz bandwidth and a gain of 25.
  - Low noise and high time resolution.
- Two chambers (COAX and RETURN) are suggested based on the connection of the layout strips with FEB.
- For COAX- half strip length are on PCB and half are connected with coaxial cables and for RETURN- half strip length are connected on PCB with return line.
- Both prototypes was tested in GIF++ in May 2018 and validated with muons and source off : all specifications fulfilled. The results are in following slides.
- Return Chamber is easier to handle, compact and also pick up less noise.

** More details on front-end electronics in Konstantin's talk.

iRPC sensitivity and Flux at HL-LHC

- S is the probability for a particle (N_{BG}) at a given energy reaching the detector surface, to produce a signal (N_{HIT}):





iRPC front-end Electronics

- With the iRPC, the deposited charge through the passage of charged particles is less, so to detect lower charge (<50 fC) without affecting detector performance, the new front-end electronics is needed.

- The main requirements for new front-end electronics are:

  - to be able to detect lower charge.

  - precise timing readout electronics.

  - fast and reliable.

  - can sustain in high background environment during HL-LHC.

-

  - Readout double coordinate : XY position (2D).

** More details on front-end electronics in Konstantin’s talk.