Precise Tracking of Cosmic Muons Using Time-over-Threshold Property of NINO ASICs

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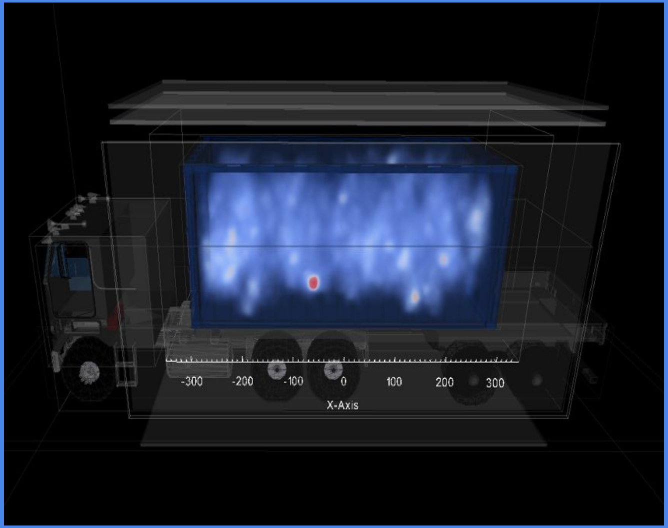
XV Workshop on Resistive Plate Chambers and Related Detectors (RPC 2020)

University of Rome "Tor Vergata" , 10 - 14 February 2020.

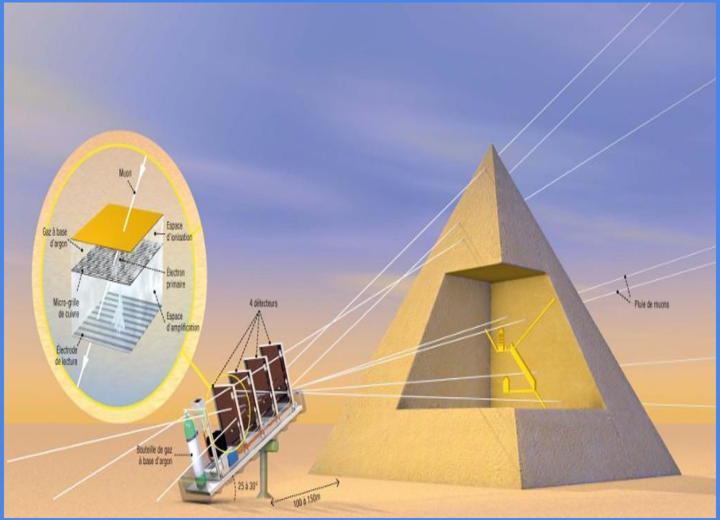
13rd Feb. 2018

Motivations

- Natural Cosmic Ray source.
- Other applications like imaging large structures, monitoring volcanoes and all.
- Based on Coulomb Scattering. (High-Z/ Low-Z discrimination)
- Accurate measurement of scattering angle requires precise tracking.



http://mutomweb.pd.infn.it:5210/



Scan Pyramid Project,CEA,

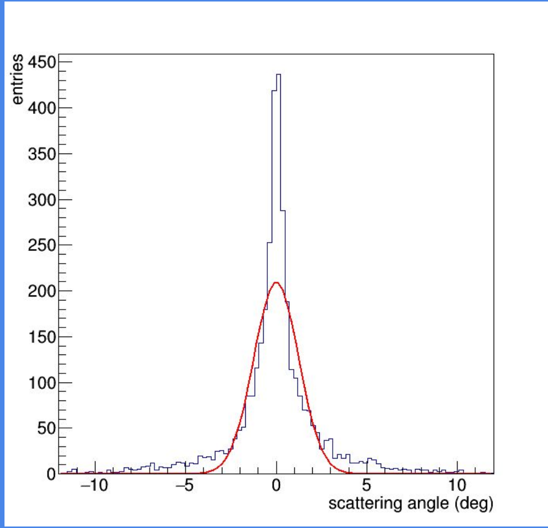
Strategy of Muon Scattering Tomography

$$\frac{dN}{d\theta_x} = \frac{1}{\sqrt{2\pi}\theta_0} e^{-\theta_x^2/2\theta_0^2}$$

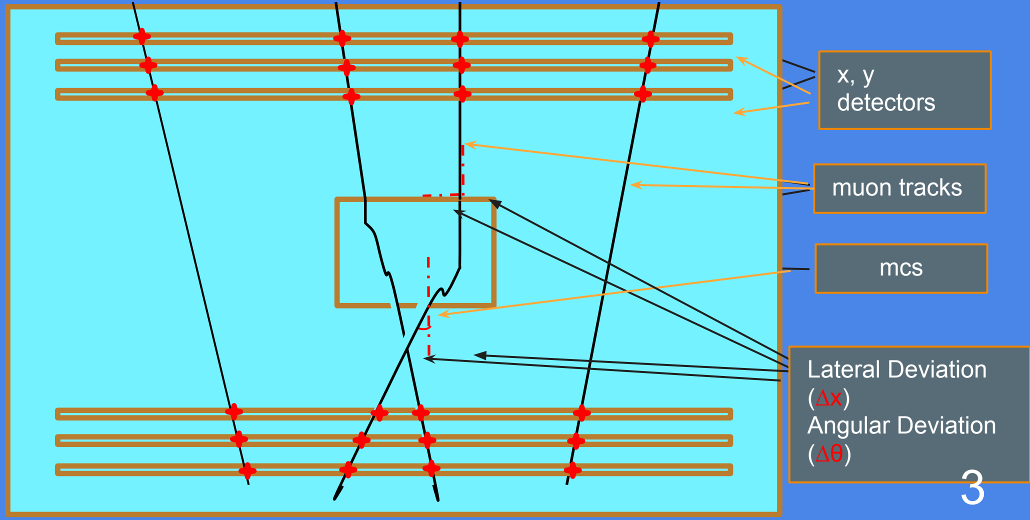
$$\theta_0 \approx \frac{13.6}{(pc\beta)} \times \sqrt{\frac{x}{X_0}} \times \left[1 + 0.038 \ln\left(\frac{x}{X_0}\right)\right]$$

$$X = \frac{716.4\,\mathrm{g/cm^2}\,A}{\rho Z(Z+1)\ln\left(287/\sqrt{Z}\right)}$$

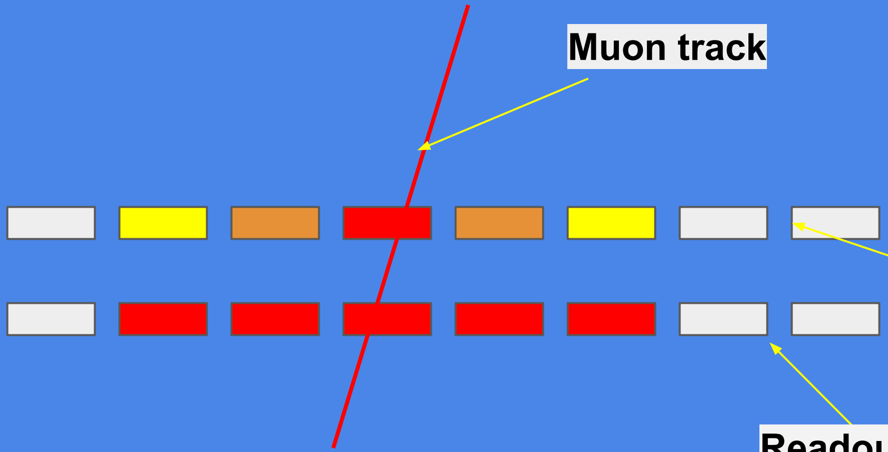
p = Momentum
β = V/C
X= Radiation Length
L= Thickness
A= Atomic Mass
Z= Atomic Number
ρ = Density



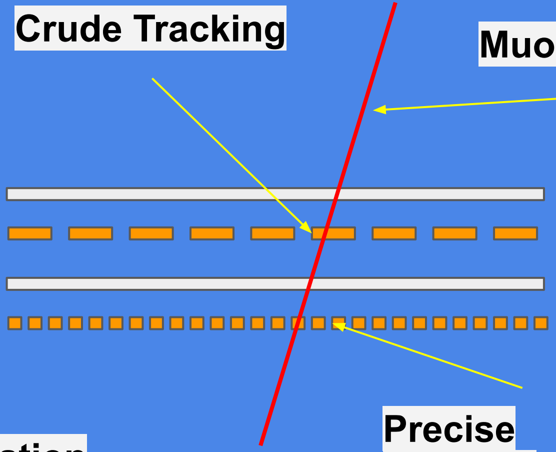
Scattering Angle Distribution

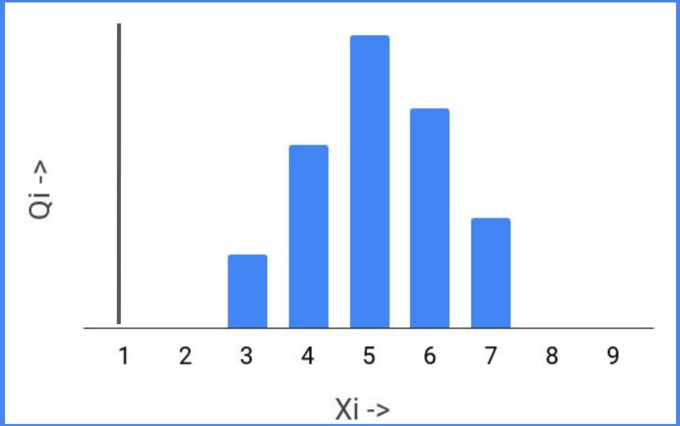


Spatial Resolution

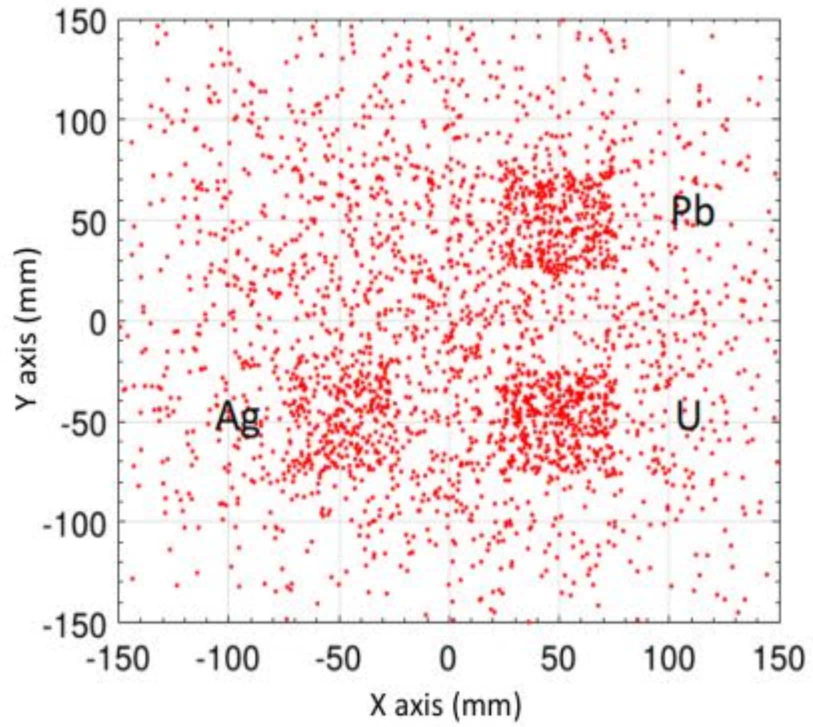


Charge Centroid
Method

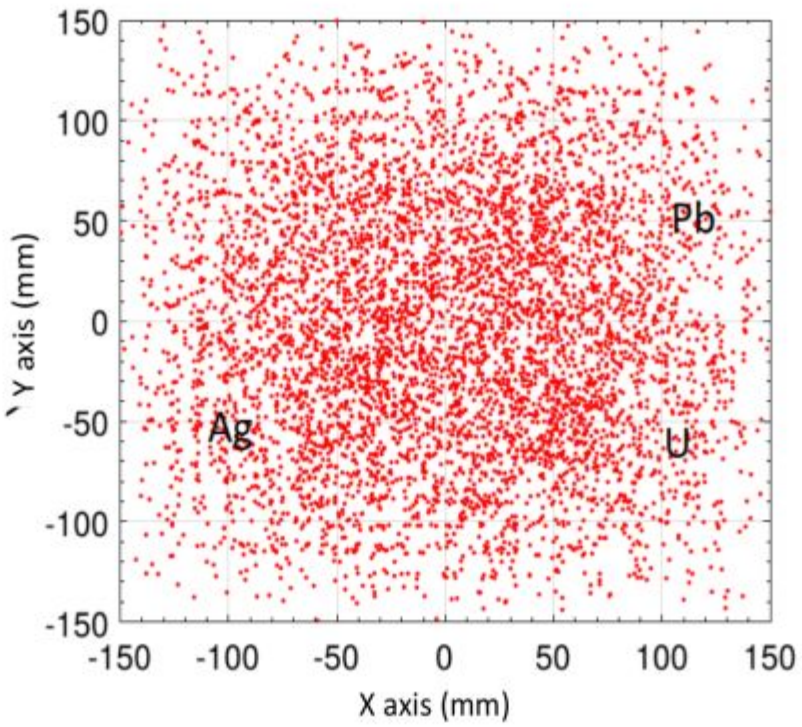




Effect of Resolution on Image reconstruction



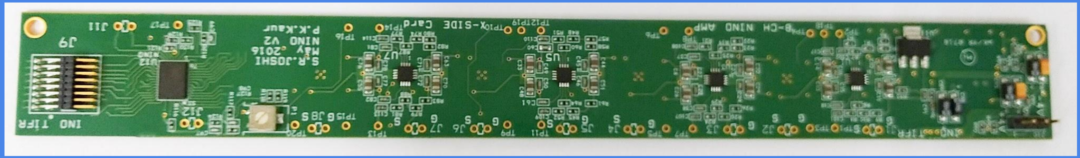
Ideal Resolution

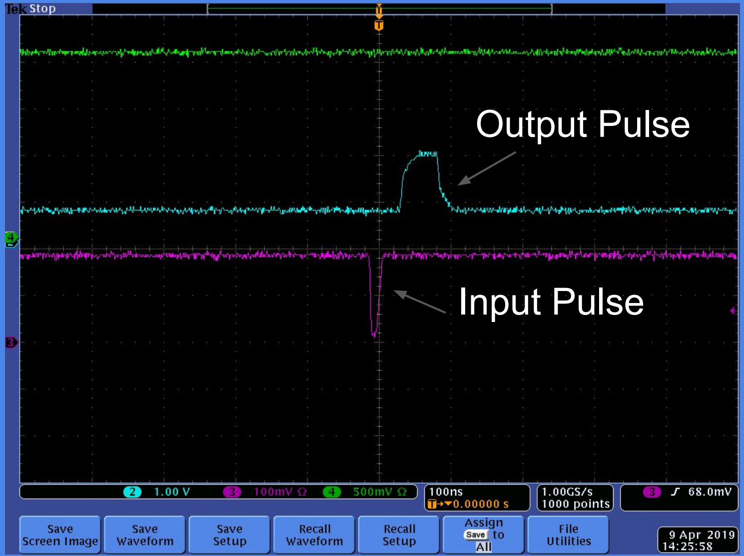


1 cm Resolution

S Tripathy et. al *Journal of Instrumentation*, *Volume 14*, *July 2019*

NINO Readout and TOT

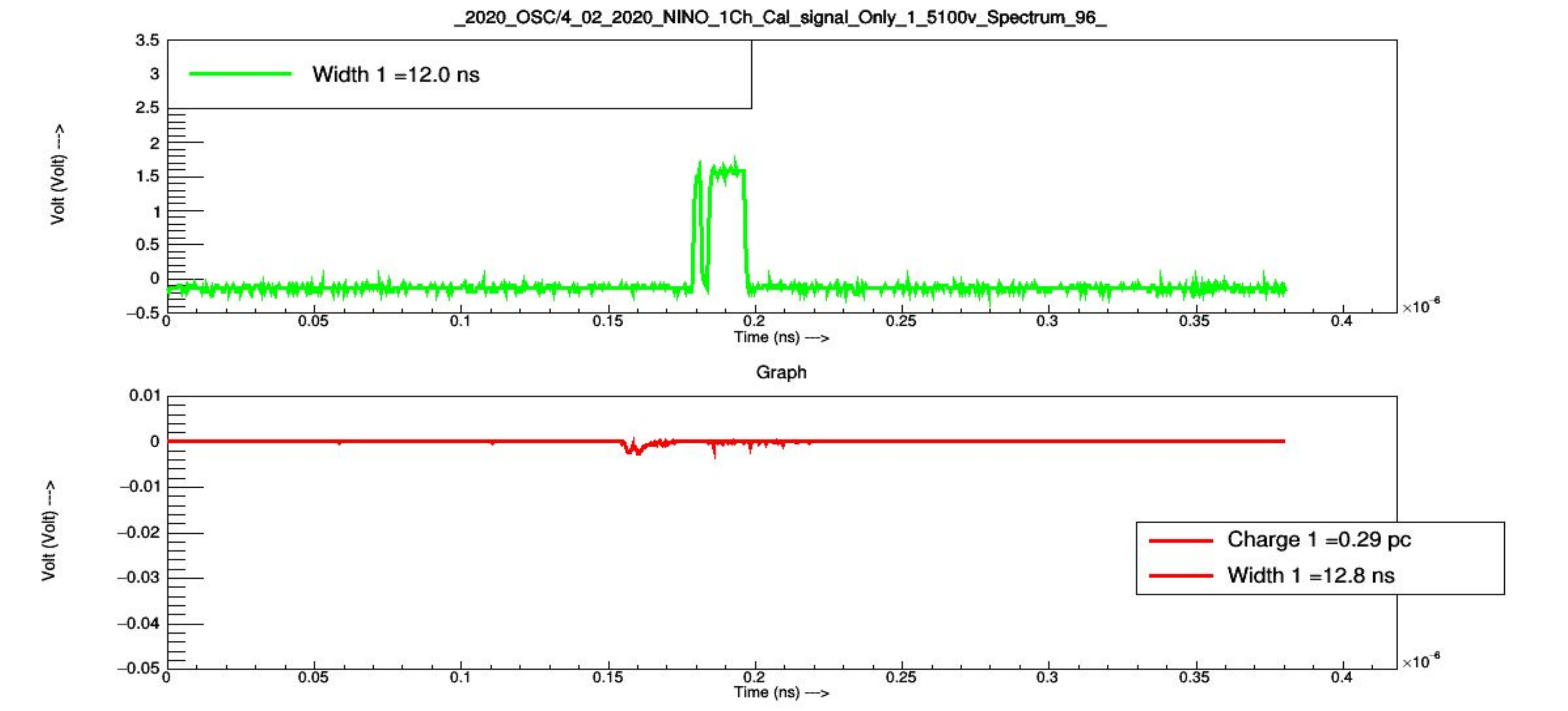




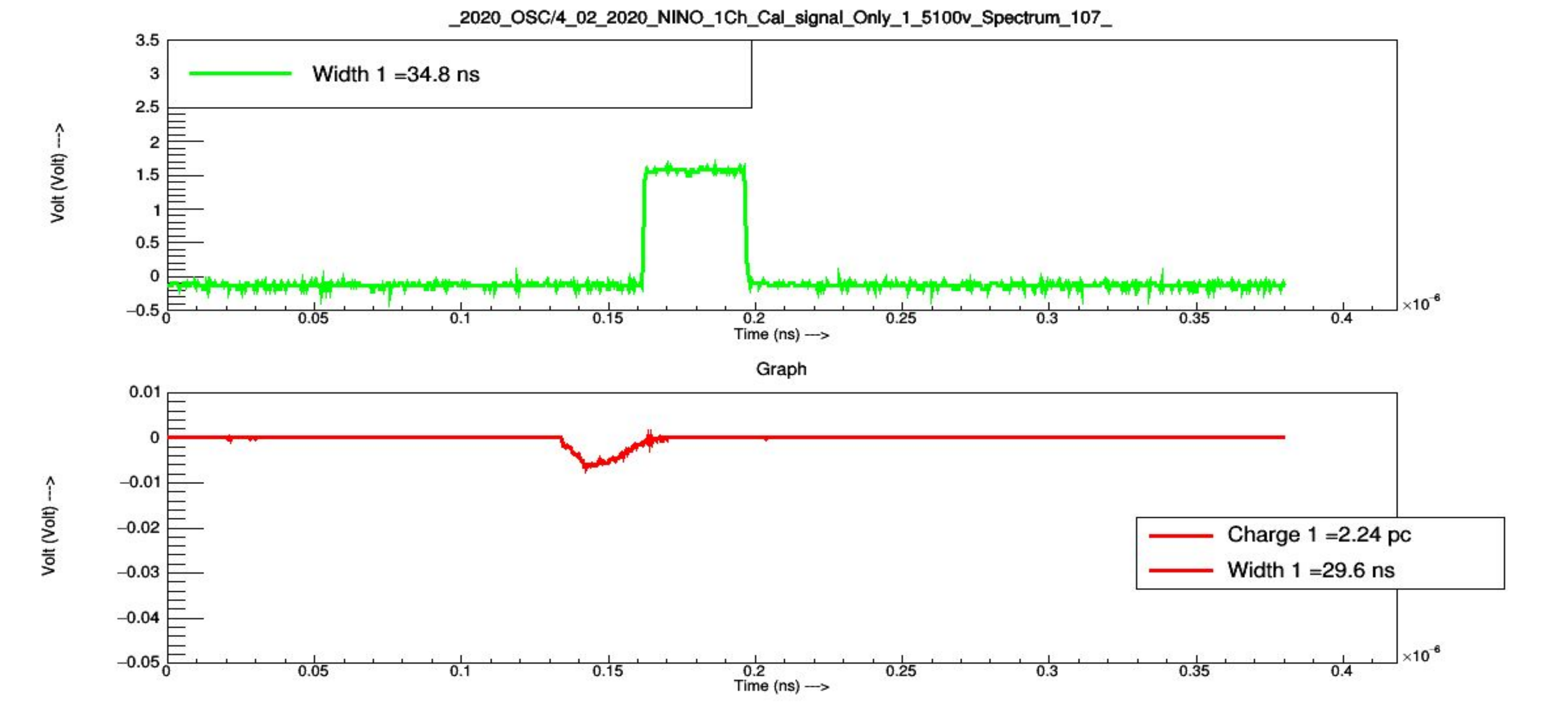
- 8 channel readout
- Individual drivers for differential input
- Input threshold control 10fc to 100 fc
- Placement of Readout close to the detector

- Time Width of o/p proportional to ToT of i/p.
- Charge content of signal proportional to pulse area
- Width of o/p of NINO can predict the center of multiple strips

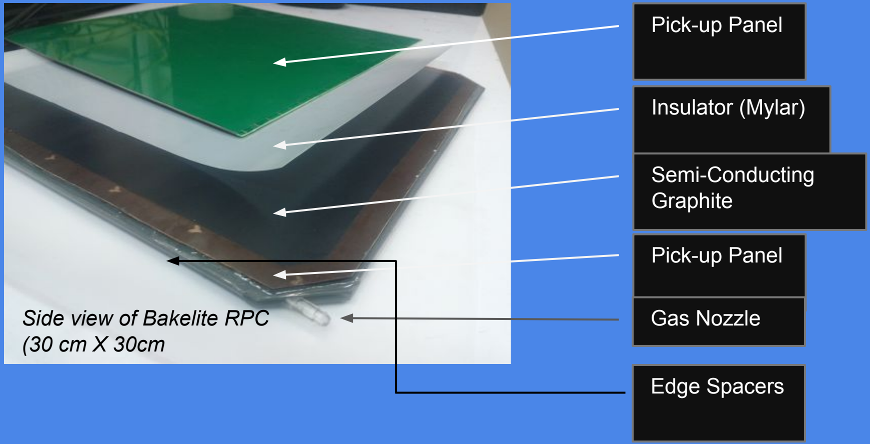
Small i/p pulse



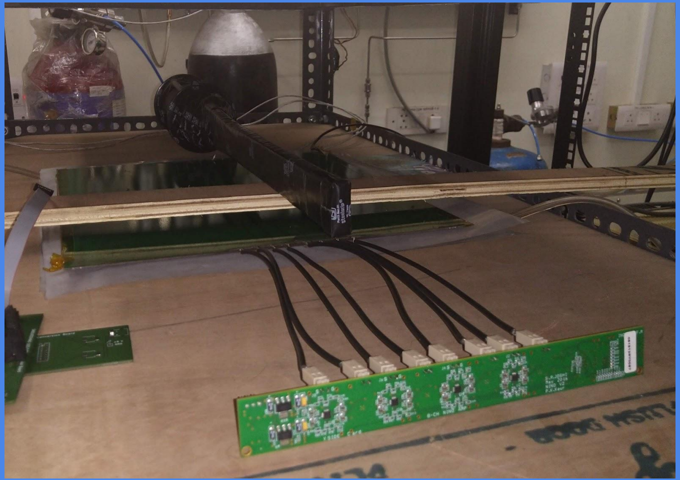
Larger i/p pulse

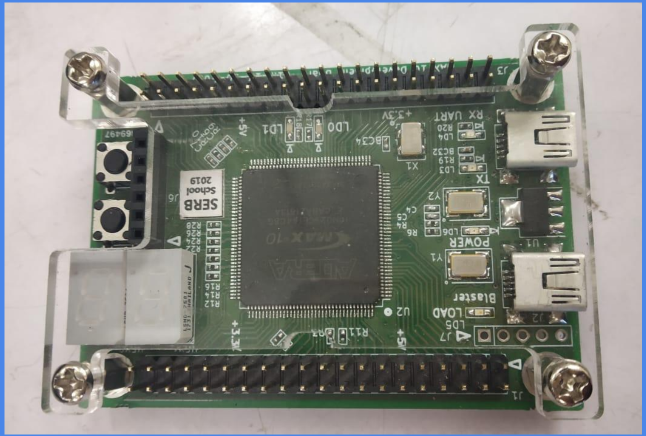


The Experimental Setup



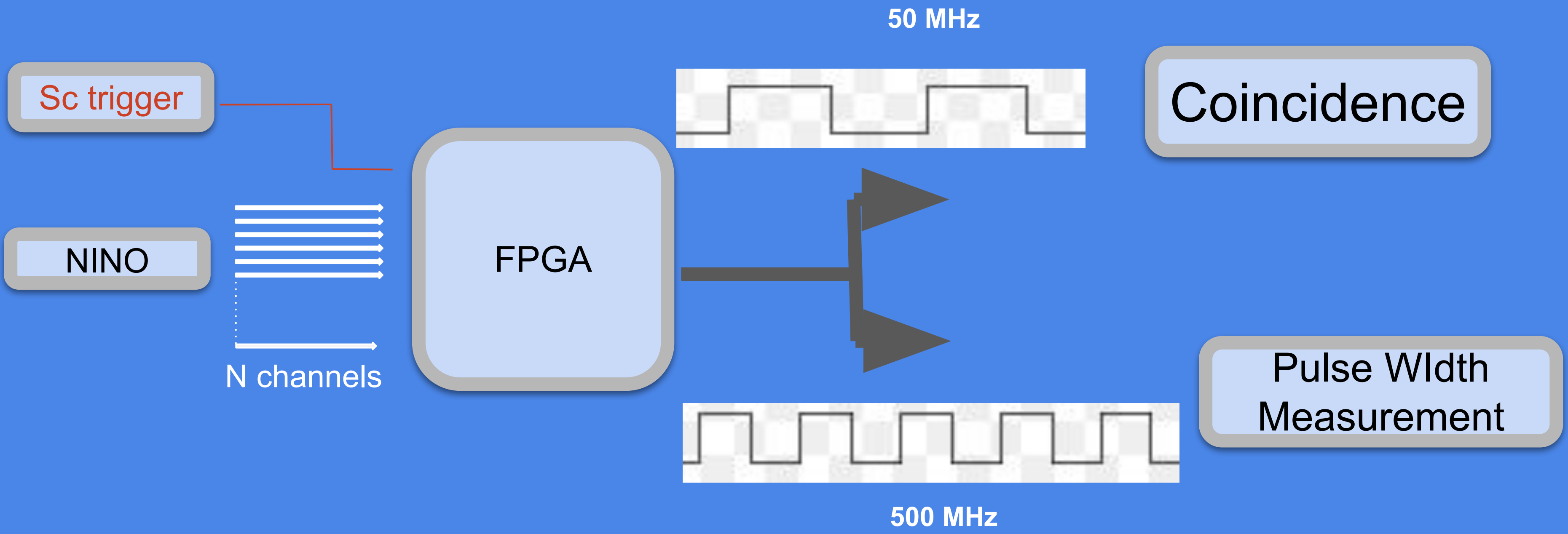
Side view of Bakelite RPC (30 cm X 30cm



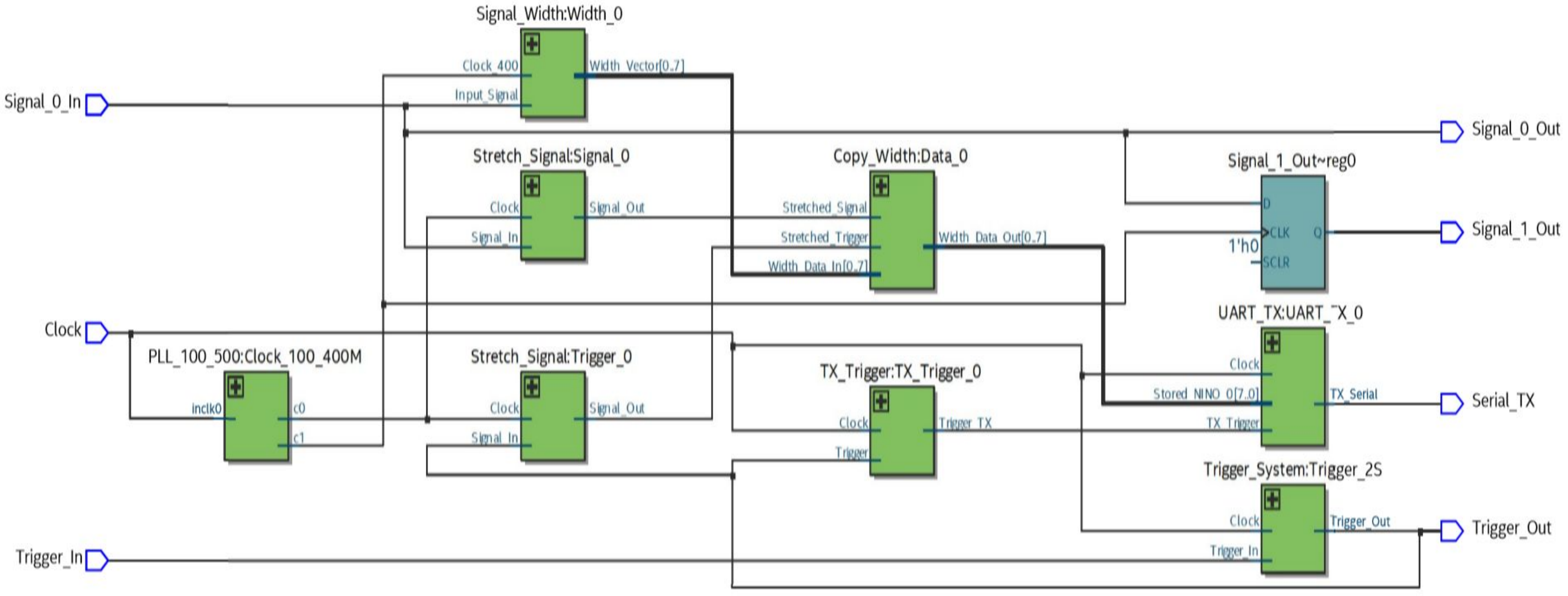


- Freon: Isobutane 95:5
- The muon triggered is obtained from coincidence of 3 plastic scintillators.
- Strip width is **1 cm.**
- Only **one strip** is triggered. 3 strips from either side have been studied.
- **Altera Max 10** FPGA board.

The FPGA Based DAQ



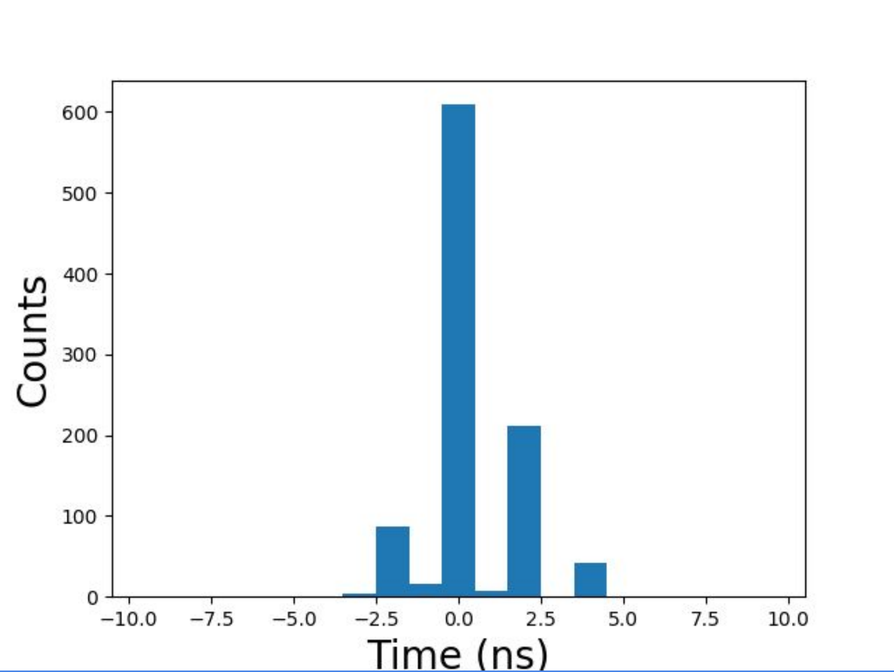
The RTL diagram of the FPGA program



Results

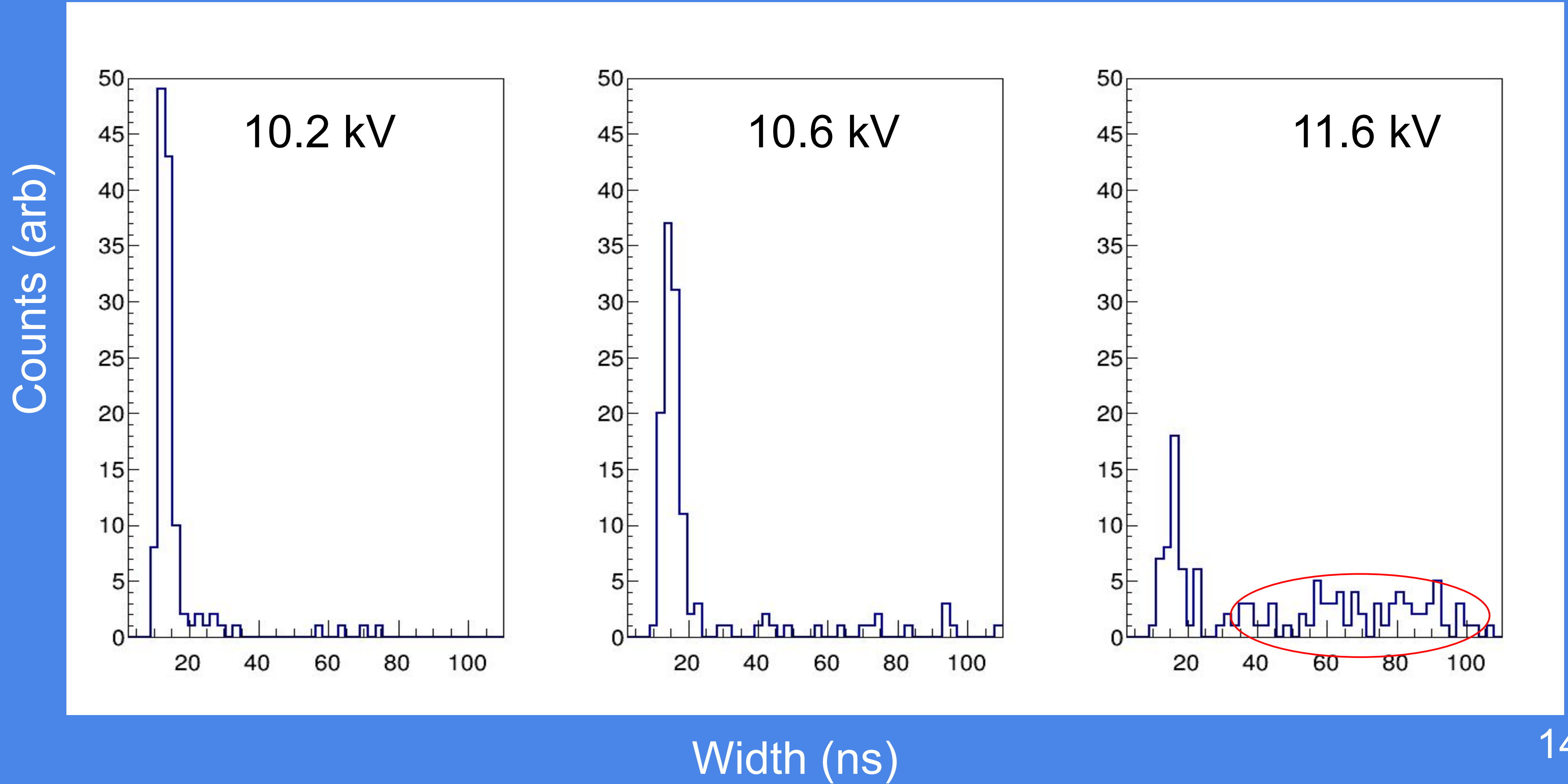
Comparison of Oscilloscope and FPGA pulse widths

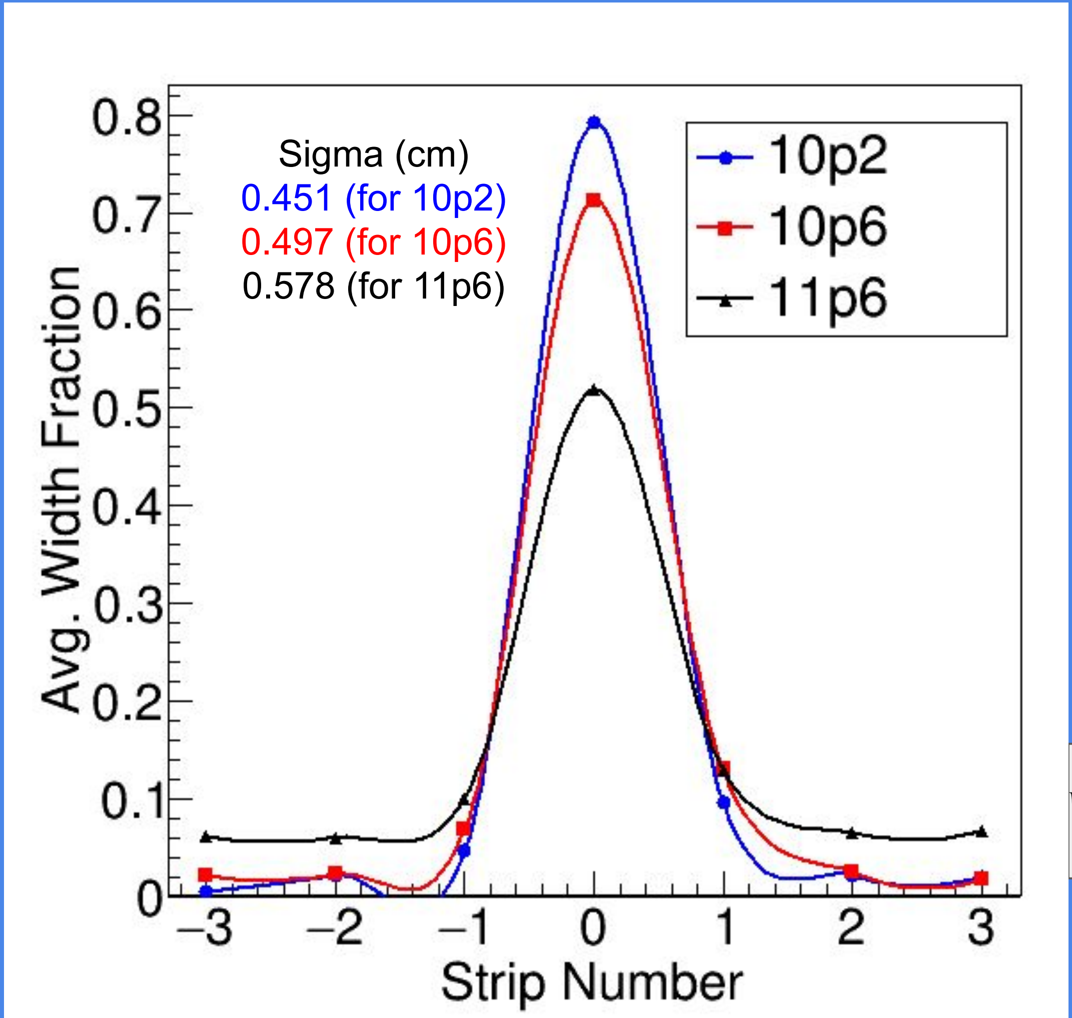
- A 60 ns pulse (from a pulse generator) was measured by both MSO-4104B Oscilloscope and 500 MHz clock of FPGA.
- 2 ns offset was added to the difference.



Difference of pulse widths measured in Oscilloscope and FPGA

Pulse Width at different Working Voltage

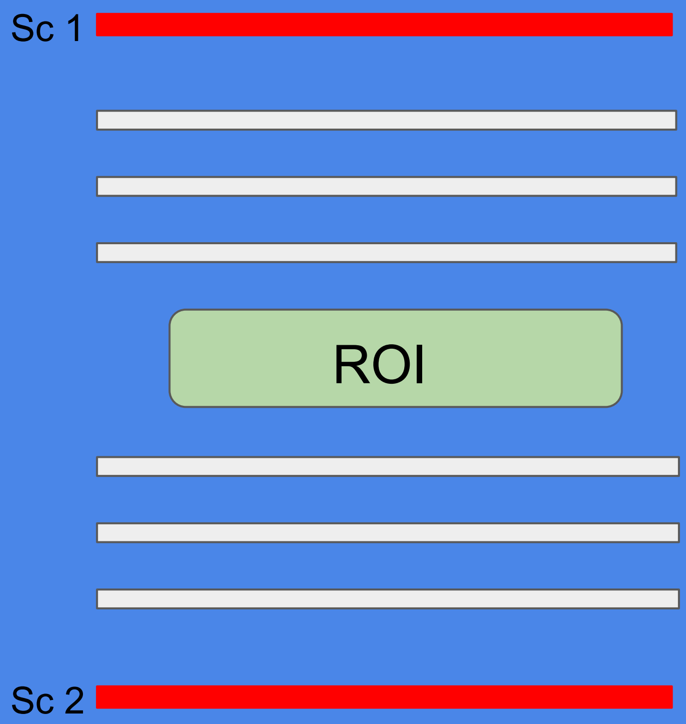


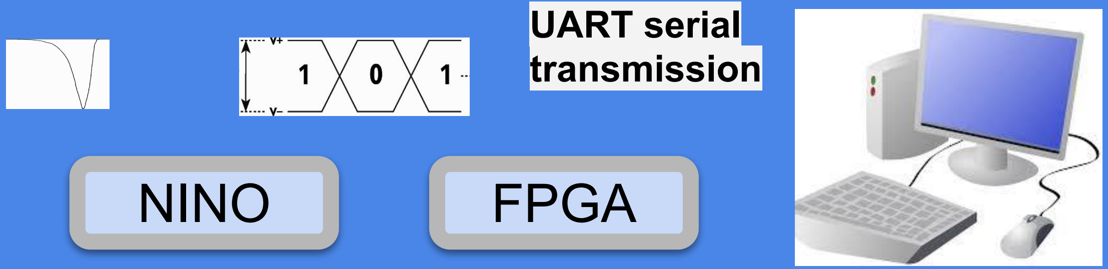


- Signal width obtained from 1000 events.
- The Center strip is triggered.
- Tracking is better in avalanche mode.

$$Width\ Fraction\ of\ \ the\ n^{th}\ strip = \frac{Width\ of\ \ the\ n^{th}\ Strip}{\sum_n Width\ of\ \ individual\ strips}$$

Proposed Tomography Setup





- Front-end NINO boards
- FPGAs for coincidence and decision for TX
- The UART serial transmission to PC
- Data obtained reading the port using Python/C++ scripts

Summary

- TOT measurement property of NINO has been exploited to find the center of the hits.
- A simple FPGA based DAQ for the cosmic muon imaging system.
- Use of PLL to use 2 different clks, one for event selection(50 MHz) and other for pulse width measurement (500 MHz).
- Pulse widths of the detector at avalanche and nearly streamer mode voltages have been studied.

Future Targets

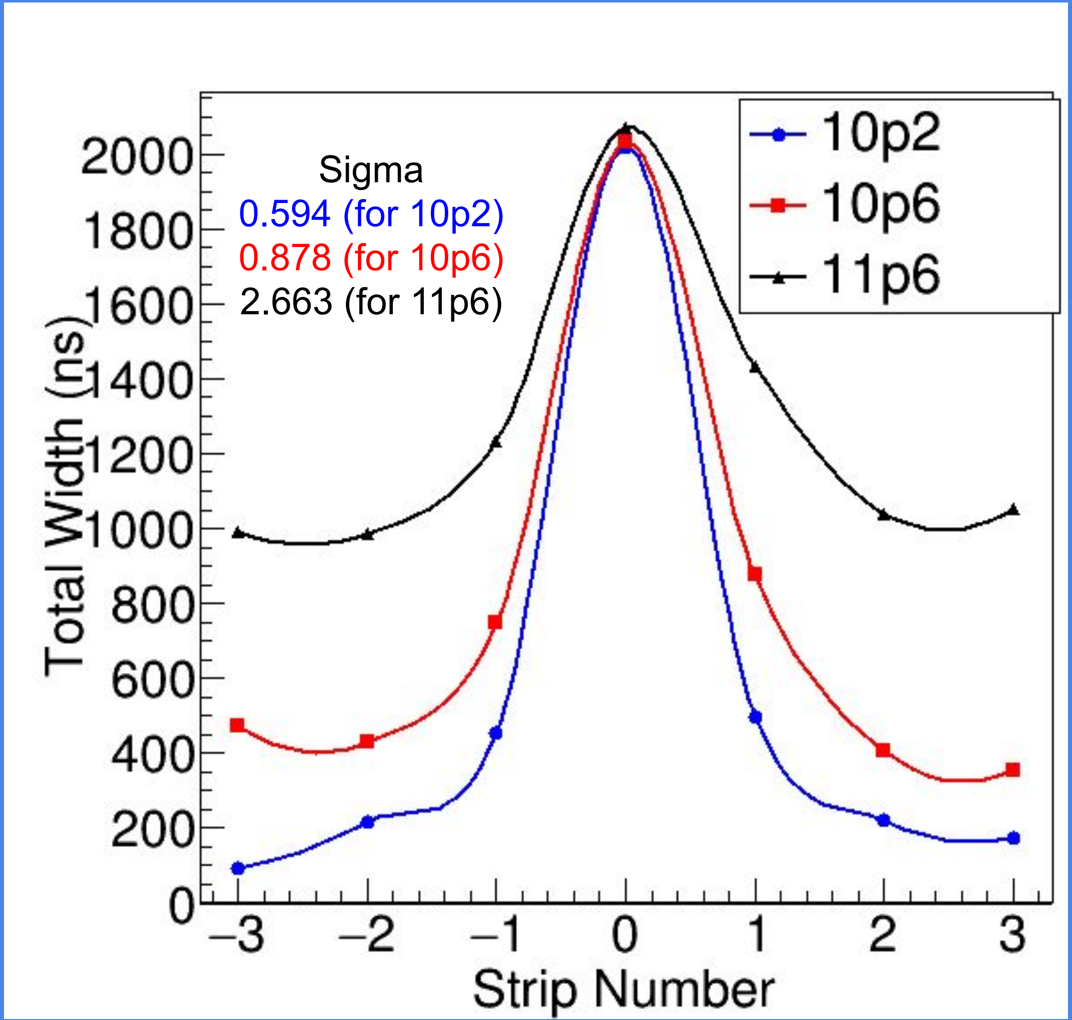
- Calibration of o/p pulse and i/p charge has to be done.
- Use of thinner strips for better resolution
- Better FPGA clk for precise measurement,
- Utilize in the muon imaging system.

Acknowledgements:

- SINP MPGD group
- DST Govt of India
- TIFR DHEP (INO)

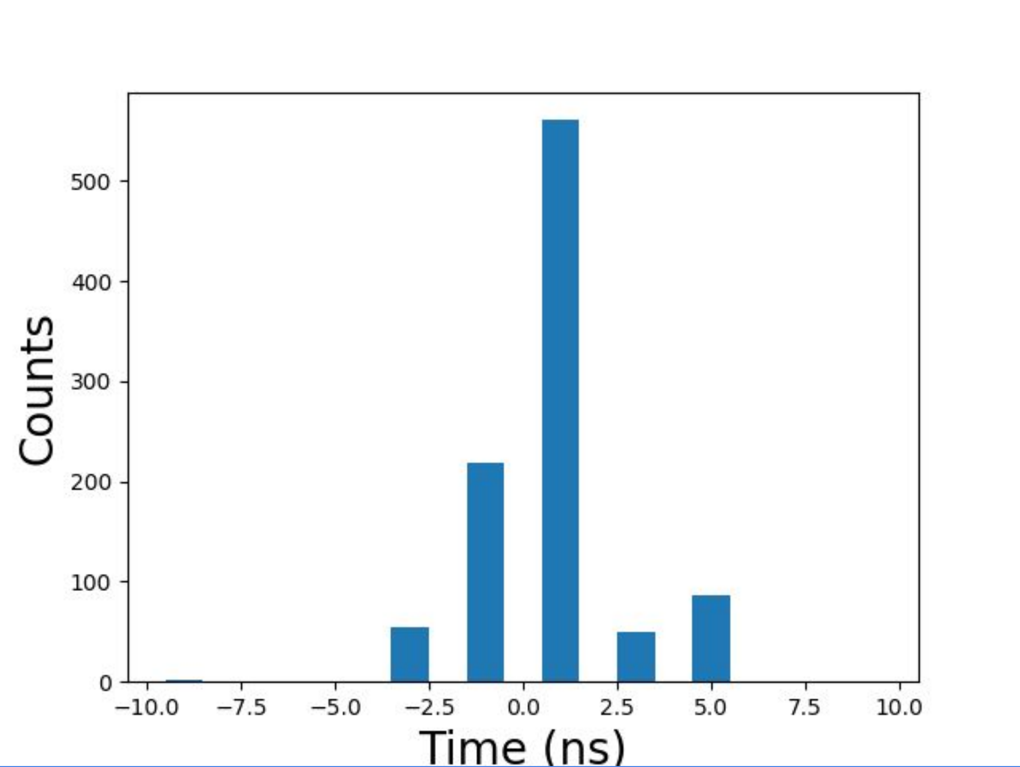
Thank You......

Back Ups

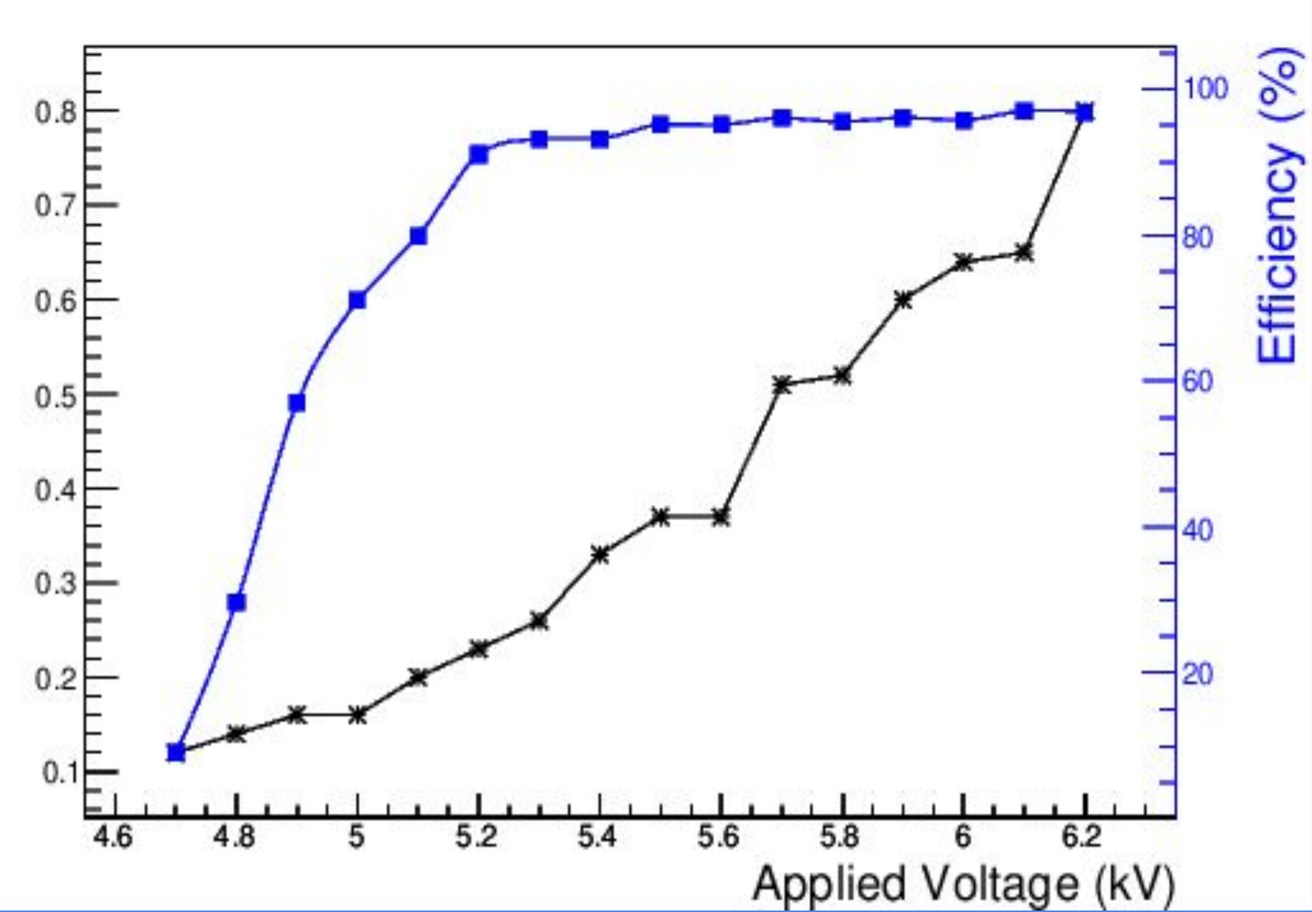


- Total signal width obtained from 1000 events.
- The Center strip is triggered.
- Tracking is better in avalanche mode.
-

Comparison of FPGA and Oscilloscope

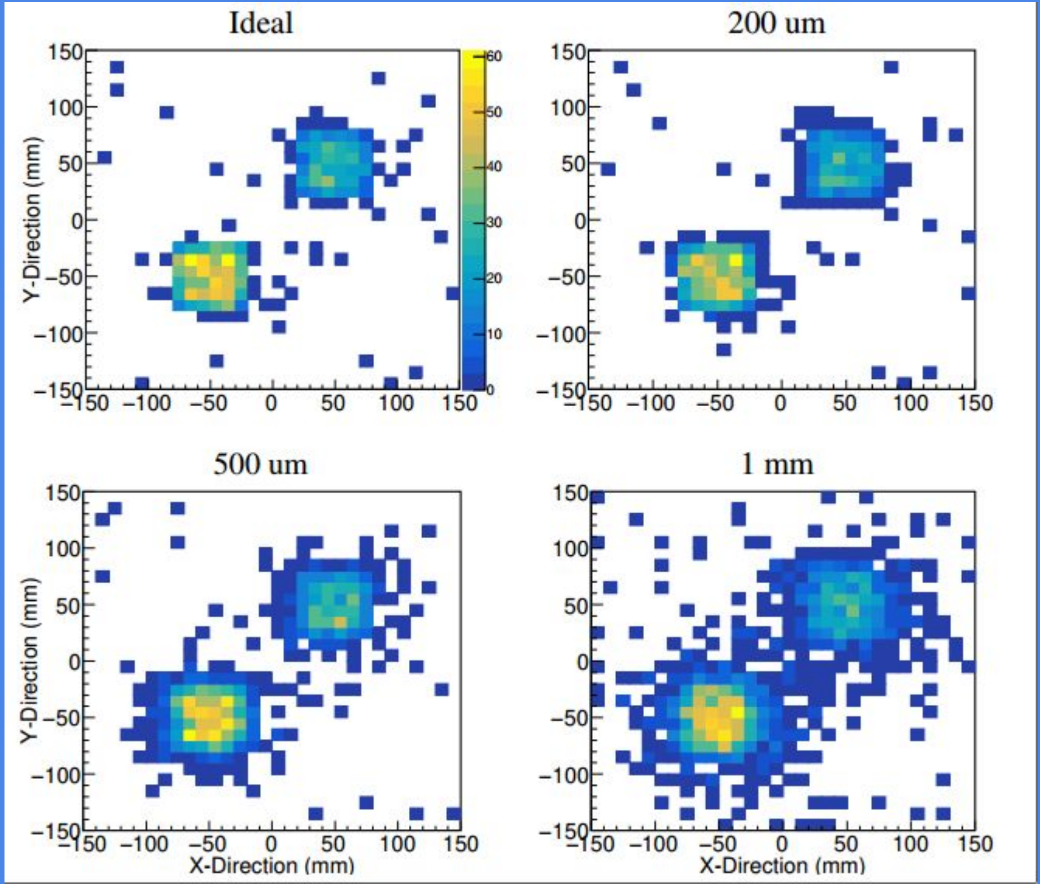


VI curve and Efficiency



HV per One Channel

Different Resolutions



Lead on left
Iron on right

- Altera/Intel® MAX® 10 FPGA – *10M02SCE144C8G*
    - 2000 Logic elements (LEs)
    - 108 Embedded memory (Kbits)
    - 12 User flash memory (KBytes)
    - Single Internal Configuration memory
    - 16 Embedded 18 x 18 multipliers
    - 2 General-purpose PLLs
    - 101 Maximum FPGA I/O pins
- Configuration Status and Set-Up Elements
    - On-board USB-Blaster compatible circuit for FPGA programming and debugging
- Expansion Header
    - Two 40-pin headers (GPIOs) provide 68 3.3V I/O pins
    - Two 5V power pins, two 3.3V power pins and four ground pins
    - One 6-pin header provides four 3.3V digital I/O pins one 3.3V power pin and one ground pin, compatible with Digilent Pmod™ connector.
    - General User Interface Peripherals
        - 2 Yellow LEDs
        - 2 Push-buttons
        - 2 7-Sement LED Displays
    - Clock System
        - On-board 50MHz clock oscillator
    - USB to UART Interface
        - CH340G based USB-UART converter for interfacing to a PC, including TxD and RxD LEDs