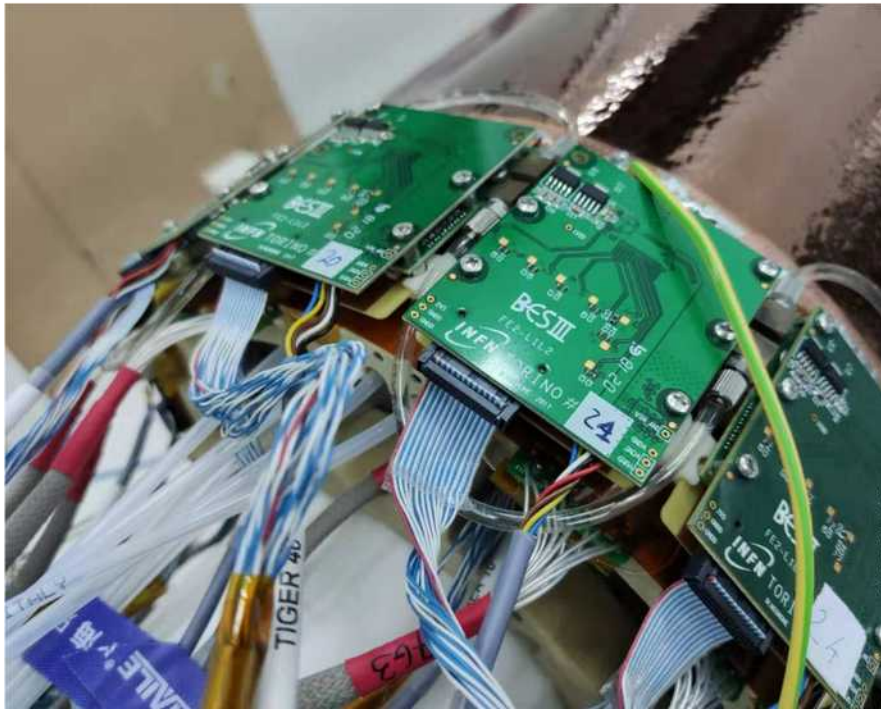
CGEM Electronics Update



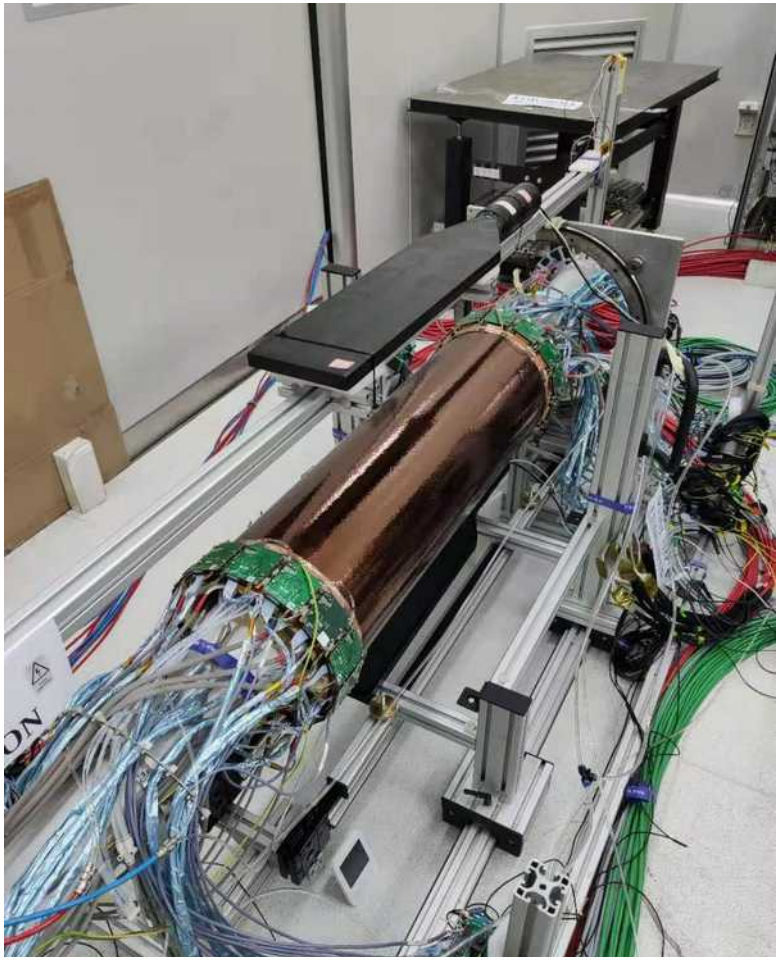
G Mezzadri – (INFN Ferrara) – gmezzadr@fe.infn.it
On behalf of the working group
CGEM-IRC meeting – 2019/07/15

Introduction

Milestone 3: Integration

Completion of the integration test of Layer-1 and Layer-2 with TIGER chips;

1) operation of the electronics at a threshold of 3-4 fC;
2) efficient cosmic track reconstruction based on strip-clustering digitization.



Introduction

Milestone 3: Integration

Completion of the integration test of Layer-1 and Layer-2 with TIGER chips;

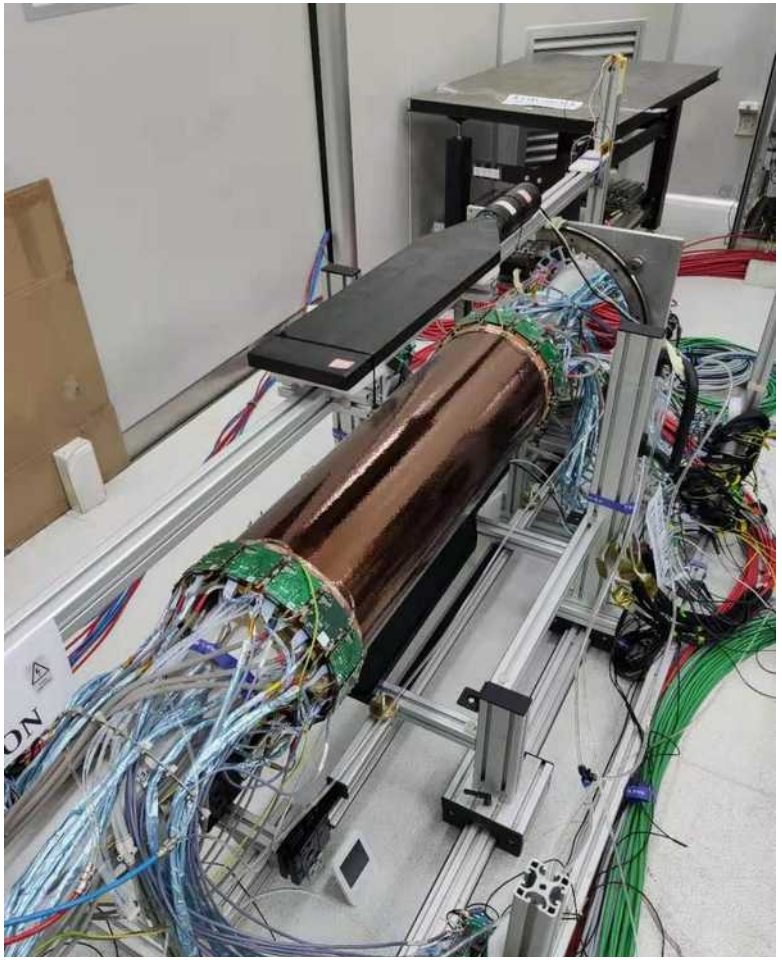
1) operation of the electronics at a threshold of 3-4 fC;

2) efficient cosmic track reconstruction based on strip-clustering digitization.

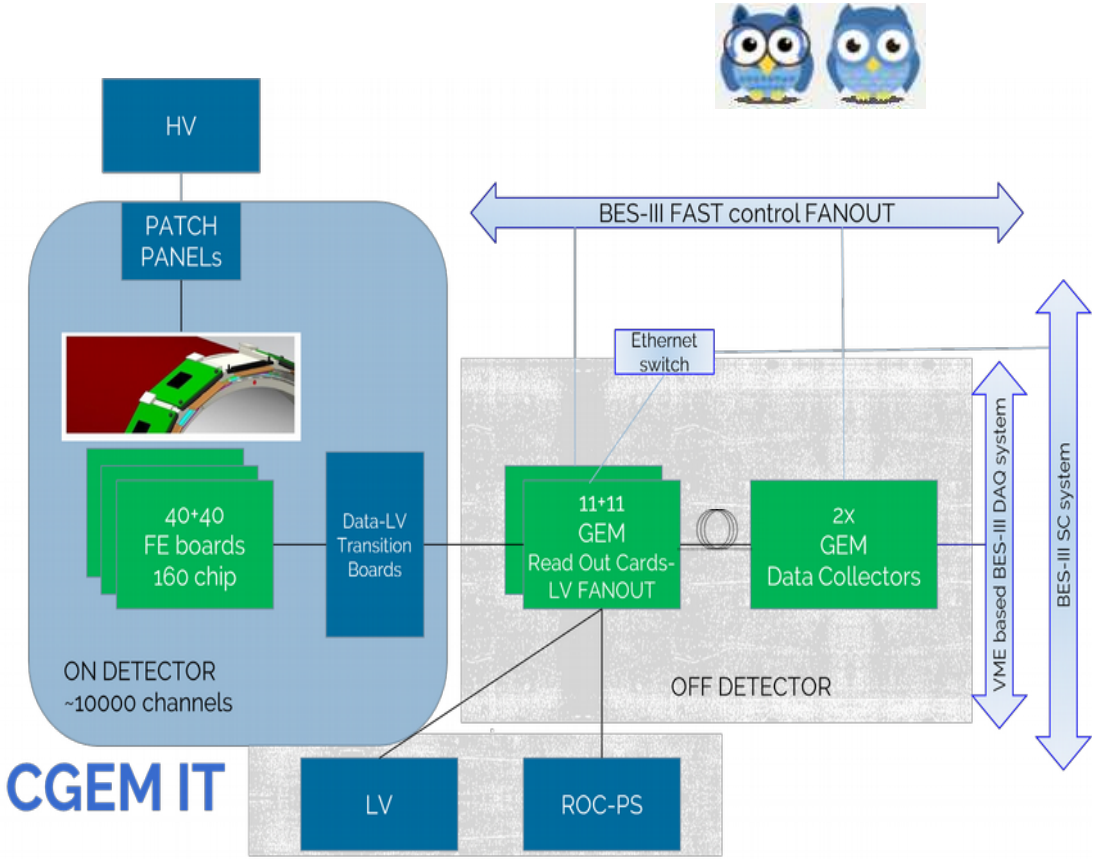
Outline:

- Status of the setup

- Reaching the milestone

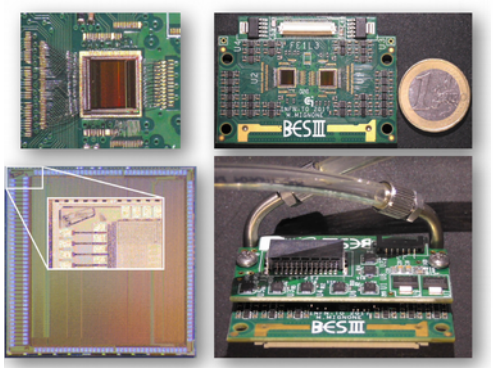


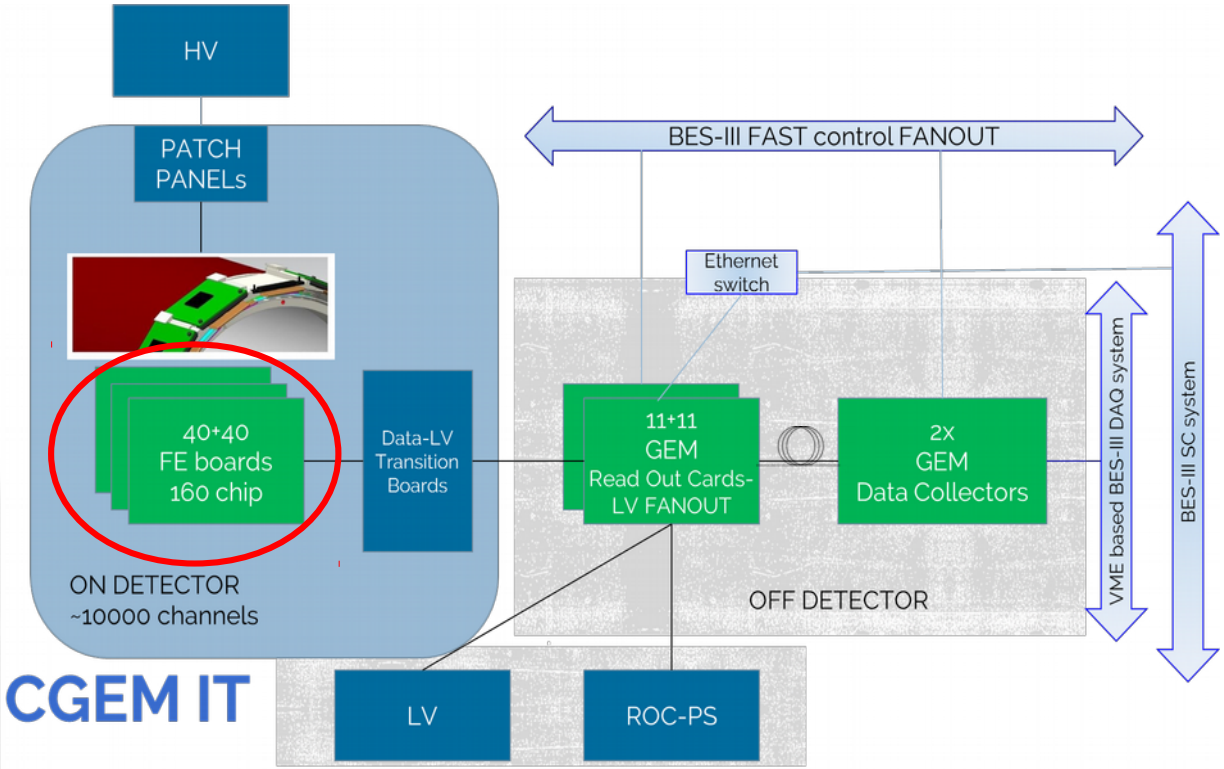
Status of the Setup



On Detector Electronics - Front End - Tiger

64 ch TIGER chip
2 **TIGER**s per **FEB**
44/80 FEB already **installed in L1+L2**





TIGERs status

(INFN-TO)

All items needed are already in IHEP

Dead channel in the first batch

	Total number of chips in the first batch	Dead channels	Total number of channels	Percentage of dead channels
L1	34	4	2176	0.18%
L2	58	3	3712	0.08%
L3	74	8	4736	0.17%
Tot	166	15	10624	0.14%

Calibration curve for each channel has been measured

2 chips do not send digital TP, they will be replaced

Spare FEBs:
L1: 7 (/16)
L2: 12 (/28)
L3: 14 (/36)

Up to now, replaced only 5 FEBs which have shown problems during the installation procedures or immediately after

Spare heat-sinks:

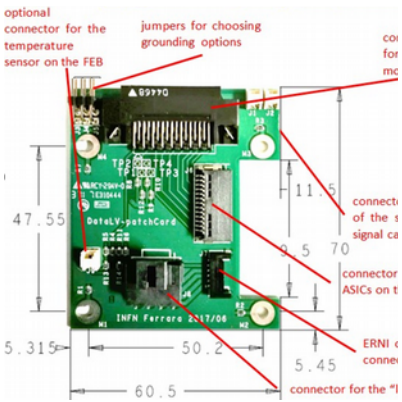
L1-L2 type available
L3-type in production

Of the 80 tested during FEBs calibration, only two have shown problems and have been replaced

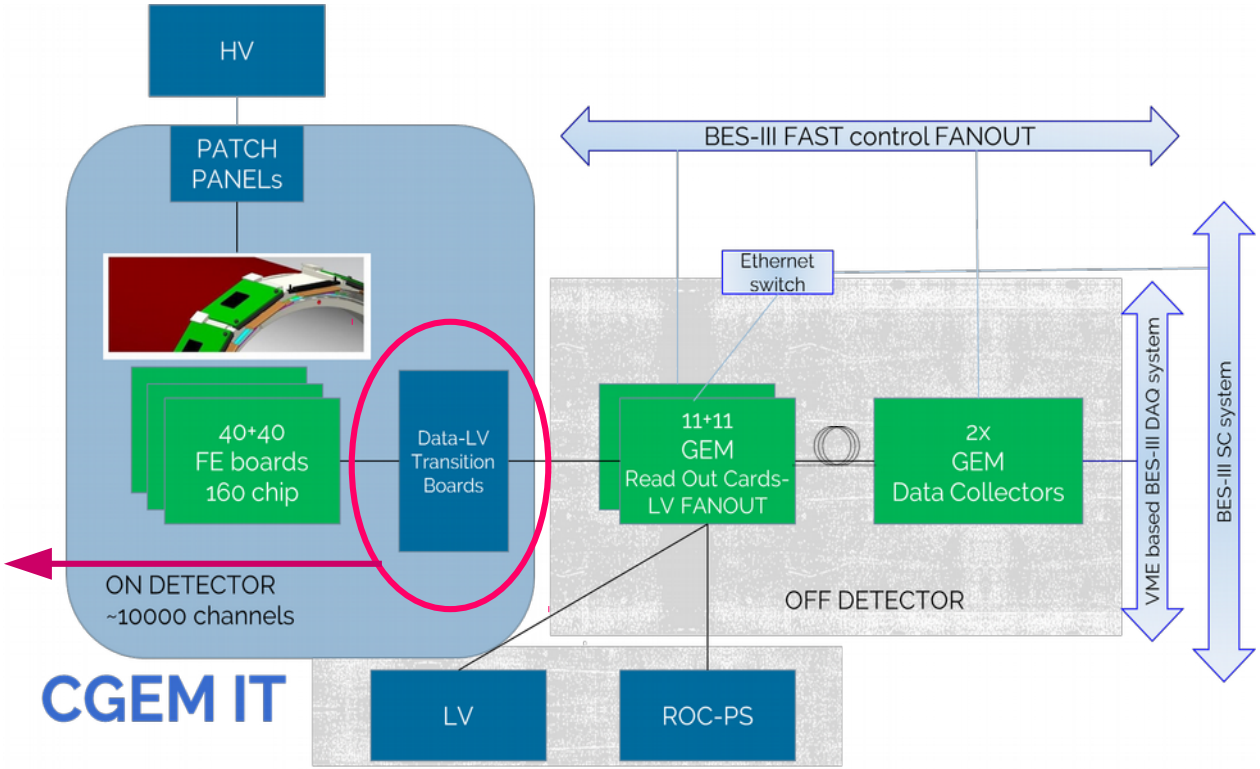
On Detector Electronics – DVLPC

All items in Beijing
80 needed
100 available

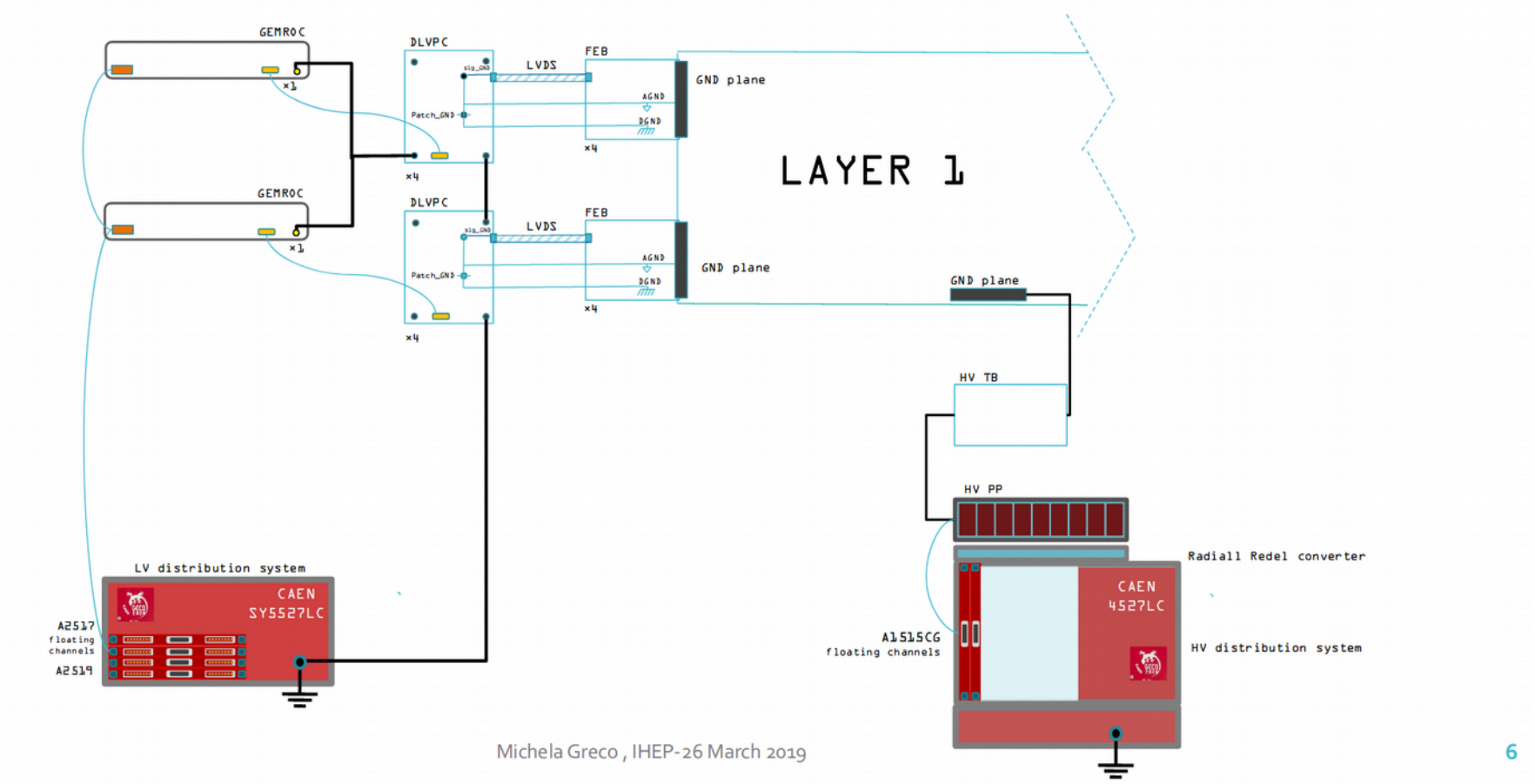
Center of the grounding scheme



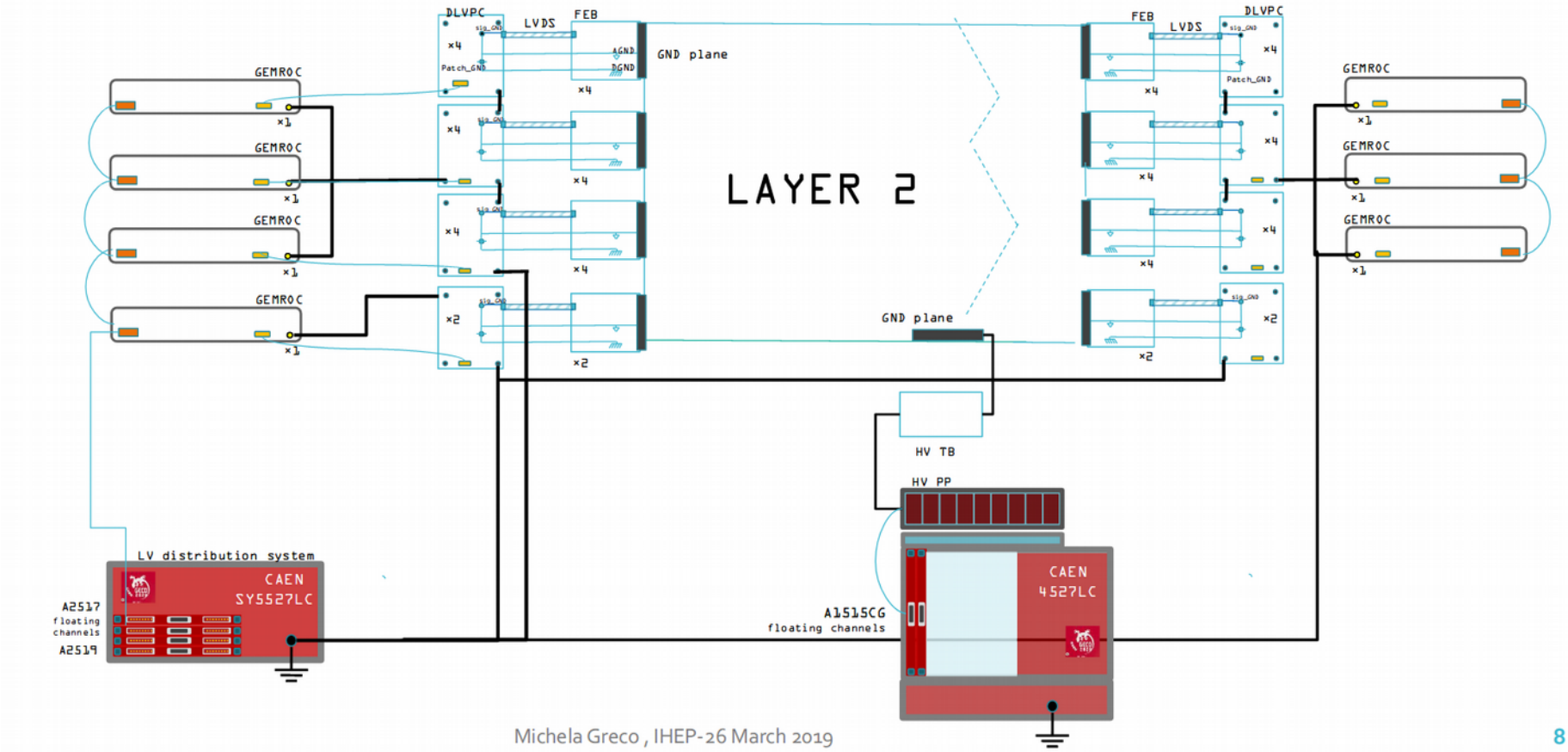
(INFN-FE)



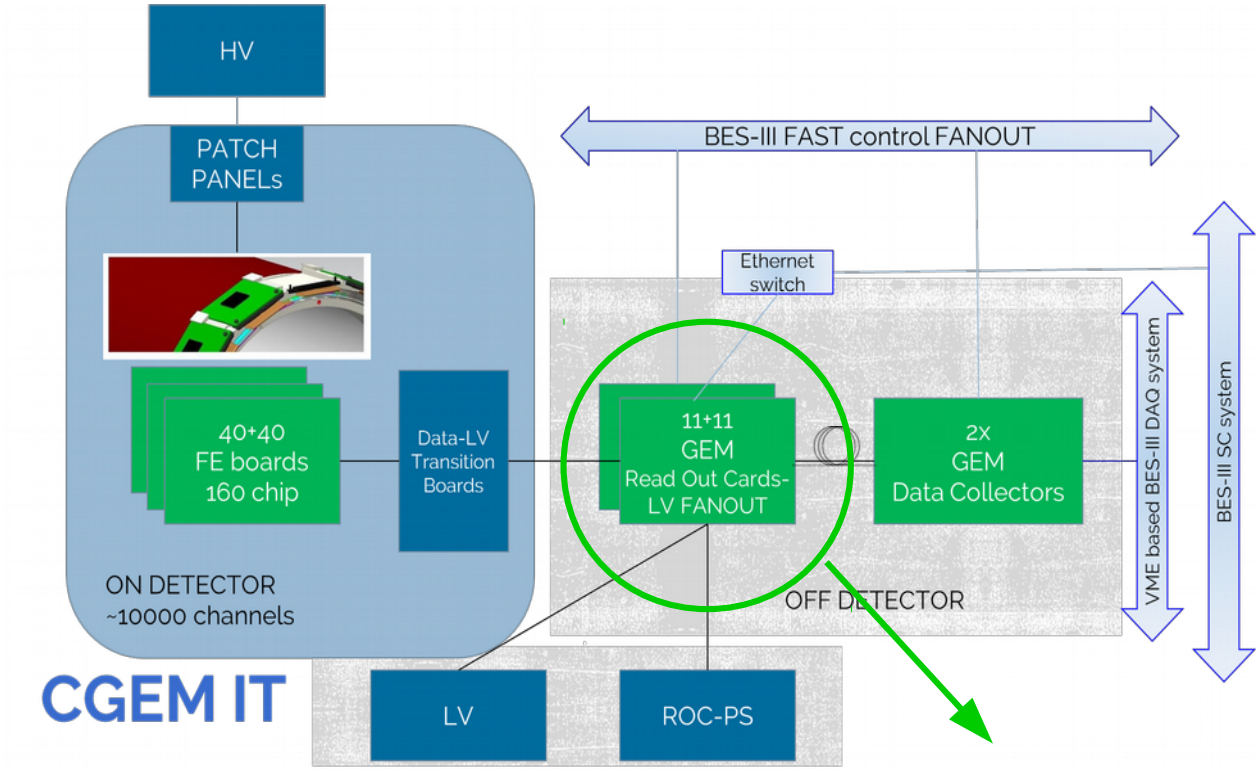
Grounding condition – L1



Grounding condition - L2



Off Detector Electronics – GEMROCs



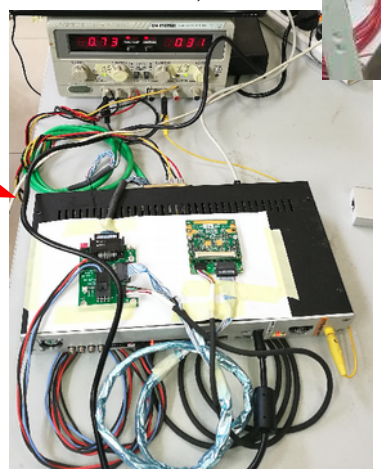
4 FEBs per GEMROC
11 GEMROCs already operating

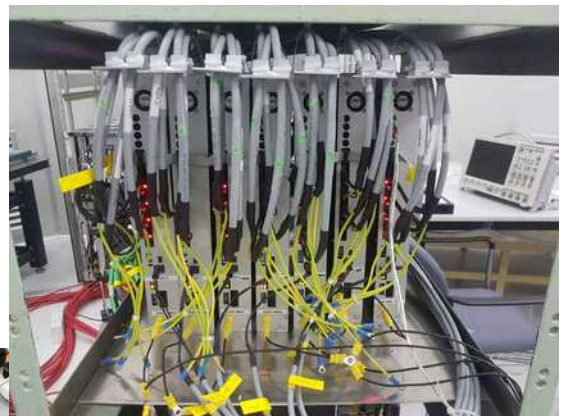
Status of the GEMROCs

(INFN-FE)

25 GEMROC modules manufactured:

- 1 in Torino for software studies
- 1 in Ferrara for firmware development
- 23 items are in Beijing:
  - 22 in the clean room (1 GEMROC is being used temporarily as a clock Fan-Out module. More on this later...)
  - 1 in BESIII DAQ Lab:



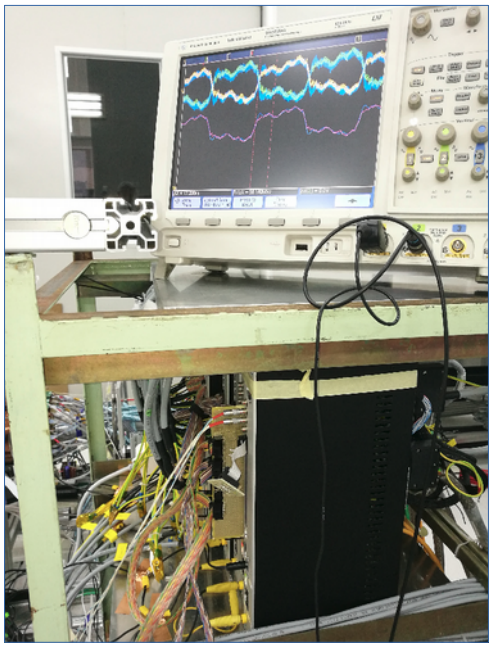


L2

L3

L1

Timing Fan Out Module



One GEMROC has been temporarily modified to distribute Fast Control Signals (FCS) to the GEMROCs in the cosmic test setup at IHEP.

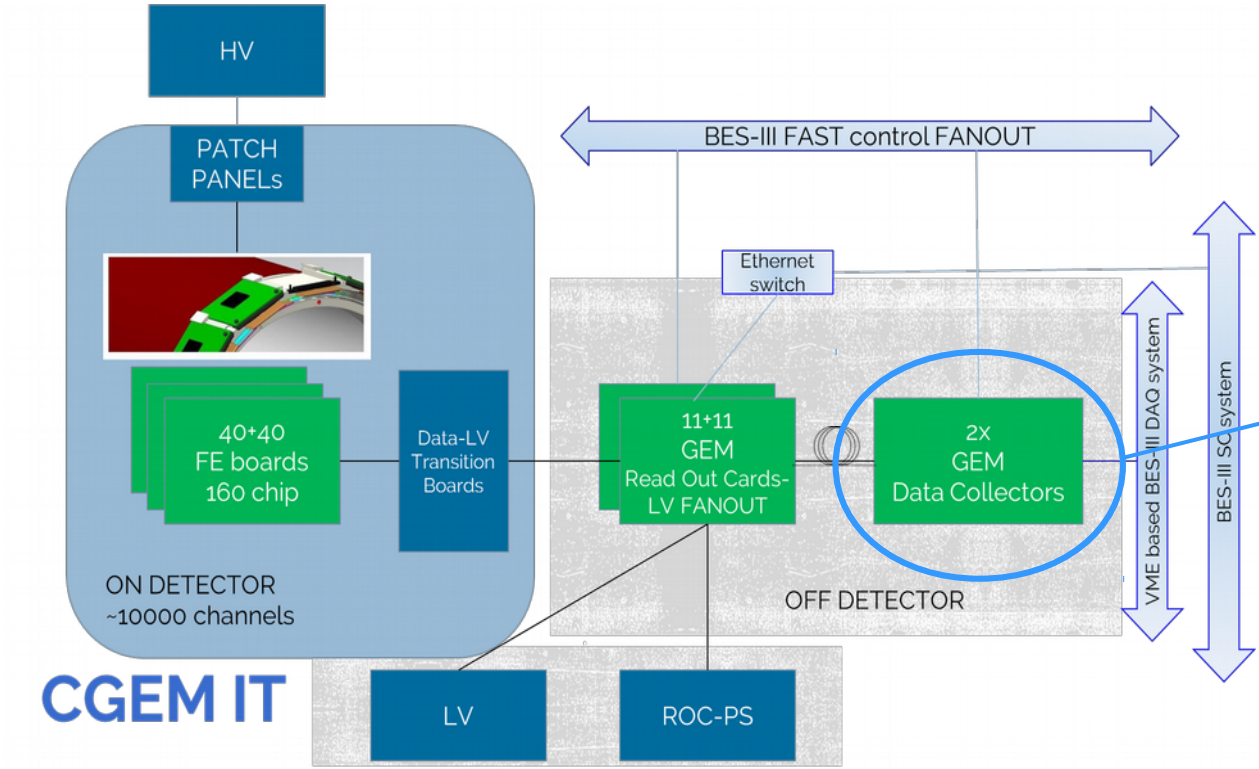
Features of the Timing Fanout Module :

- Generation of the main clock for all the GEMROCs in the setup
- Fanout, over 4 identical ports, of:
  - **Clock** : internally generated.
  - **"In-time"** signal : received from the PMT front end. Used to generate a test pulse in coincidence with the cosmic event to a dedicated TIGER channel
  - **Trigger** : received from a delay module. The signal, arriving 8.6us after the "In-time" pulse is used to trigger the event readout
- Programmable self generation of all fast timing signals listed above.

Effects of its introduction in the recent integration week:

- It has allowed full synchronization (through a common Clock and Trigger signal) across all GEMROCs
- It has improved the system stability by distributing a slower (¼ BES-III clock frequency) and better terminated reference clock

Off Detector Electronics – GEM-DC



2 needed
3 available

Designed for WASA and KLOE2.

Modified version to comply with BESIII requirements

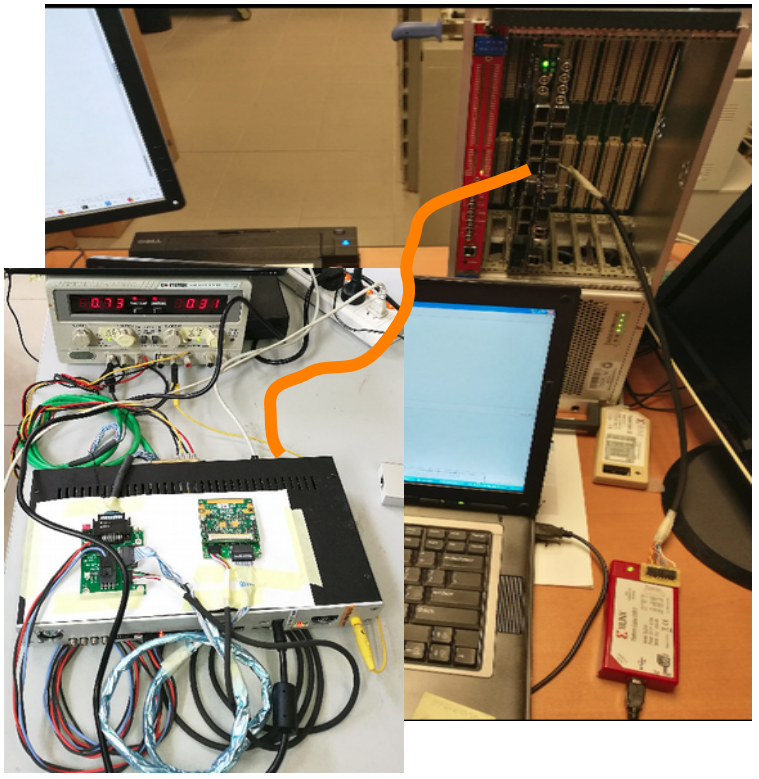
Off Detector Electronics – GEM-DC

(Uppsala University)

3 GEM-DC modules are available:

- 1 in BESIII DAQ Lab, delivered on June 13th 2019 for the first integration tests:
  - **GEM-DC stand-alone test**
    generation of simulated CGEM trigger matched packets
  - **full path readout test**
    TIGER → GEMROC → GEM-DC → VME
- 2 in Uppsala for hardware and firmware implementation

The TIGERs used in this test are configured through the GEMROC ethernet port thanks to the a simplified version of the Graphical User Interface



GEM-DC Integration test

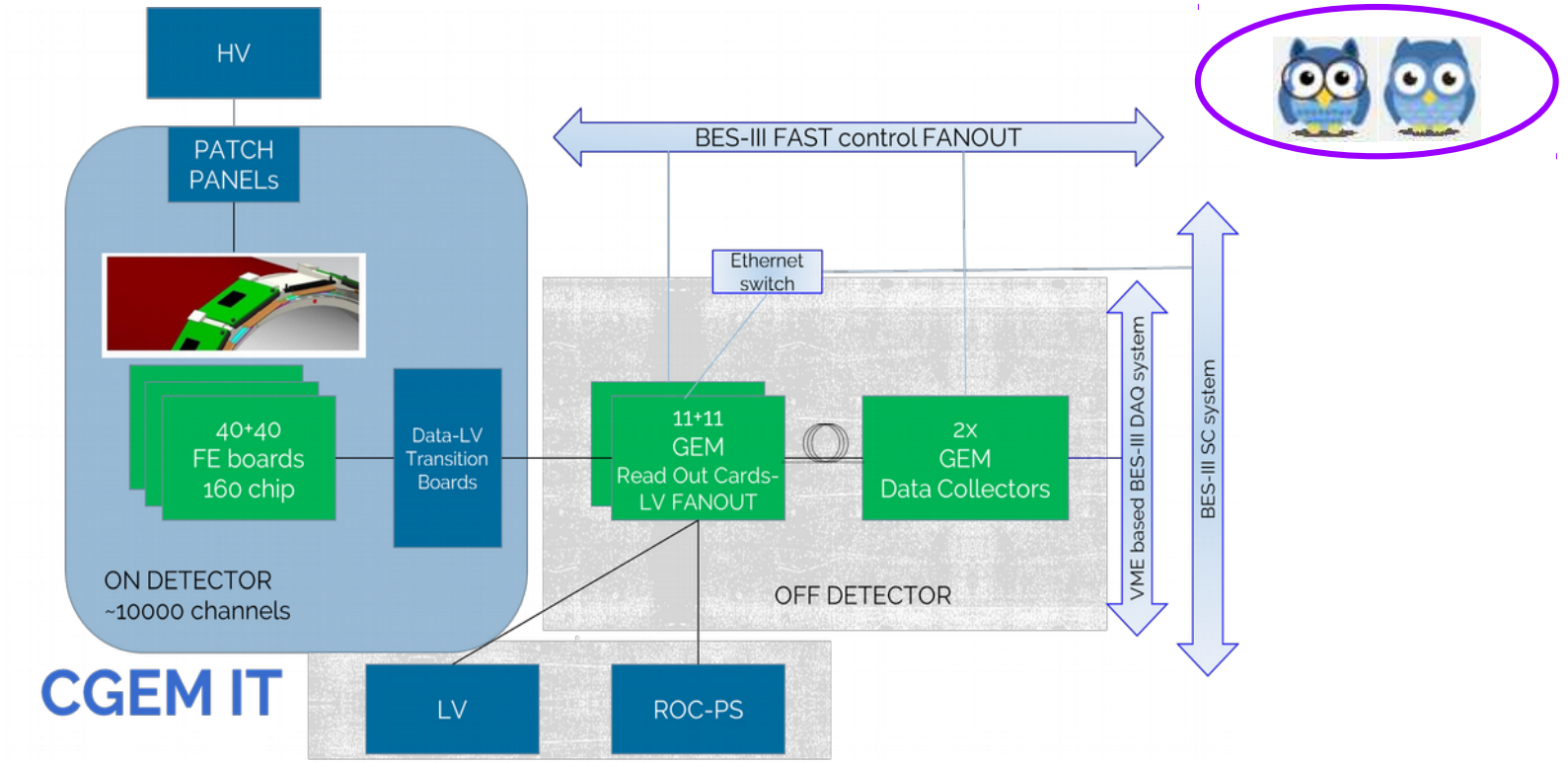
Outcome:

- ALL GEM-DC were successfully accessed via VME (also the one with little different power consumption)
- One GEM-DC was modified to implement generation of **simulated trigger matched data** packets, which were **successfully accessed**
- The same GEM-DC was then connected to a GEMROC sending **real TM (Trigger Matched) TIGER data** over the **optical link** to the GEM-DC. Again the **data were successfully accessed**. Close to real situation!
- VME Block read mode (BERR terminated) was succesfully tested

To be done next:

- Implement VME Interrupt handling in the GEM-DC. The interrupt is to inform the VME CPU that a block read transaction can be scheduled because a fully built event is ready in the GEM-DC data buffer.

Graphical User Interface - GUFI

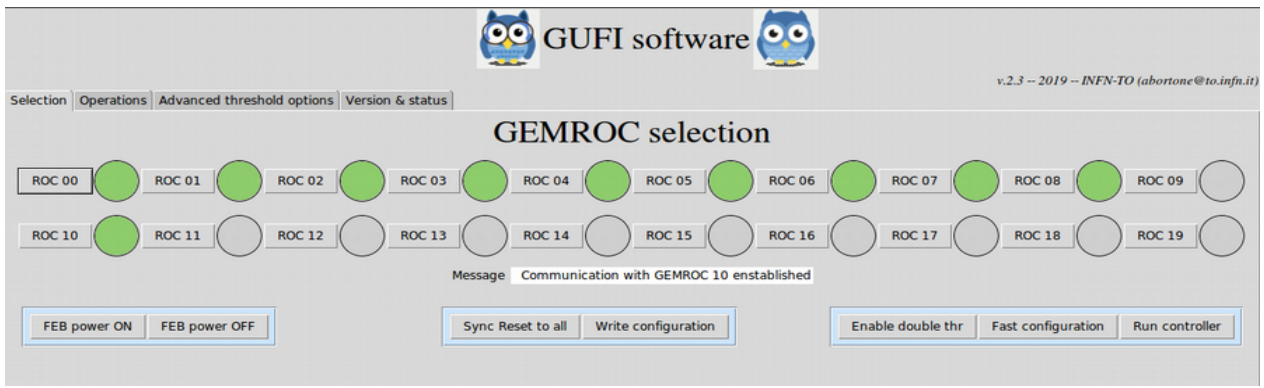


Graphical User Interface - GUFI (INFN-TO)

A Graphical User Interface has been prepared:
GUFI (Graphical User Frontend Interface) v2.3

Features:

- Simplified view for non-expert users and tabs with advanced settings
- Configure GEMROCs and TIGERs, scan and load both threshold, control the communication, set pause, noise scan
- Control the temperature and the currents of analog and digital part
- Run control

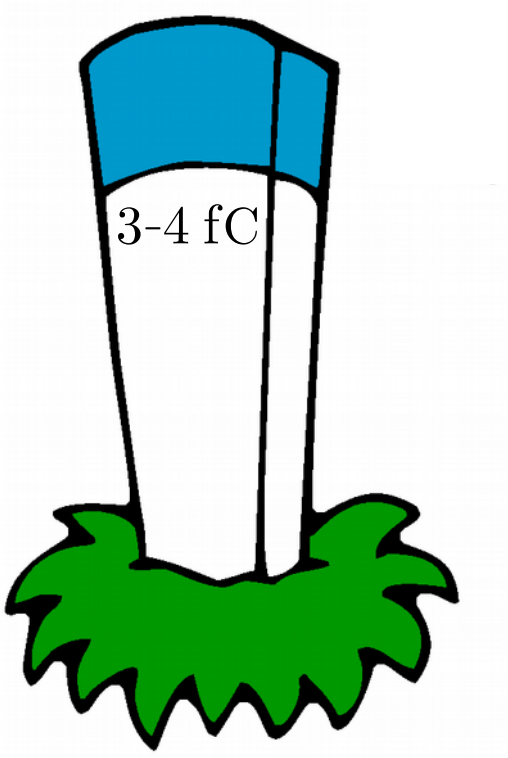


Summary of the hardware status

- Most of the needed hardware already available in IHEP
- Very low failure rate for FEBs (less than 10%) with large number of spares available
- No GEMROC failures in the past months
- Clock and synchronization improved with the new Fan-Out module
- First integration of the TIGER-GEMROC-GEMDC-VME test on-going
- Reliable GUFI system to configure the system and to control the data taking

Reaching the milestone

Operation at 3-4 fC thresholds

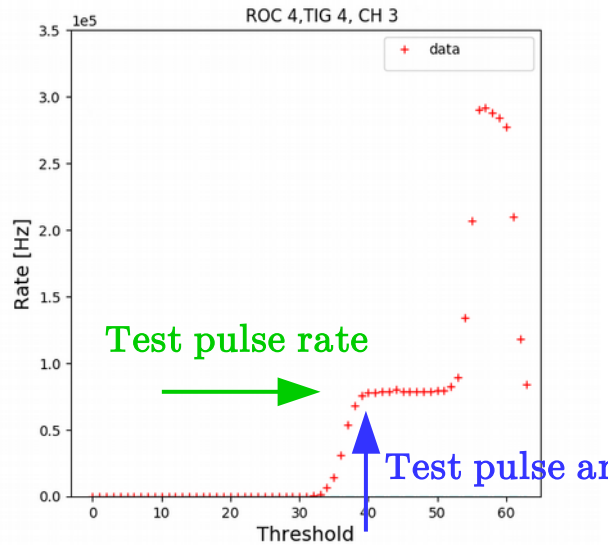


Status of the noise measurements

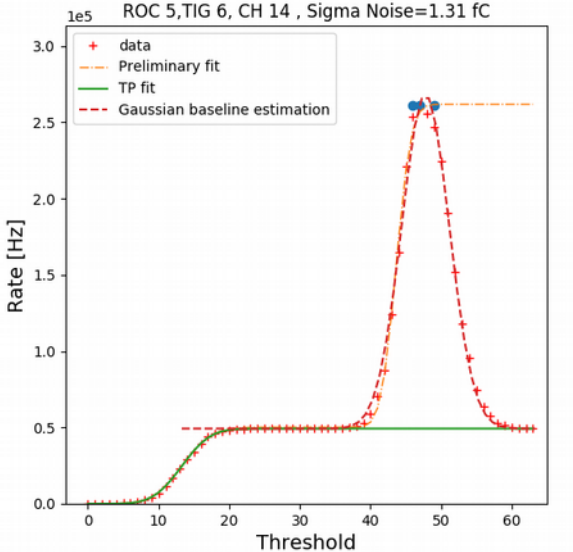
A large effort has been dedicated to study the noise.

Applied threshold on both T and E branch.

Change of paradigma in the noise estimation. Two steps procedure:
1) Inject a fixed number of analog test pulse of known amplitude
2) Fit the full shape to extract S-curve (from TP rise) and baseline



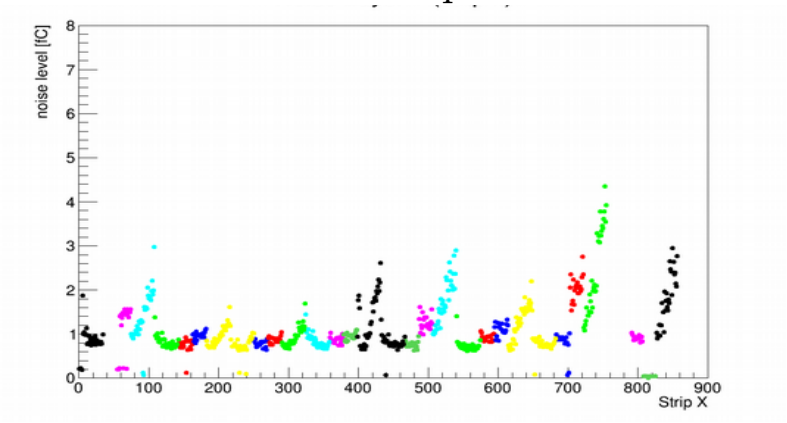
Calibration of the test pulse done channel by channel!



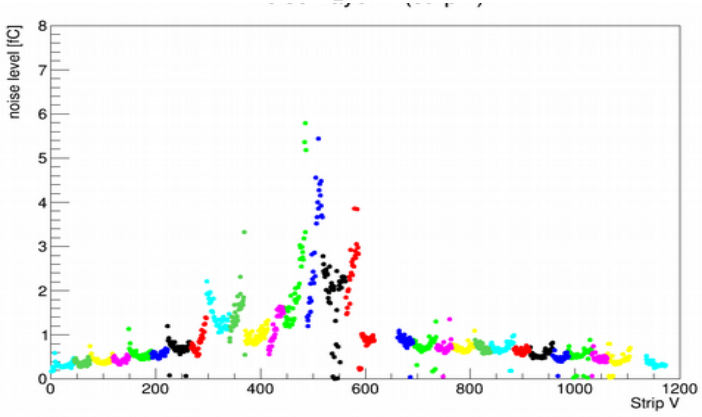
Strip-by-strip noise measurements

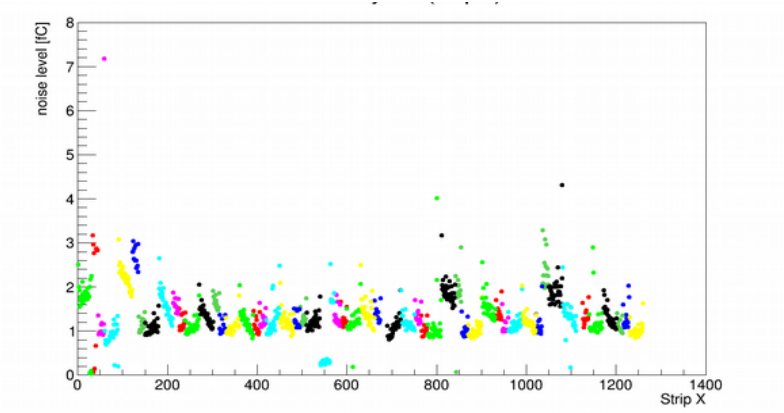
Strip X

Strip V

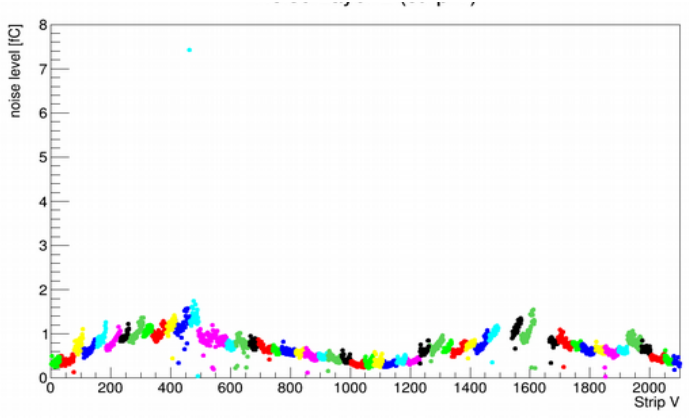


Layer 1



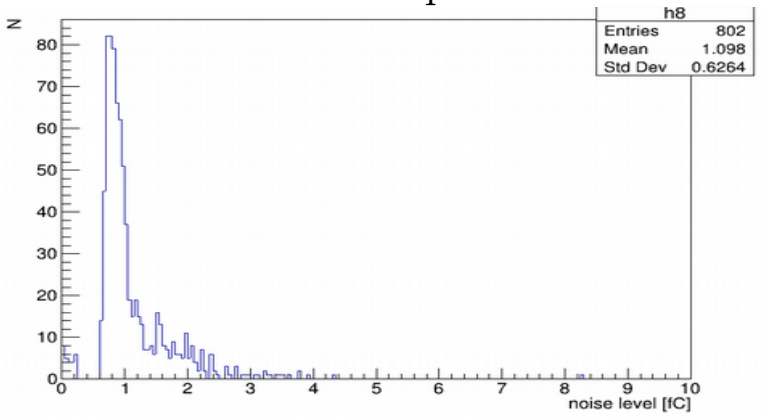


Layer 2

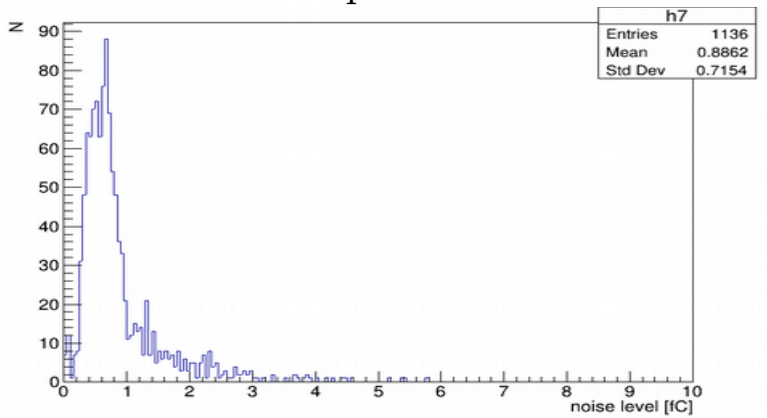


Strip-by-strip noise measurements

Strip X



Strip V



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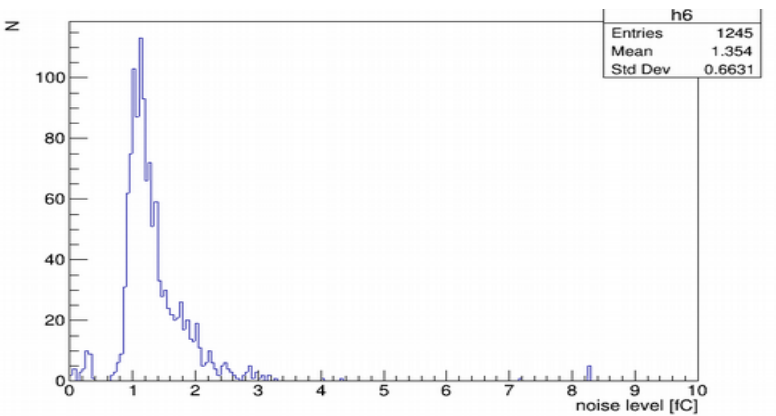
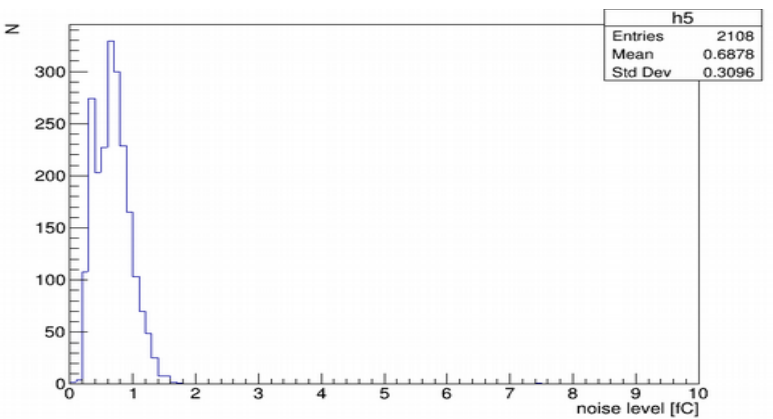


Layer 2



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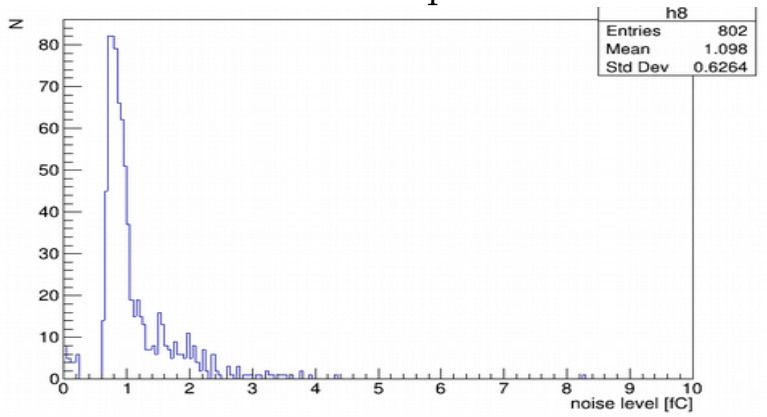
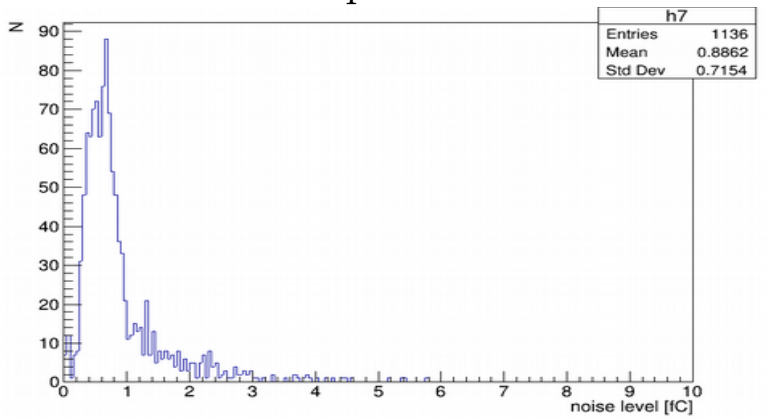
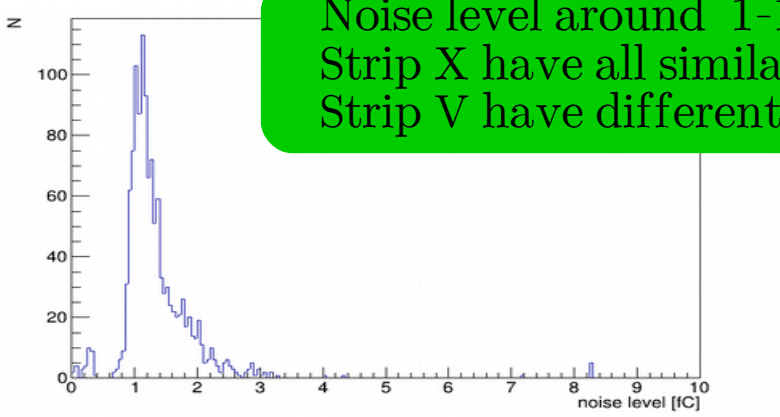


Strip V

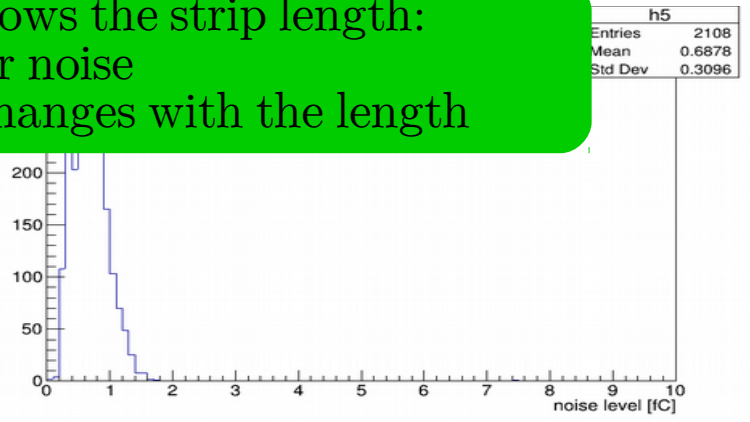


Layer 1

Noise level around 1-1.5 fC, and it follows the strip length:
Strip X have all similar length – similar noise
Strip V have different length – noise changes with the length

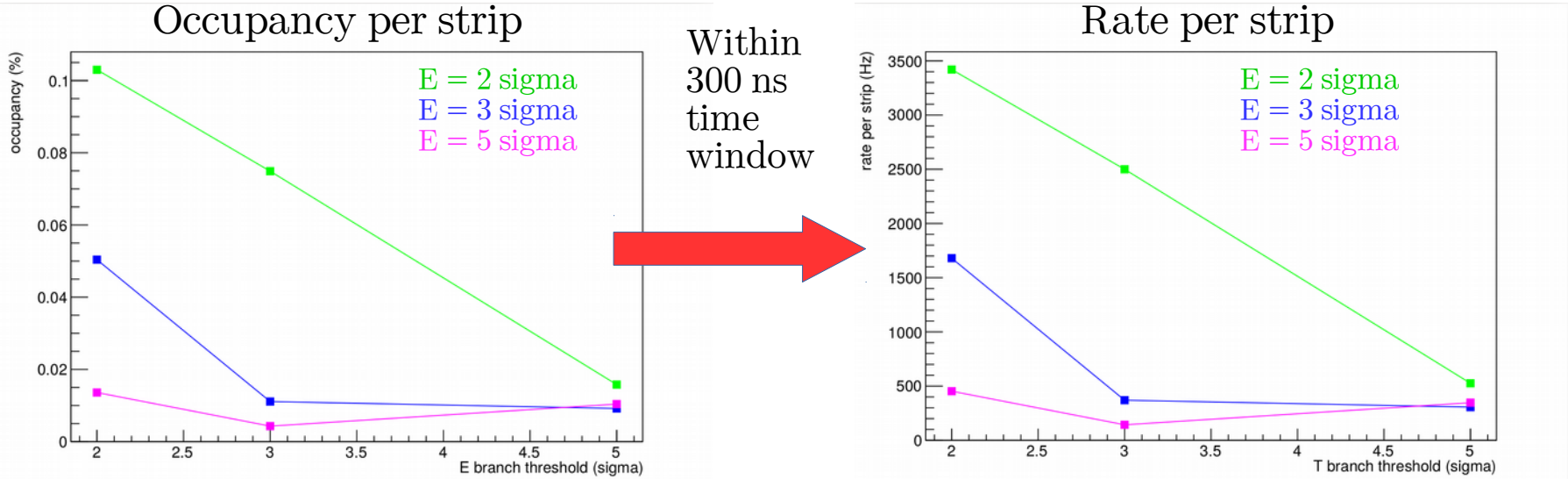


Layer 2



Noise rate with random triggers

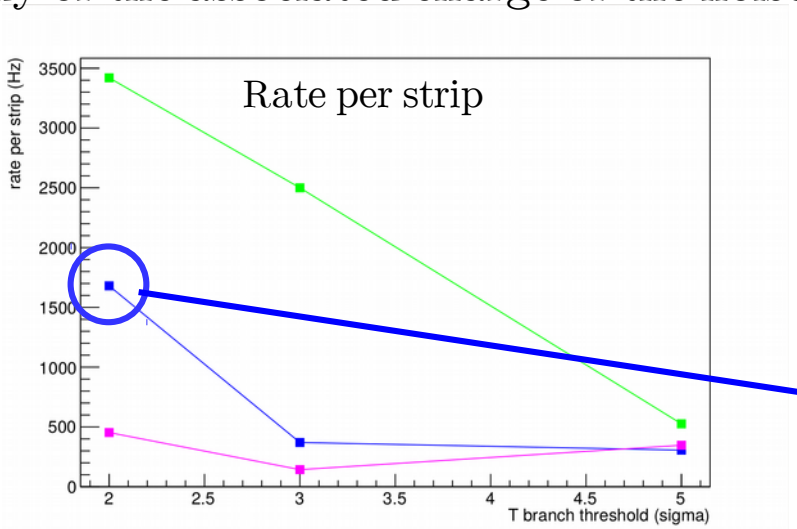
Random triggers are generated with an **external dual timer** to isolate noise distributions.
Possibility to tune each threshold individually to find the best working condition

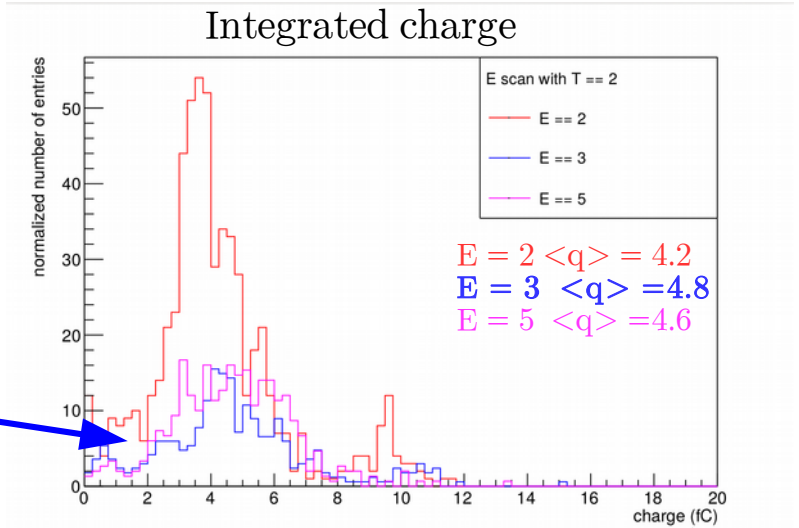


Noise rate in a chosen set of thresholds (T = 2 sigma and E =3 sigma) for one tested FEB is less than 1.7 kHz per strip.
This can be compared with the noise extracted with the all the FEBs in real data (Riccardo's slides)

Charge of the noise with random triggers

Random triggers are generated with an **external dual timer** to isolate noise distributions.
Possibility to tune each threshold individually to find the best working condition.
Study of the associated charge of the noise hits.



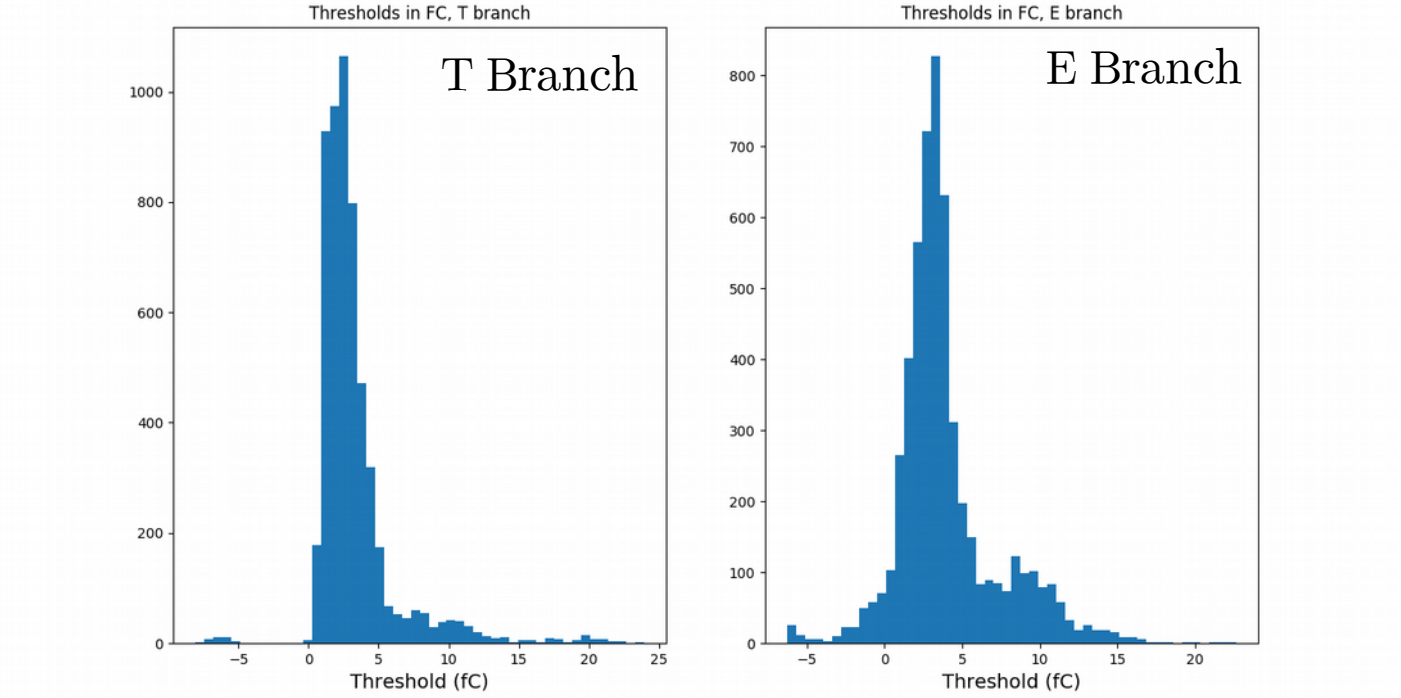


Example with T threshold at 2 sigma, E threshold at 3 sigma. 2 noise strip per event in the full layer

Optimization is still **on-going using the cosmic data taking in IHEP clean room** (more on Riccardo's slides)

Equivalent fC thresholds

It is possible to have a quantitative idea of the thresholds in fC, with some careful considerations (under-estimation if noise is v. high; if fit fails negative threshold). Each entry corresponds to one channel



Example with Threshold at 2 sigma in T Branch and 3 Sigma on E branch.
Not so far away from the milestone!

Commissioning the readout chain

We use the in-time signal to generate **digital test pulses**: analog part of the chip is **disabled**.
This information is used as the truth and we **study the performance** of the system by counting the number of times we re-collect the test pulse in the data output

Efficiency in Triggerless: the full data stream of the TIGER is readout from the GEMROC and send out.

- 100% up to 60 kHz/channel

Efficiency in TriggerMatch: check that the injected test pulse are collected

- ~95% tested at 500 Hz

Synchronization in TriggerMatch: check that the injected test pulses are collected and the time distribution is enclosed in 2 clock hits.

- ~95% tested at 500 Hz

Work in progress

Good performance, yet not perfect

- For trigger-matched, a bug has been found to be solved in the next firmware release
- 12 (out of 88) chips are affected by 8b/10b errors: cause identification in progress:
  - 2 chips do not send digital TP and they will be replaced
  - 2 FEBs (4 chips) do not receive proper RESET signal $\rightarrow$ replace the long haul cables
- Solutions for 8b/10b errors have been already proposed: reduction of long haul cable length and/or implementation of active signal/clock repeaters

Test in BESIII experimental hall

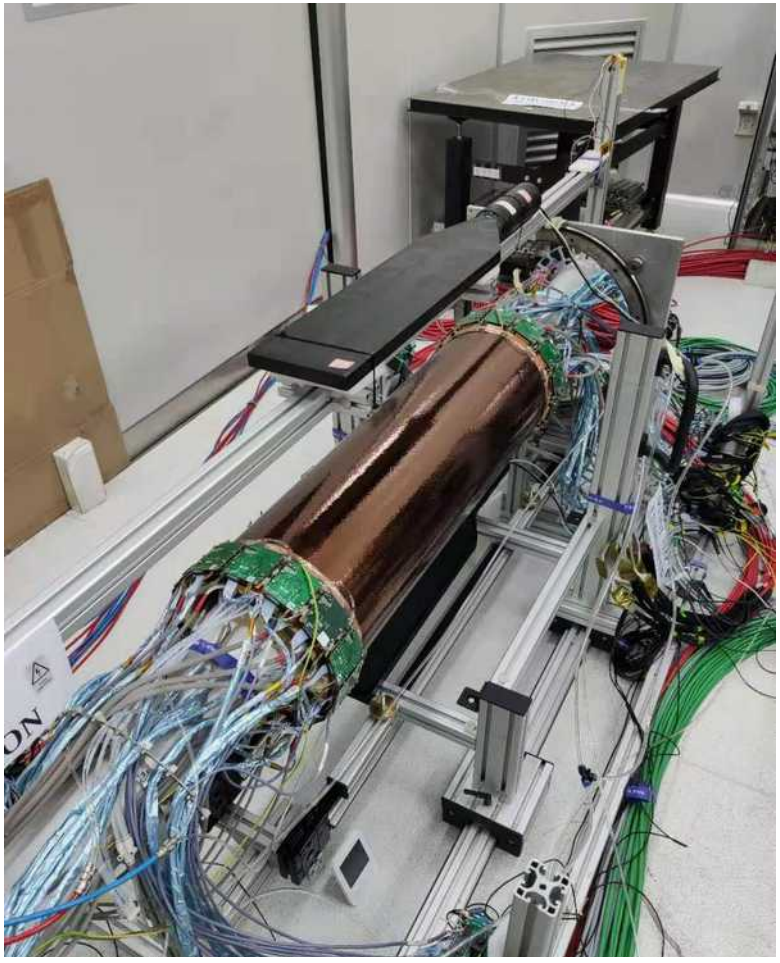
In February joint EB-TB meeting, the RF shielding issue was raised.

- To verify, bring one layer inside experimental hall to test effect of the accelerator RF on the electronics noise.
- In September, before the synchrotron radiation run of BEPCII, the present L1 instrumented with 4 FEBs, 1 GEMROC and 1 DAQ computer will be brought inside the experimental hall. **No cooling and no HV for space and service availability constraints**
- Placement on the layer inside the experimental area will be confirmed at the beginning of the BEPCII Summer Shutdown (in 1 week).
  Possible spot: BESIII hall west entrance, nearby the interaction point
- Condition of shielding will be much worse compared to the one in operation. To test the **effect on the noise**, a full **characterization** (noise scan, noise rate, noise charge) will be performed **before and during the accelerator operation**

(almost) Final words

Close to the milestone to operate with 3-4 fC thresholds

- Optimization goes through:
  - Investigation on the source of 8b/10b errors
  - Improvement of general noise situation
  - Newer firmware release to improve efficiency of Trigger Match data
- Additional tasks: test in BESIII experimental hall
- More exciting results in the data analysis talk (by Riccardo)!



Thanks for your attention!