AGATA PROJECT

Preprocessing Electronics Status

N. Karkour

Outline

- Carrier Cards Production Status
- Mezzanine Cards Production Status
- Mezzanine GUI Slow Control Status
- Pre Processing Test Bench Facility @ Orsay
- Mezzanine Local Slow Control Status
- Mezzanine Cards VHDL Status

Carrier Cards Production status

- **12/2008** : Production started with the Emelec company
- **02/2009 (1st week) :** 3 pre-production cards were received
  - Emelec signaled design footprint problem with the DC DC components « LTM4600 » prior to go to full production.
  - Discussion about taking risk and going to production or modify the pcb footprints.
  - Decision to go to production with existant pcb was made.

Carrier Cards Production status

- **03/2009 :**
  - Repair of 3 pre production cards
  - Production of 30 cards started
  - Assembly Bench @ IPN SEP to modify the received pcbs (adding wire modifications cutting tracks and adding components.
  - Production of ATP (Acceptance Test Procedure), and ATR (Acceptance Test Reports) for :
    - To the Emelec Company partial Power Supply Test
    - To IPN Full Power Supply Test (PIC programming)
    - JTAG Test (re writing of the Boundary Scan program)
    - Power PC Test (Test program from Padua)

Carrier Cards Production status

- **Summary of 2009 cards status :**
  - 33 CARRIER cards were produced.
  - 18 cards are in Legnaro.
  - 3 CARRIER cards are @ CSNSM working with the Orsay Test Bench.
  - 2 cards tested @ CSNSM and OK they are @ IPN
  - 1 card tested at IPN, to test at CSNSM Test Bench
  - 3 cards to send to Emelec for repairs (2 cards : Zarlink Problem, 1 card: Power Supply Problem)
  - 6 cards at Emelec for repairs. (2 cards will arrive at IPN on 14/01/2010 and another 2 cards in next week).

Summary of the Carrier Card Production

- Out of the the 33 delivered cards :
  - 12 cards were produced and tested OK without any problem @ Emelec (36%)
  - 7 cards went only once back to Emelec (21%)
  - 4 cards went back twice to Emelec = 1 carte (3%)
  - The rest of the cards (10 cards) went at least 3 times or more to Emelec and are not delivered yet (33%)
- The risk to go to production without pcb modification costs at least 7 months of delay (still 9 cards to be delivered) but it was important to get at least the 12 cards to start experiments

Local Level Processing Mezzanines

D. LINGET & N. KARKOUR

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Local Level Processing Mezzanines

- Manpower : development & integration

Hardware
Firmware
Software

CSNSM actors :

Electronic team
- Karkour Nabil
- Lafay Xavier
- Leboutellier Stephane
- Linget Denis
- Perrier Simon
- Pierre Eric-Gibelin Laurent
- Travers Bruno

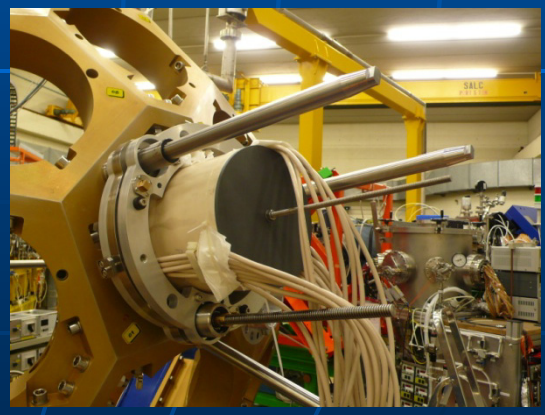
Computer team
- Dosme Nicolas
- Legay Eric
- Grave Simon

AGATA collaborators :
- Bazzacco Dino (INFN)
- Bortolato Damiano (INFN)
- Chavas Joel (INFN)
- Coleman-Smith Patrick (STFC)
- Grave Xavier (IPNO)
- Lazarus Ian (STFC)
- Oziol Christophe (IPNO)

Local Level Processing Mezzanines

• Reminder Segment board status

- **begining 2009** : Legnaro tests
  - ➢ Carrier power supply test for Mezzanines ➔ OK.
  - ➢ Stand alone Ethernet test in AGATA area ➔ OK
  - ➢ Ethernet test through Carrier ➔ OK (Jan 2009).
  - ➢ Integration of High speed link automatic tests (Digitizers ←→Mezzanines) ➔ OK (Jan 2009).
  - ➢ Server for exchange files (firmware, software) Orsay←→ Italy ➔ OK (Jan 2009).
  - ➢ Preliminary Slow control via I2C (per channel setup) in collaboration with Damaino (before Orsay version) ➔ OK (Jan 2009).
  - ➢ Burning tests : T° variations on 4 points with functionality control on data transfert from Digitizer ➔ OK (Jan 2009).



End of qualification phase

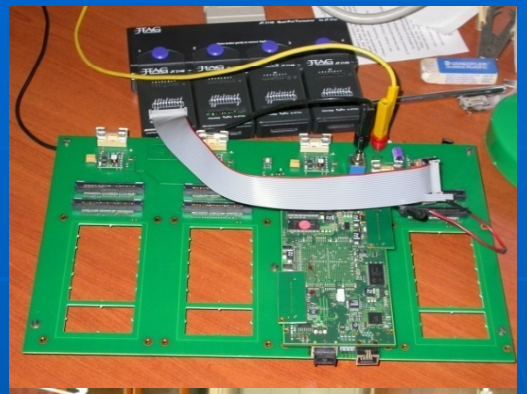
GREEN LIGHT for Mezzanines Demonstrator production

Local Level Processing Mezzanines

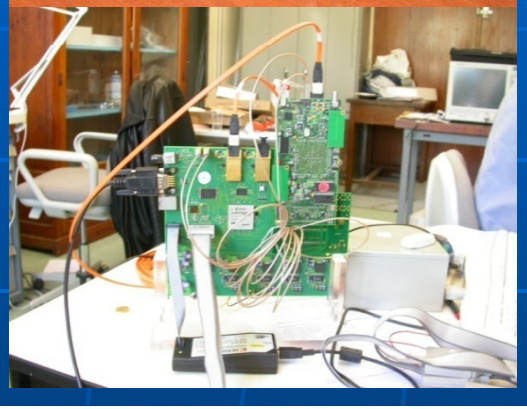
• Segment board status

- Winter 2008-2009 : Assembly company selection
- Manufacturing procedure included the following phases:
- Components Assembly
- Xray test (BGA packages)
- Power supply tests.
- JTAG Boundary Scan tests (CPLD & FPGA and memories)
- CPLD and FPGA Programming
- functional tests (with Orsay Test Mezz)
- Coverage test is around 88%
- Since the functional test is OK no card returned for failure.

JTAG Setup



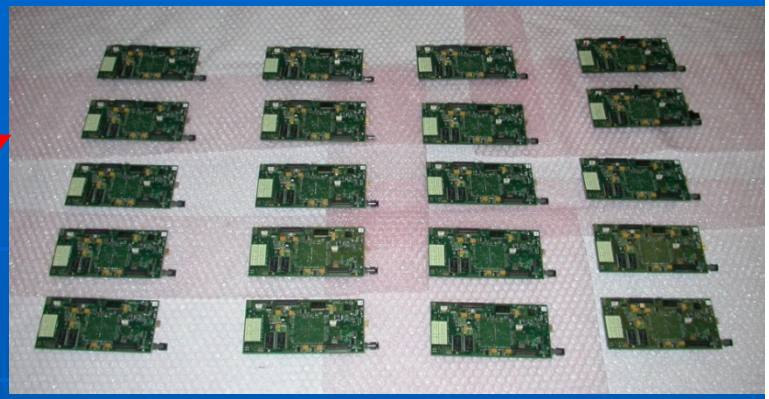
Orsay Test Mezz



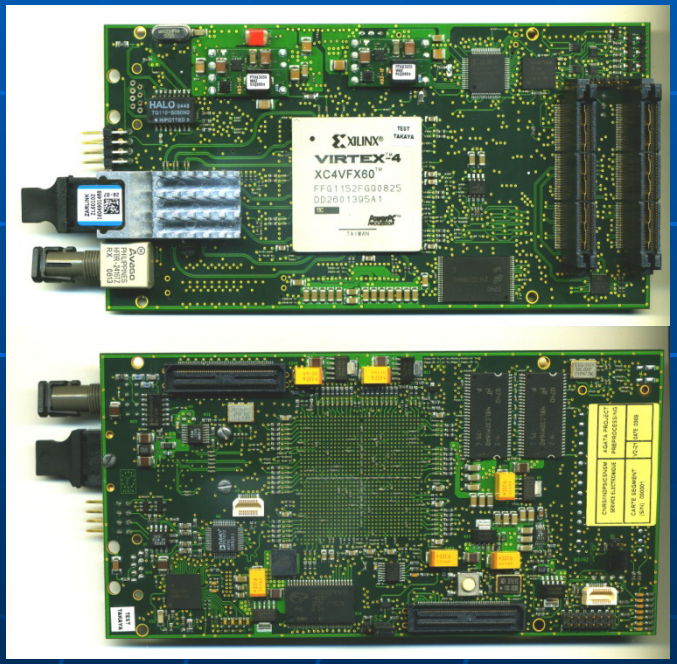
Brest

Local Level Processing Mezzanines

- Segment board status



- 2009 (continued):
  - Preproduction delivery ➔ End March 2009.
  - Validation tests on 20 preproduction cards ➔ OK (end Apr 2009).
  - Assembly production start on 90 cards with delivery schedule on several batchs ➔ May 2009.
  - delivery batchs to Legnaro ➔ from May to Sept 2009 (3 TCs).



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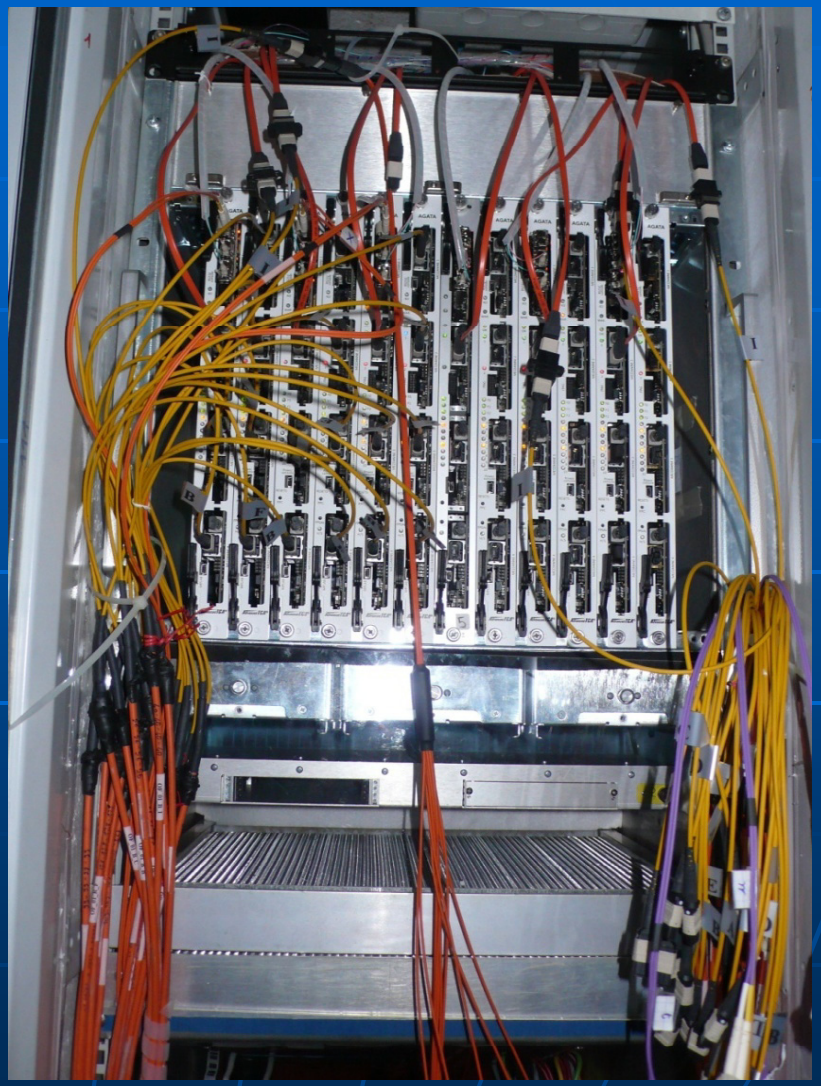
Local Level Processing Mezzanines

- Segment board status

2009 (week 51):

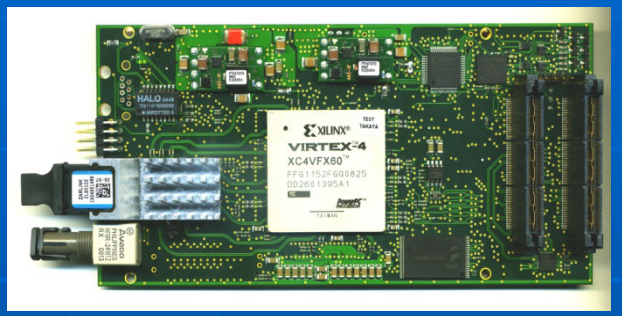
Crate 1 with Carriers for 2 TCs

18 IPNO Carrier Front panels mounted by Bruno Travers (Thank you Bruno for this sensitive process)



Local Level Processing Mezzanines

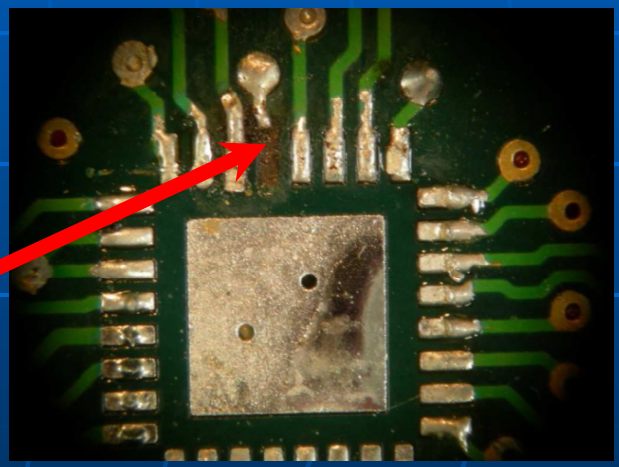
- Segment board status



- Today:
  - **110 Segment cards V2.21** manufactured:
    - 71 OK : Legnaro.
    - 36 OK : Orsay
    - 3 Not OK :

      - 2 with FPGA failures (to be investigated with JTAG probe facilities).

      -1 with clock driver failure (PCB track destroyed).



  - 10 extra Prototype Segment cards V2.2 delivered : used in Orsay for AGATA Testbench and/or for development.

Local Level Processing Mezzanines

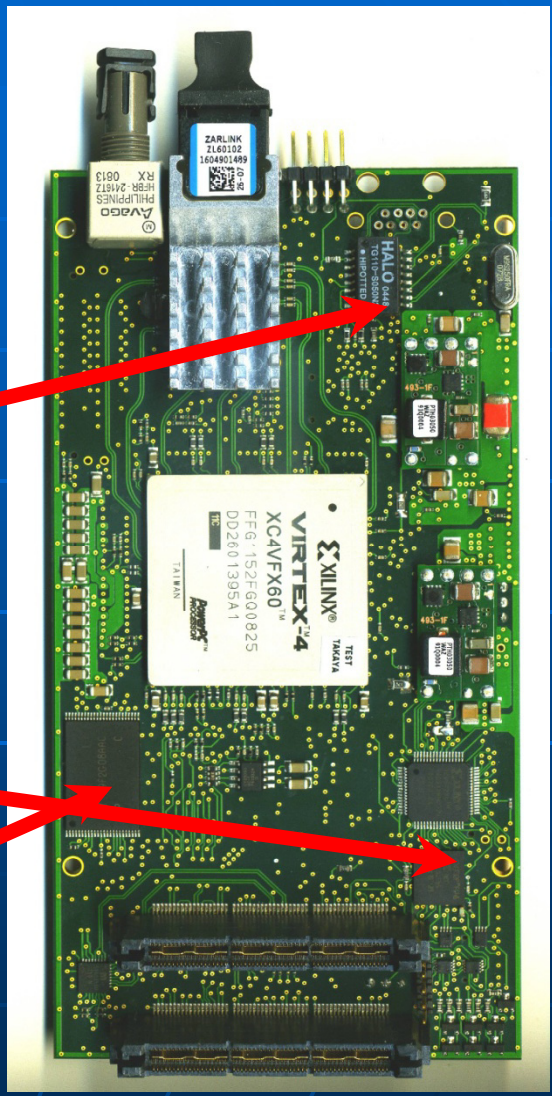
- Comments about production:

➢ After this production experience: excellent results (80 % first time functional test OK). Only 3 cards have serious problems. quick reactivity when failure occured) ➔ time reduced for us to finalise validation tests. reduced for CSNSM engineer Manpower

➢Small cracks on plastique Ethernet Transformer ➔ safety action : manually replacement with new component.

➢Xilinx memory failures on JTAG tests: due to BGA package and no default detected on Xray pictures, we take the decision to replace the component.

➢Flash memory Failures on around 15 cards replacement with new components from a new batch (bad manufacturing batch).



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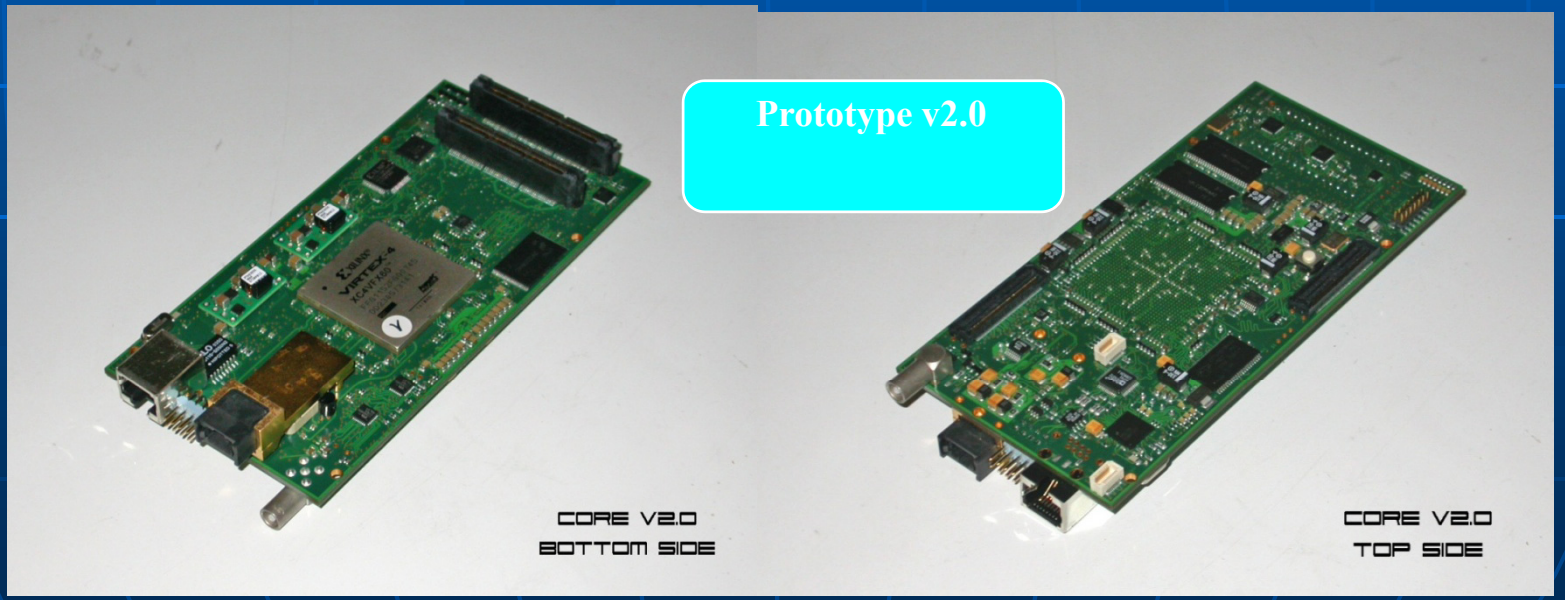
Local Level Processing Mezzanines

• Core boards

- No more development due to Segment production priority.
- Dino Bazzacco is OK to continue validation tests on this part (NOV 2009) ➔ Integration of the actual segment firmware is integrated.
- Tests stopped because the GTS does not send the defined Sync signal directly from GTS to the core card (diff. PECL). Waiting for GTS source files to move sync pin to the mictor.



Local Level Processing Mezzanines

- 2010 Schedule

➢Core card : validation tests and production for 5 TCs ➔ need to do a realistic schedule.

Mezzanine GUI Slow Control UPGRADE

S. Perrier & N. KARKOUR

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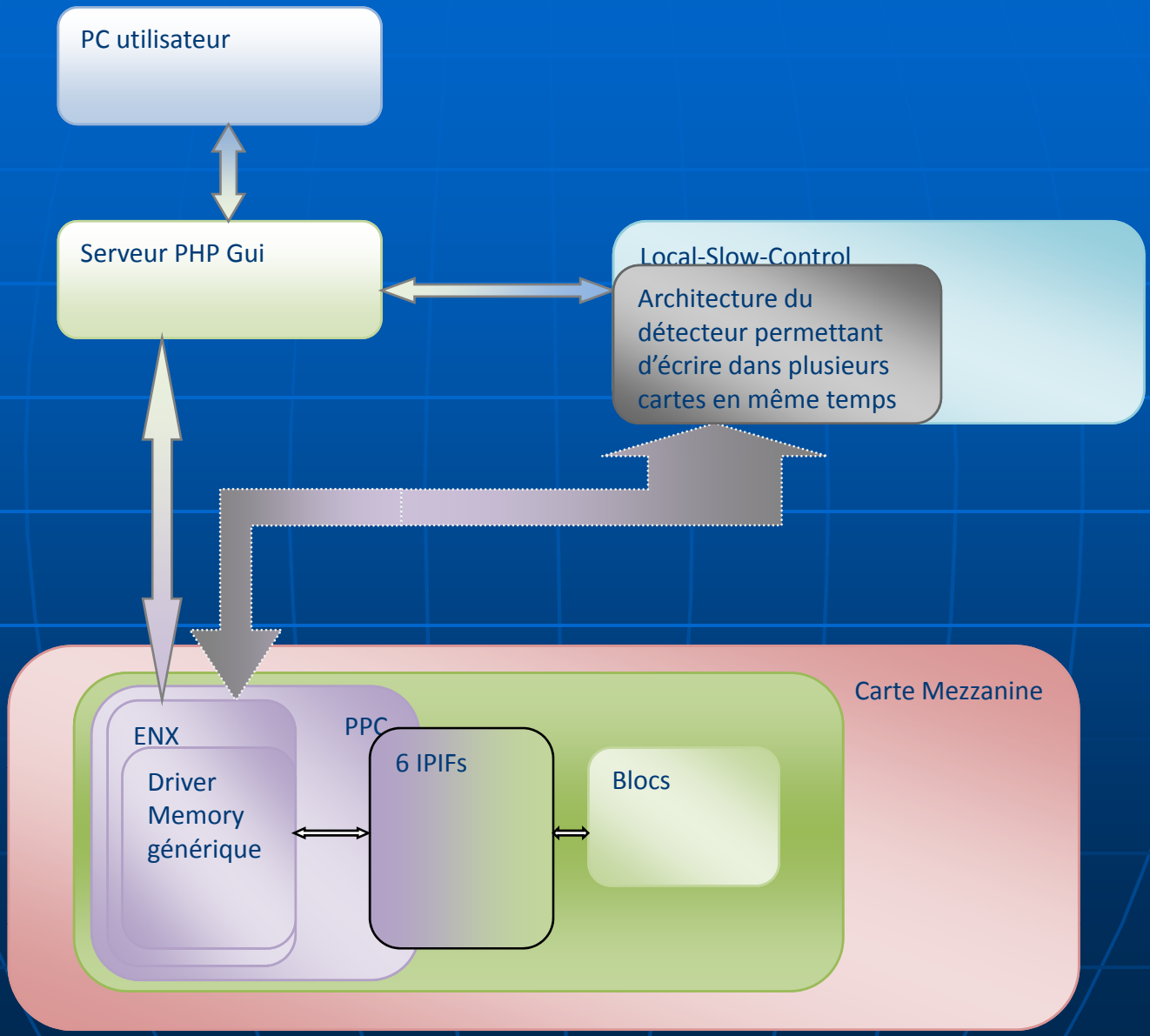
Mezzanine GUI Slow Control UPGRADE

- Preliminary GUI Mezzanine was developped for segment by segment control.
- Good to start and qualify VHDL code, PPC drivers, Linux integration drivers, and soap command interface.
- Very limited to setup a mezzanine card, and veryvery limited (impossible) for setup of 1 crystal.
- It was designed for expert use, mezzanine maintenance, qualification in integration area of Legnaro.

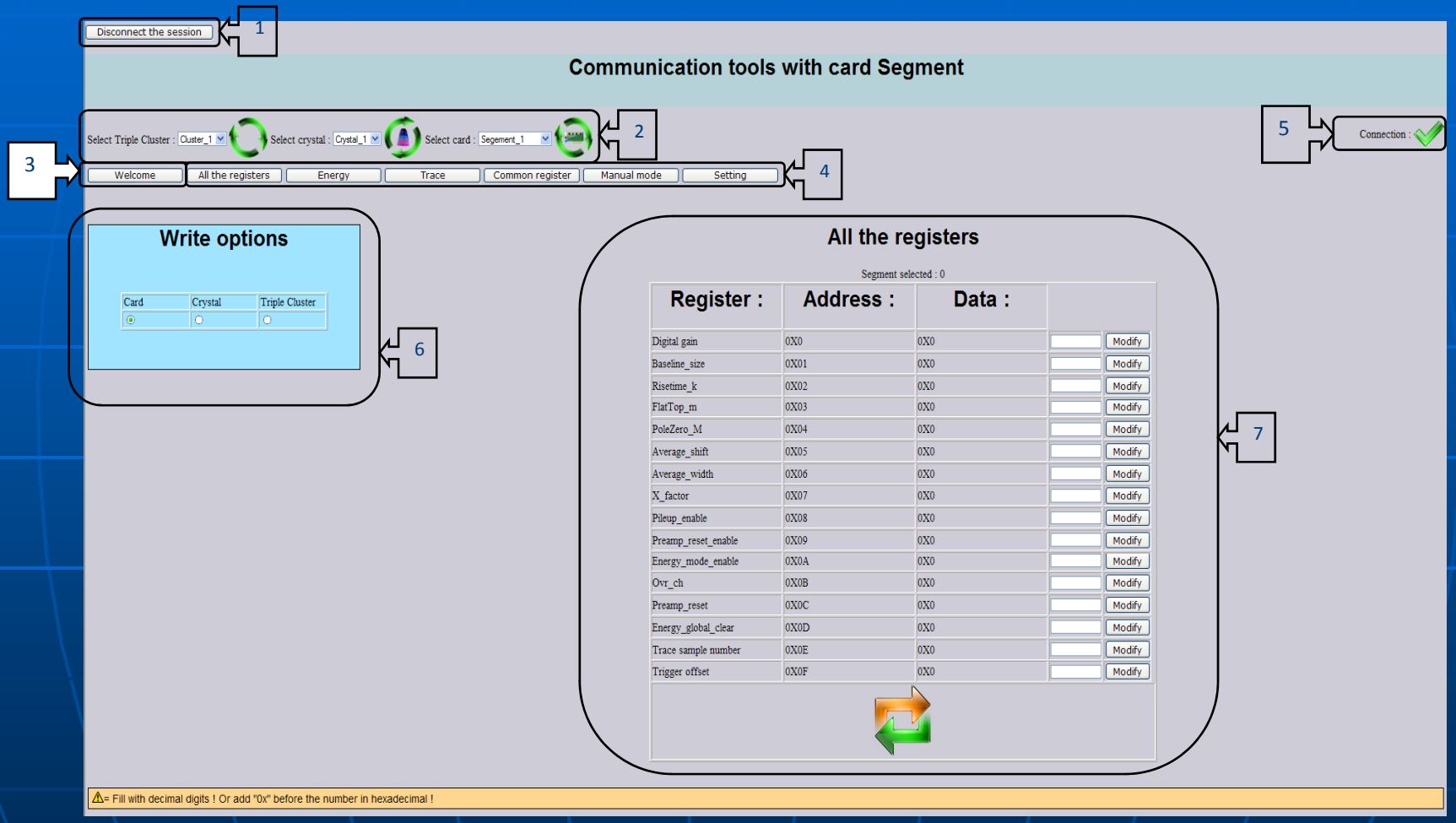
Mezzanine GUI Slow Control UPGRADE

- New GUI was rapidly needed to setup 1 mezzanine card simultaneousely, and use of the LSC mezzanine to setup 1 crystal or 1 TC or all detectors with 1 command.
- New design and new architecture was designed,
- New windows and new interfaces were developped.
- GUI is finished and virtual tests were qualified.
- Since LSC is working now the new GUI is to be qualified in Jan 2010.

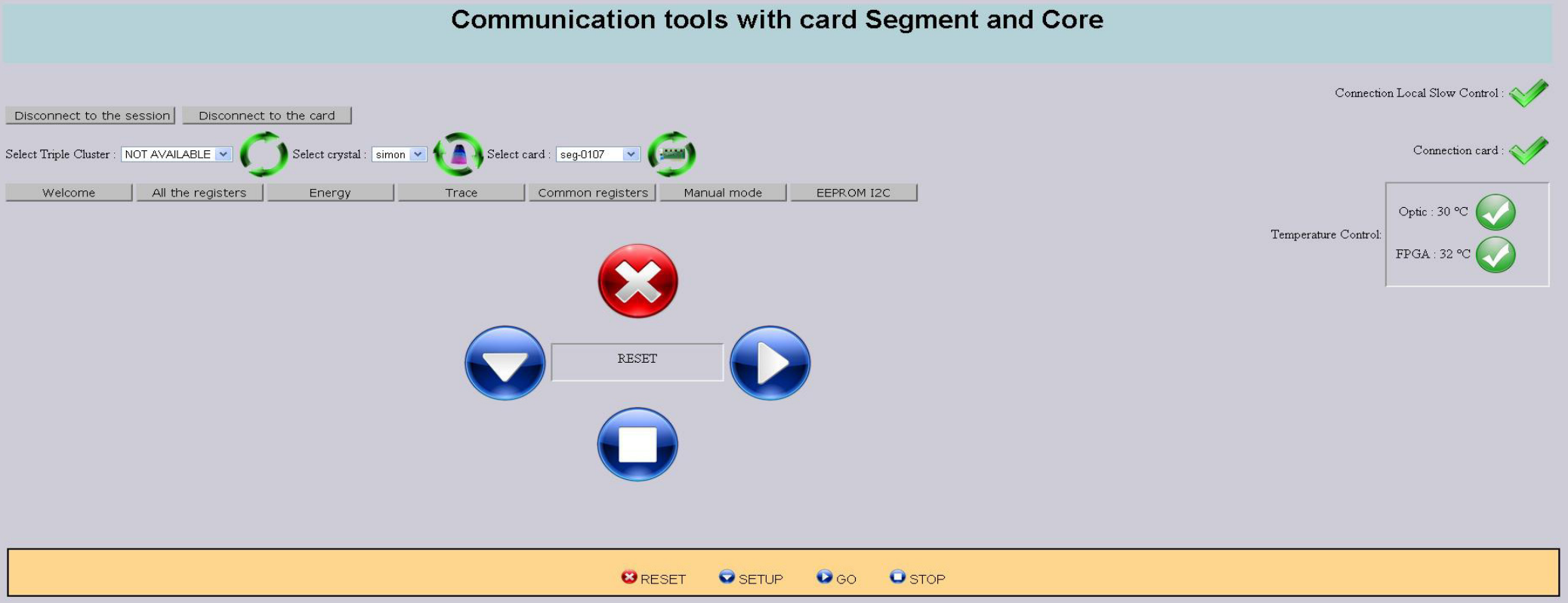
Mezzanine New GUI



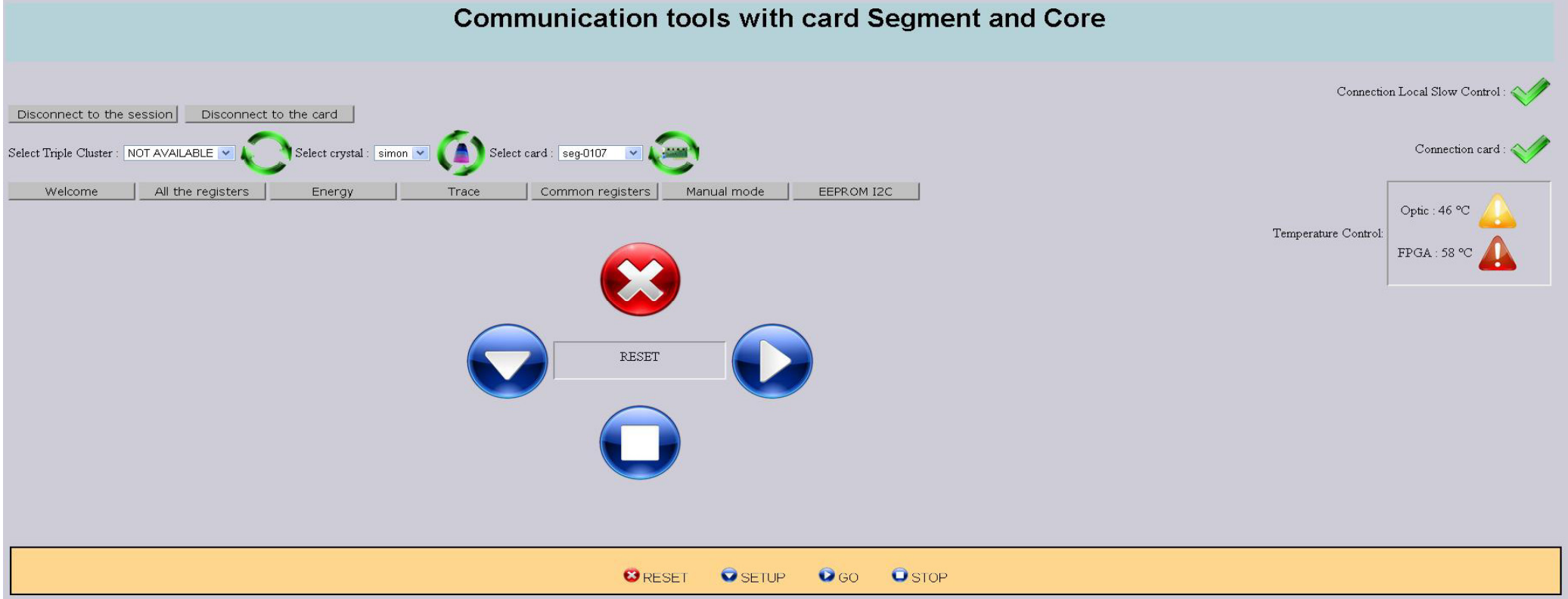
Mezzanine New GUI



Mezzanine New GUI



Mezzanine New GUI



Mezzanine New GUI

- Allows user to connect and disconnect easily (logout user before).
- Allows to switch easily from one card to the other by simple menu select.
- Allows user to connect to the GSC.
- Access to the old GUI menu is possible.
- Verifies the good connection to the card.
- Allows user to choose the card to write to.

Pre Processing Test Bench Facility

N. KARKOUR

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Pre Processing Test Bench Facility

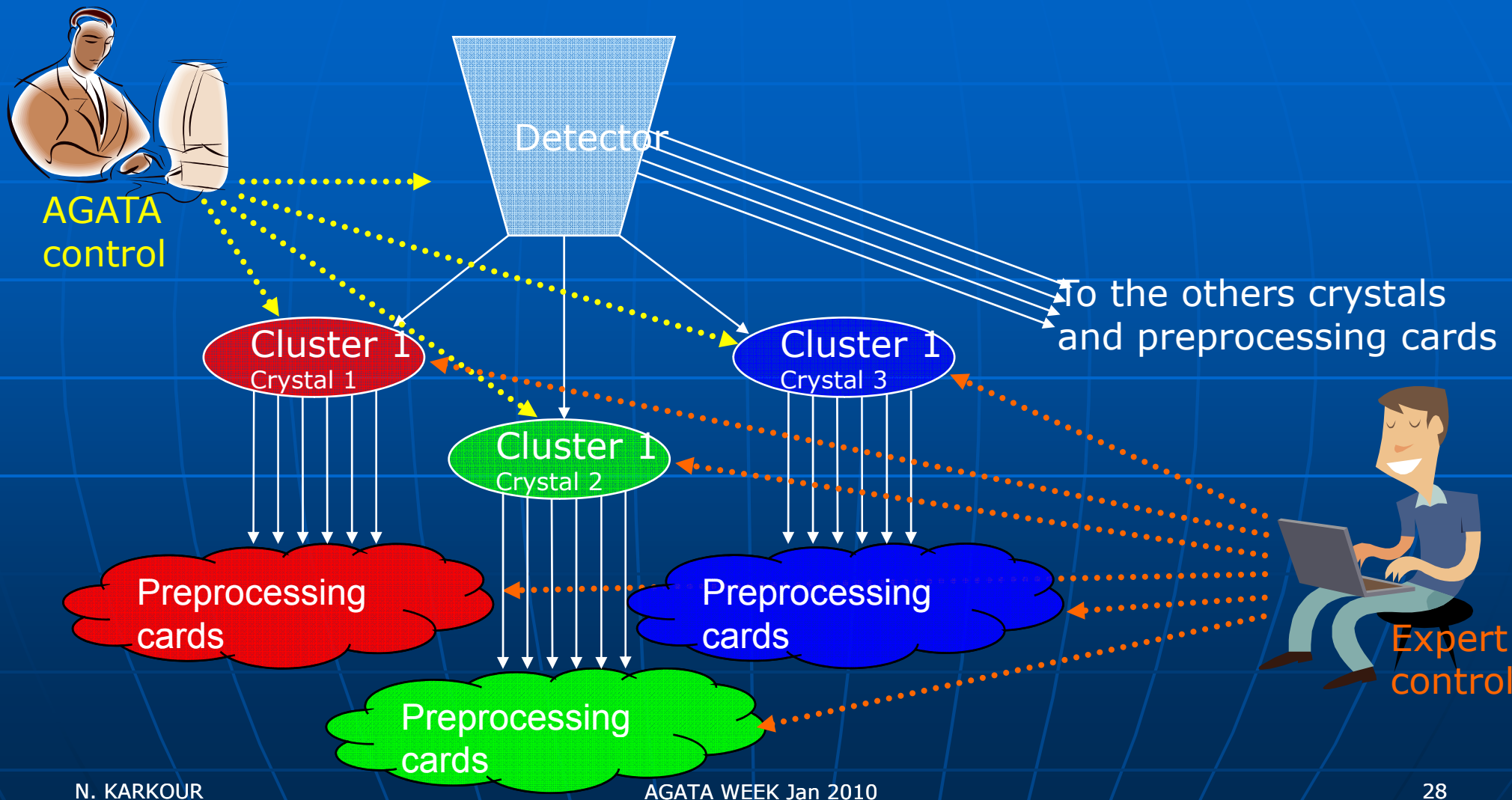
- Due to Project priorities the Orsay Test bench material started delivery Q4 2009.
- GTS board received in September 2009.
- 2 months of GTS tests and maintenance from CSNSM engineer to persuade the collaboration that the GTS is defected (toooo long to insist on the reality of the defect inside the GTS)
- Need an optical splitter to make acquisition
- Need routing the sync signal on to the mictor connector
- Digitiser was received Nov. 2009. All software installed and tested in December 2009. Delay due to lack of Manpower
- Optical interface is needed between the carrier card and the pizza box to complete DAQ.
- New 2 slots ATCA crate is ordered because the actual 24 Slot is too big to house inside the AP1 bay.

Mezzanines Slow Control

Nicolas Dosme

CSNSM

Design for Segment Slow Control



ENX Architecture

AGATA control

Linux server
(slowcontrol.agata.daq)

ENX core

Crystal device

Crystal device

Crystal device

Detector device

Mezzanine device

Mezzanine device

Mezzanine device

Embedded Linux
Mezzanine segment 1
ENX core
Low Level device

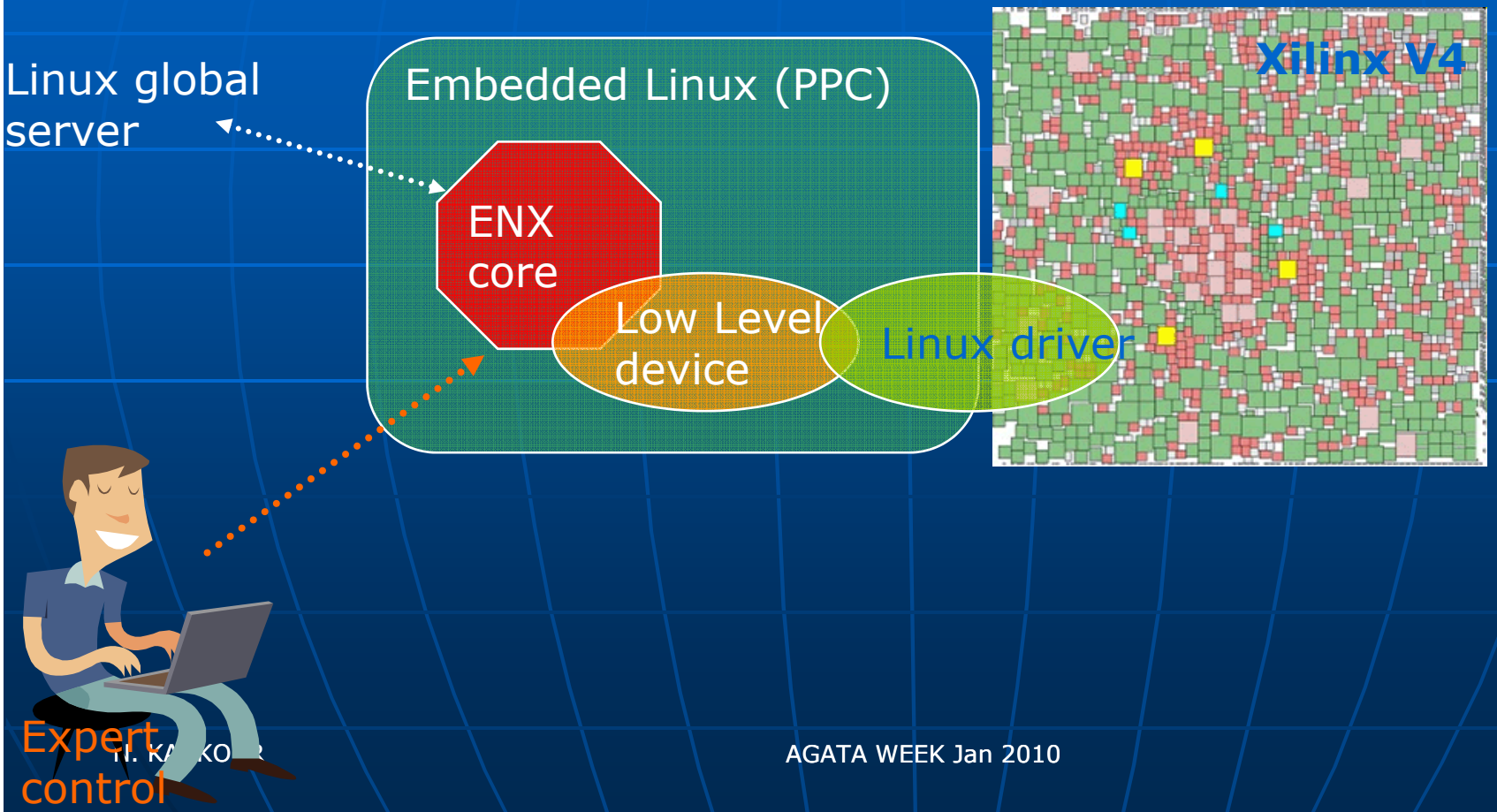
Embedded Linux
Mezzanine segment 1
ENX core
Low Level device

Embedded Linux
Mezzanine segment 1
ENX core
Low Level device

Expert control

To others
Segment cards

ENX sur une Mezzanine



Embedded Linux

- Basic Linux is inside the mezzanine Flash memory
- @ system boot 2 script startup files are executed :
  - Update system (Librairies, …)
  - Update software
    - ENX, Drivers ENX
    - ENX Scripts (loading, «setup»)
- Updating Linux inside flash memory by simple command automatic code put inside the scrip files while booting

Interfaces

- Standard Interface
  - Web Services identical to the Digitisers (DoReset / DoSetup / DoGo / …)
  - Ready to be integrated inside the GSC
- Expert Interface «expert»
  - Direct Access to Mezzanines registers

Configuration and topology

- Topology Text File:
  - Détecteur ⇔ Cristal ⇔ Mezzanines
    - Possibility to define virtual mezzanine
- Psuedo Static Configuration
  - ENX Script file for each action (Setup, …)
    - Loaded @ system startup

Integration @ Legnaro 12/2009

- Installation succeeded
- Test succeeded

- Slow Linux Boot for certain cards if the mezzanine number exceeds 25 cards
  - ⇒DHCP Problem HW SW?
  - ⇒Solutions To be tested:
    - ⇒ Linux upgrade
    - ⇒ ATCA Chief manager control

Current or Future Problems to solve

- Compilateur
  - Licence Ada Core ...
  - upgrade machine SlowControl
- Topology
  - consistancy Problem => DB needs to be updated
  - Lack of exchanged information between electronic modules
- Configuration
  - No global Save / Restore for the moment its text file

Mezzanines VHDL CODE STATUS

N. KARKOUR

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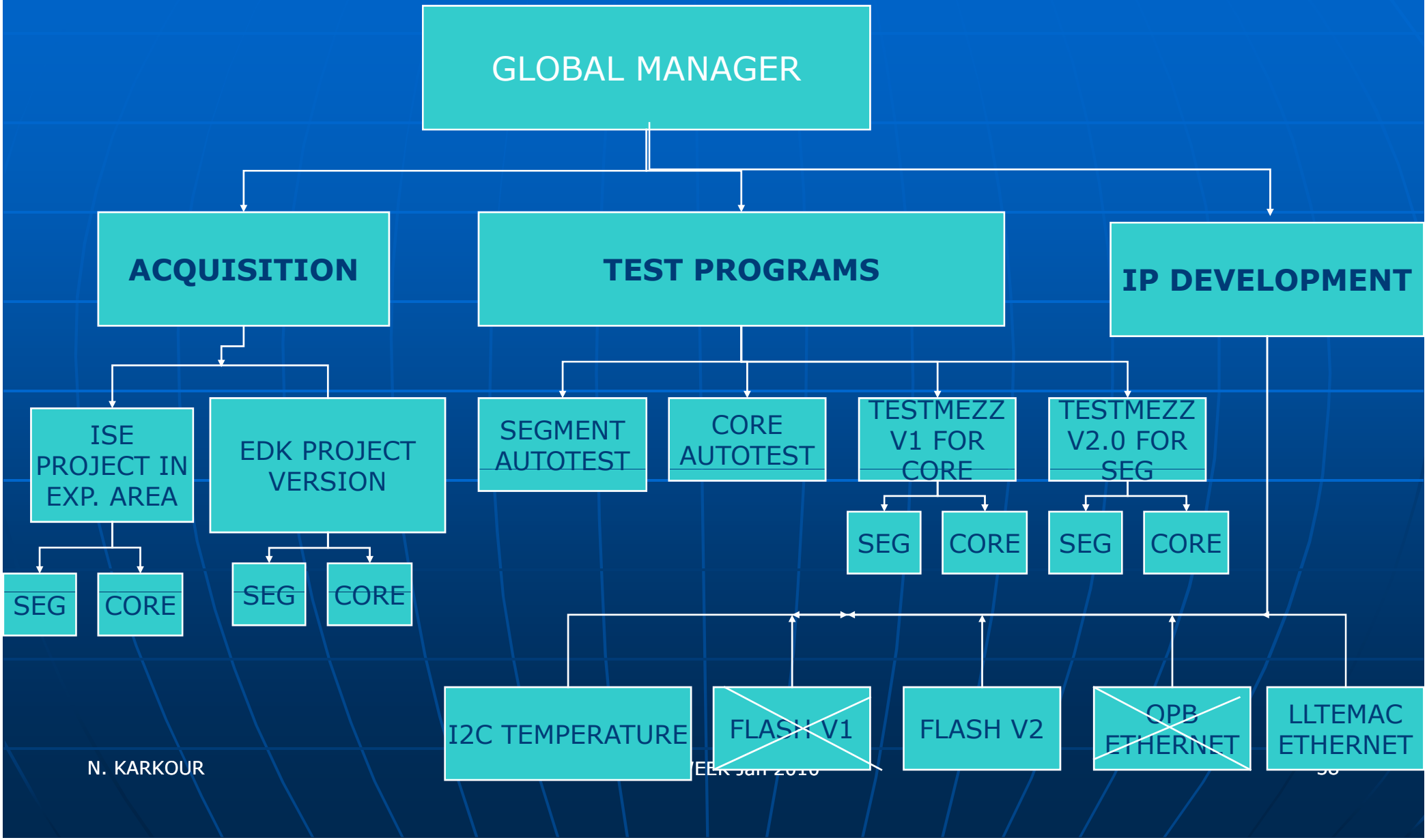
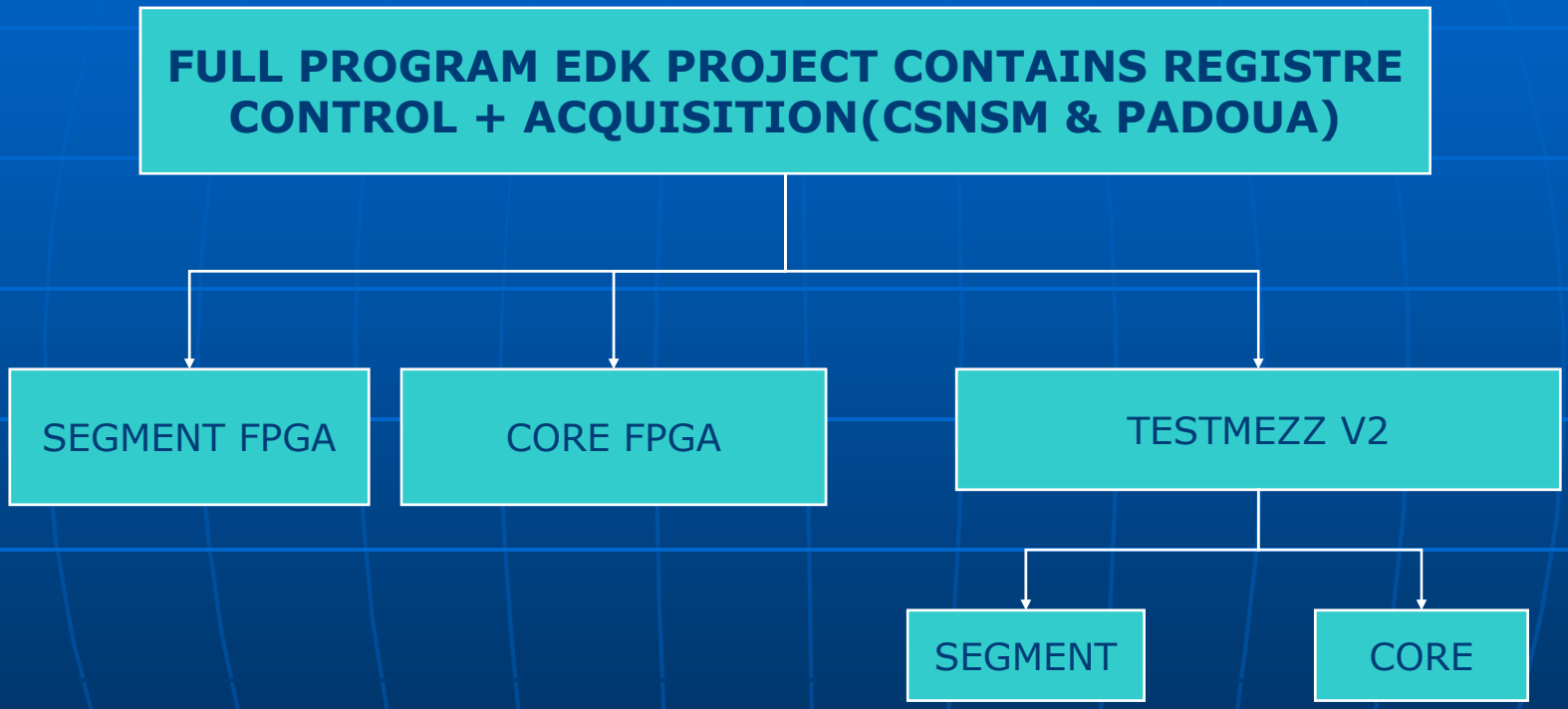
List of work on Hardware and VHDL since last AGATA week

- Qualification of all VHDL IPs developped to control all the mezzanine interfaces
- Replacement of the I2C Slow Control through the Carrier card (only DCM and HSSD left)
- Developpement of the Long Trace Algorithm to calibrate the TC segments
- Developpment of the I2C Database E2PROM (Card Identity data)
- Developpement of the Temperature sensors to send alarms TO GSC through LSC
- Developpement of the monitoring and counting rates IP.
- Developpement of a 32K depth 256 channel logic analyser.
- FPGA capacity reached full design and Several designs were made to reduce space.
- 1 month to solve the above problem.
- New problem is FPGA compilation time became long (1 hour approx.)
- Full qualification after each modification to insure system stability.
- NEW Firmware was installed successfully in Legnaro in week 14-18 of Dec. 2009

OLD Management of the VHDL



Management of the Actual VHDL



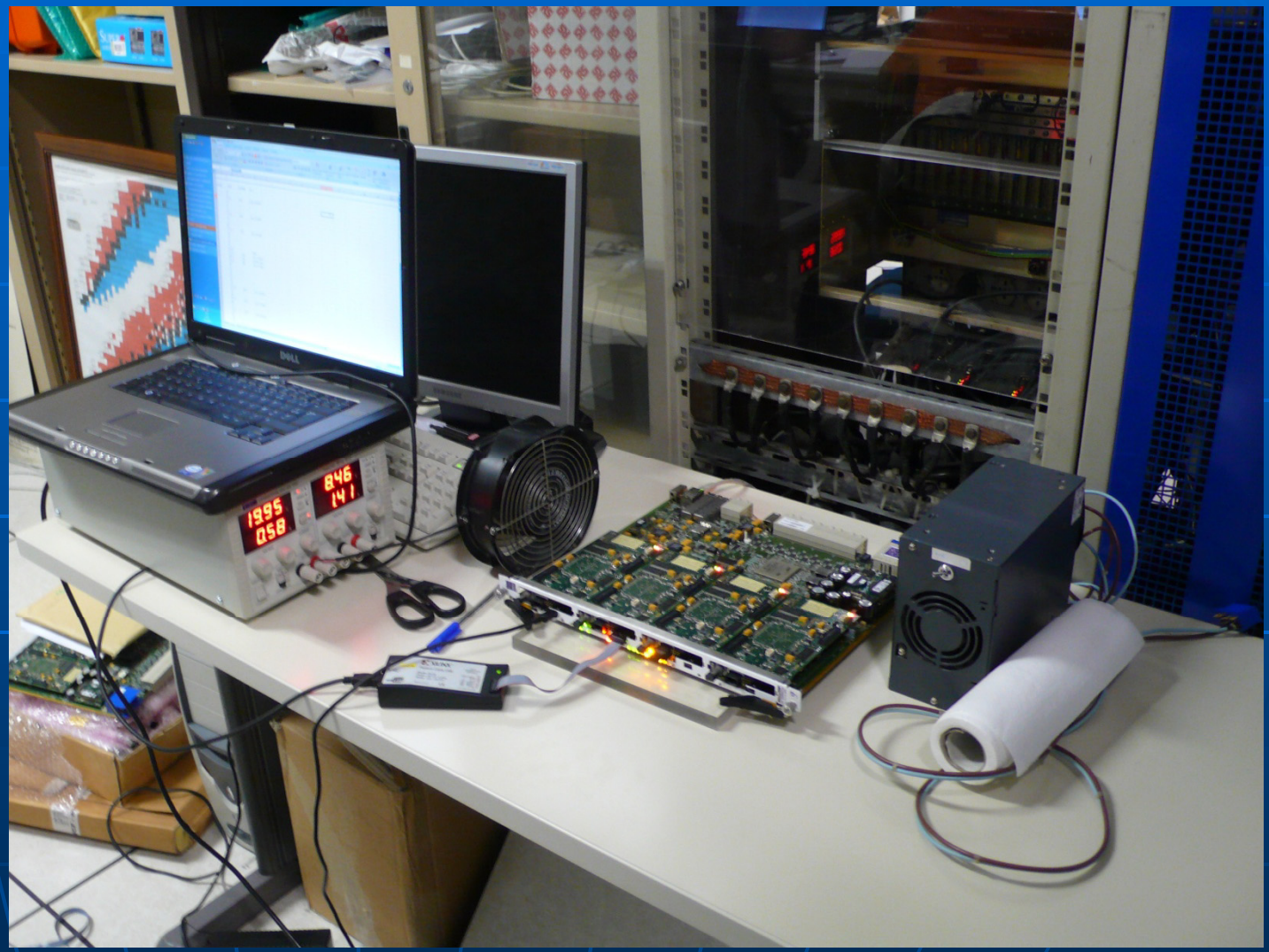
Report 14-18 Dec 2009 visit

- Goal of the visit is to install the full VHDL code (PPC + Acq)
- Lot of preparation were made to make this visit successful.
- 80 cards to be upgraded in place.
- System MUST stay as it is after the modification.
- Heavy qualification at Orsay to make sure the upgrade is feasible.
- Detailed timing Flow chart to optimise working tasks.
- To upgrade a mezzanine (take off carrier card and take off solder drop on each mezz).
- Program CPLD and put on solder drop
- Program FPGA E2PROM mcs file.
- Test card to check network connection and check acquisition and system stability.

Report 14-18 Dec 2009 visit

2009 (week51):

Stand alone setup for Linux Flash upgrade



CSNSM

Report 14-18 Dec 2009 visit

2009 (week 51): Most of CSNSM Team @ work

Results of the 14-18 Dec 2009 visit

- First day visit was to check network linux program installation with working carrier from Orsay plus starting CPLD programming (Day 1 successful)
- Day 2 was dedicated to continue CPLD and to start FPGA updates. (problems started)
- Discovery of the VHDL code modification between September and December 2009 @ Legnaro (to improve system checking) without any updates on SVN server to add the changes in Orsay.
- Moreover the changes were not documented and the Orsay team had to verify file by file all the differences.
- Day 2 Late at night upgraded VHDL code was tested on the full code from Orsay.

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Core card VHDLStatus

- Deadline to reply to electronics preprocessing team (somewhere Q3 or Q4 2009?)
- Started in Jan 2010 (FIRMWARE CODE INTEGRATED 2 DAYS AND ALL CARD INTERFACE IS TESTED)
- STOPPED BECAUSE OF THE GTS CODE TO BE MODIFIED(MOVE SYNC PECL SIGNAL TO MICTOR AS AGATA SPECIFICATION TDR)

Conclusion

- Thanks to all those who helped the Orsay team to reach their Goal
- Special Thanks to the Orsay Team.