

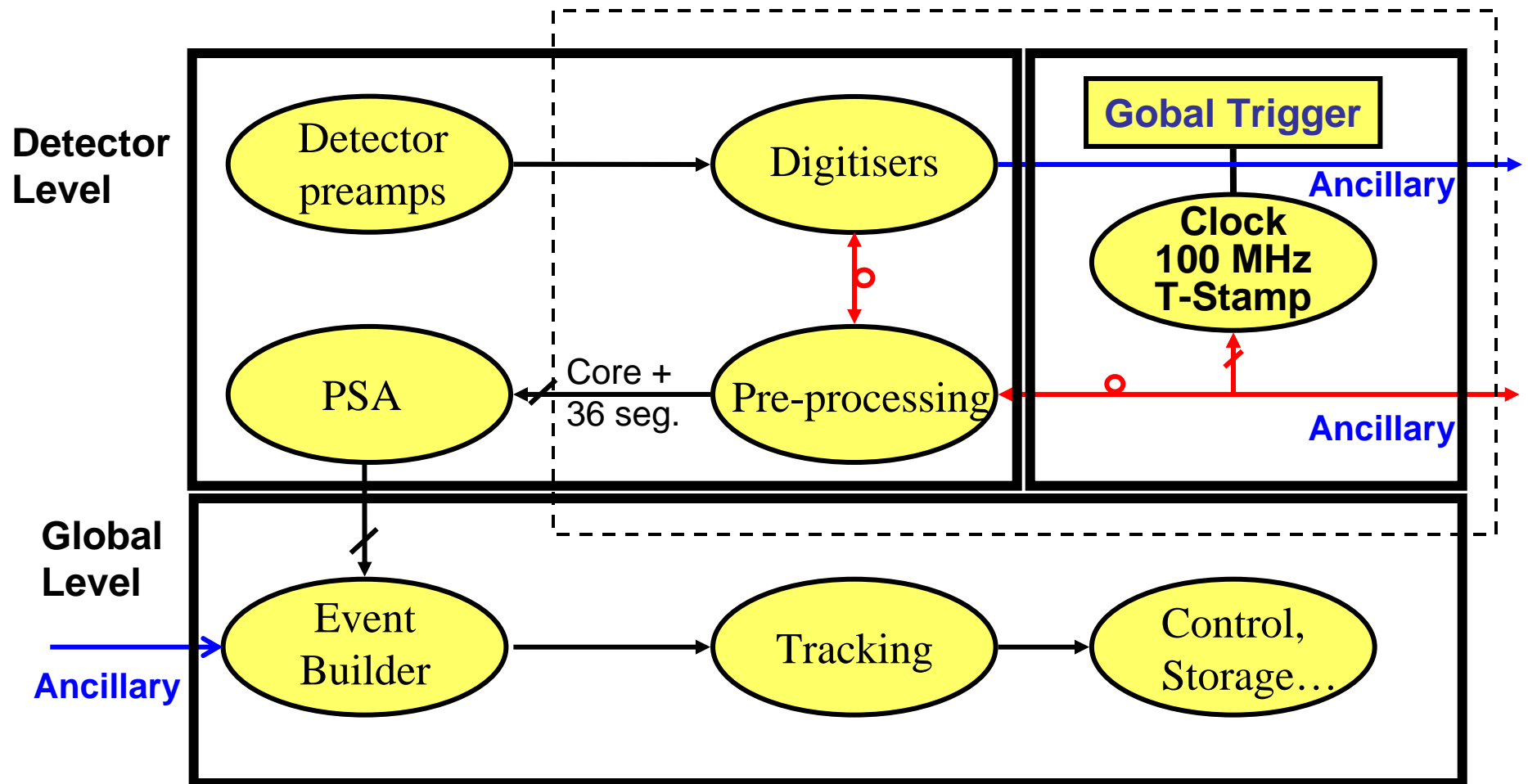


Front End Processing Working Group

- ❖ Digitisation P. Medina / P. Coleman-Smith
- ❖ Pre-processing I. Lazarus
- ❖ GTS M. Bellato
- ❖ PSA R. Gernhäuser / P. Desesquelles

9th AGATA Week, LNL, January 20-22 2010

Structure of EDAQ



Ancillary
detectors

- interface to GTS via mezzanine
- merge time-stamped data into event builder
- prompt local trigger available from digitisers

AGATA EDAQ Specs

- 180 segmented germanium detectors
 - 6840 channels high resolution channels
 - Up to 50 kHz singles rate
- Trigger rate
 - Up to 300 kevents/s at high multiplicity
 - Up to 3 Mevents/s at low multiplicity
- Real time operation of PSA and γ -ray Tracking
- Operation with other detectors

Specs for the Demonstrator

- **15 germanium detectors (5 triple clusters)**
 - 570 channels high resolution channels
 - Up to 10 kHz singles rate
- **Trigger rate \rightarrow up to 10 kHz**
- **Real time PSA at \sim 1 kHz/det. and γ -ray Tracking at \sim 10 kHz**
- **Operation with ancillary detectors**

Status

- The last *AGATA* week took place just after the first test experiment with one full triple cluster
- Now we operate 3 triple clusters
 - 9 digitizers
 - 18 ATCA carriers
 - 63 processing mezzanines
 - 9 + 5 *GTS* mezzanines (+1 in *AGAVA*)
 - Real time digital trigger
 - Readout to DAQ via PCI Express
 - No need to reboot every 5 hours thanks to B. Cederwall
- Can perform *PSA* in real time but don't trust it yet
 - store raw traces (14 MB/s/detector at 1 kHz)

Milestones

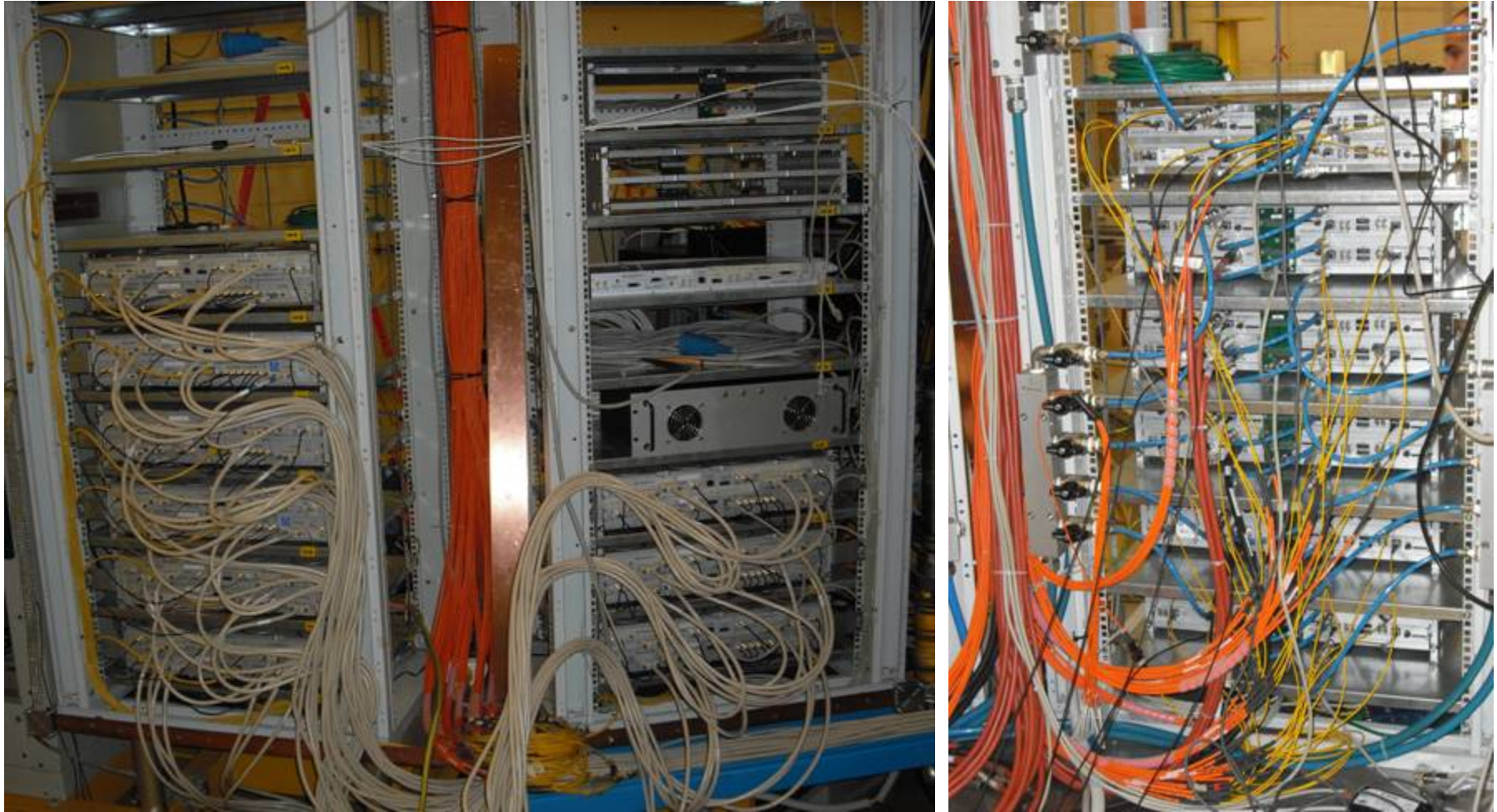
- 1st data out 2007 July
- 1st crystal 2007 September
 - week43
- 1st cluster 2008 August
- GTS tree 2008 December
 - week12
- Trigger 2009 March
 - week 22, week27
- 2nd cluster 2009 August
 - week 43
- Agava 2009 September
 - week 46, week 49
- 3rd cluster 2010 January

Commissioning experiments

	# TC	Ancillary	#Evts	
2009_week12	1		1 G	Triggerless
2009_week22	1	Dante*		Fail : evbuild problem due to unstable bits in timestamp (GTS or PS)
2009_week27	1	Dante*	150 M	OK
2009_week43	2	5 LaBr ₃ Si 16 strips	1 G	OK
2009_week46	2	PRISMA 2 Dante	100 M	Disaster : warm-up of detectors, no access to expt hall; ATCA electronics, AGAVA
2009_week49	2	PRISMA 2 Dante	500 M	OK: efforts to setup VME/AGAVA and PRISMA
2010_week06	3			

*Ancillary taken with AGATA electronics

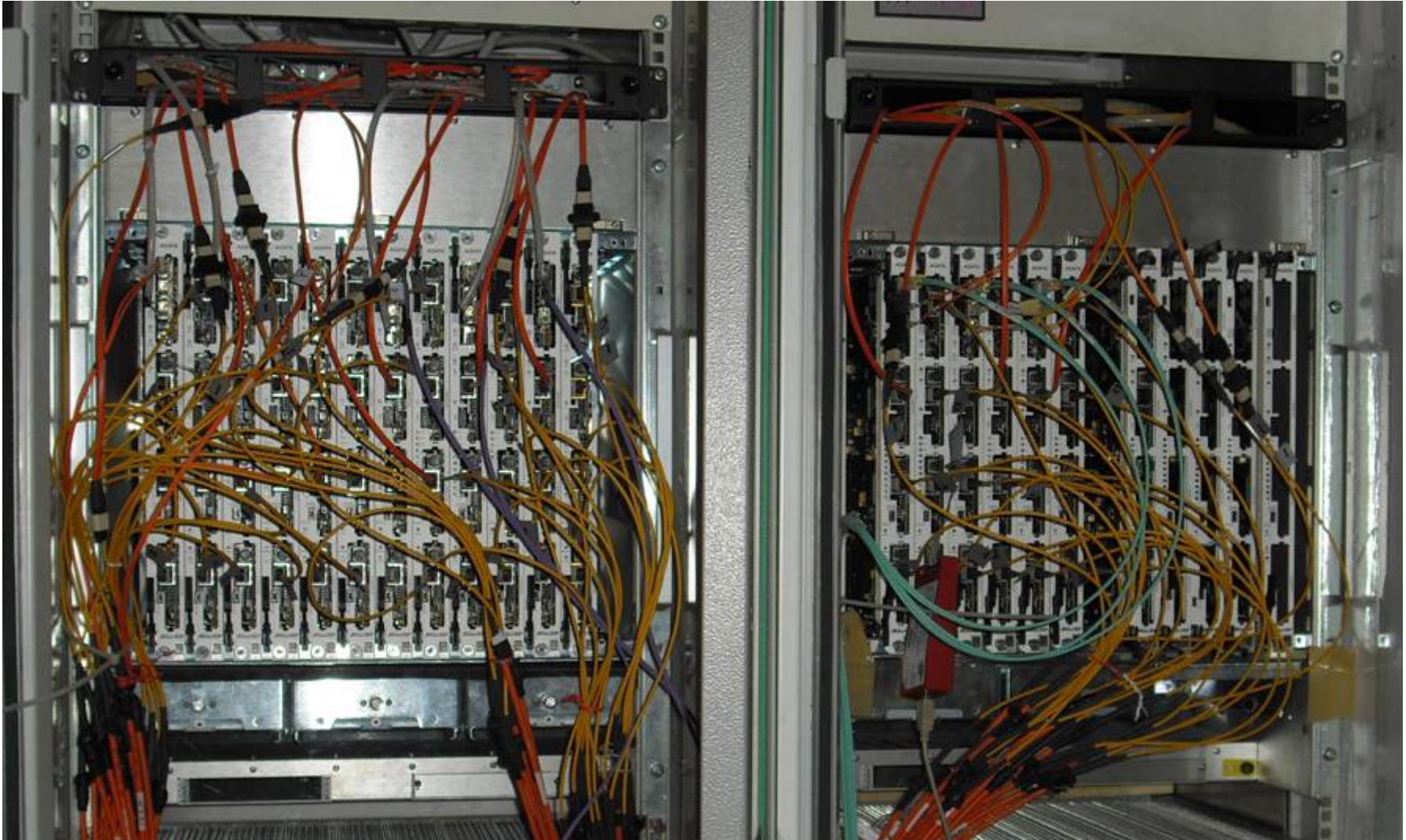
Digitisers in the experimental hall



1 digitizer per crystal

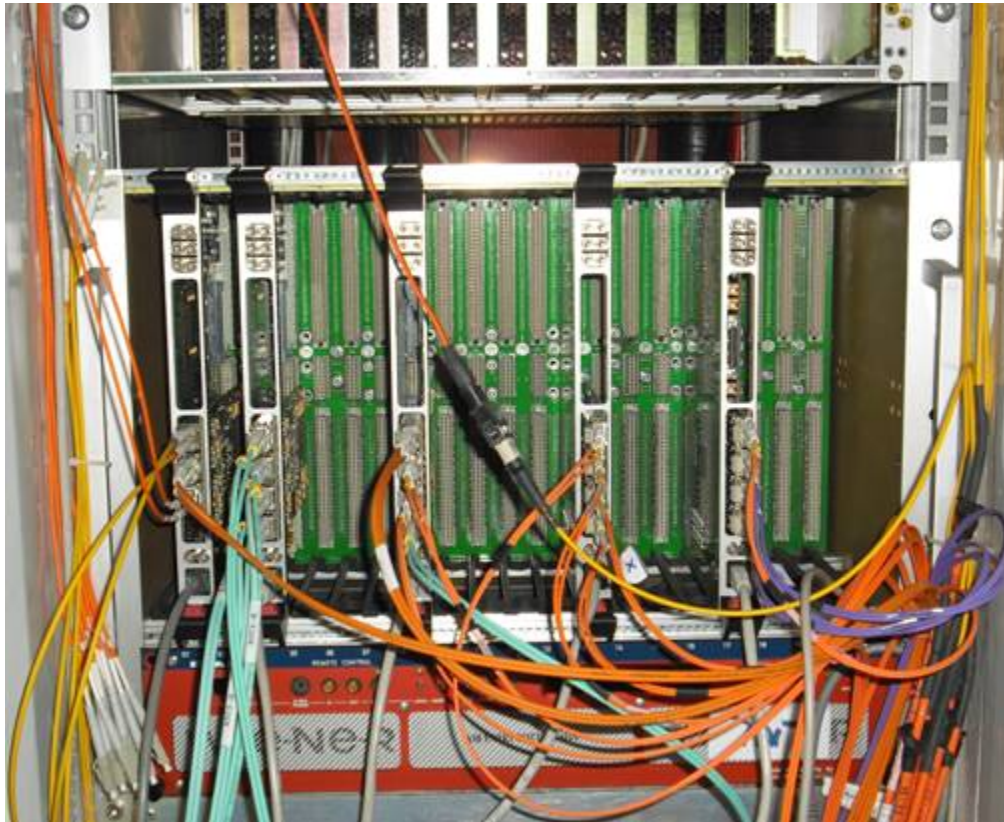
- core module with 1 core board and 2 segment boards (Sectors A B)
- segment module with 4 segment boards (Sectors C D E F)

Preprocessing electronics

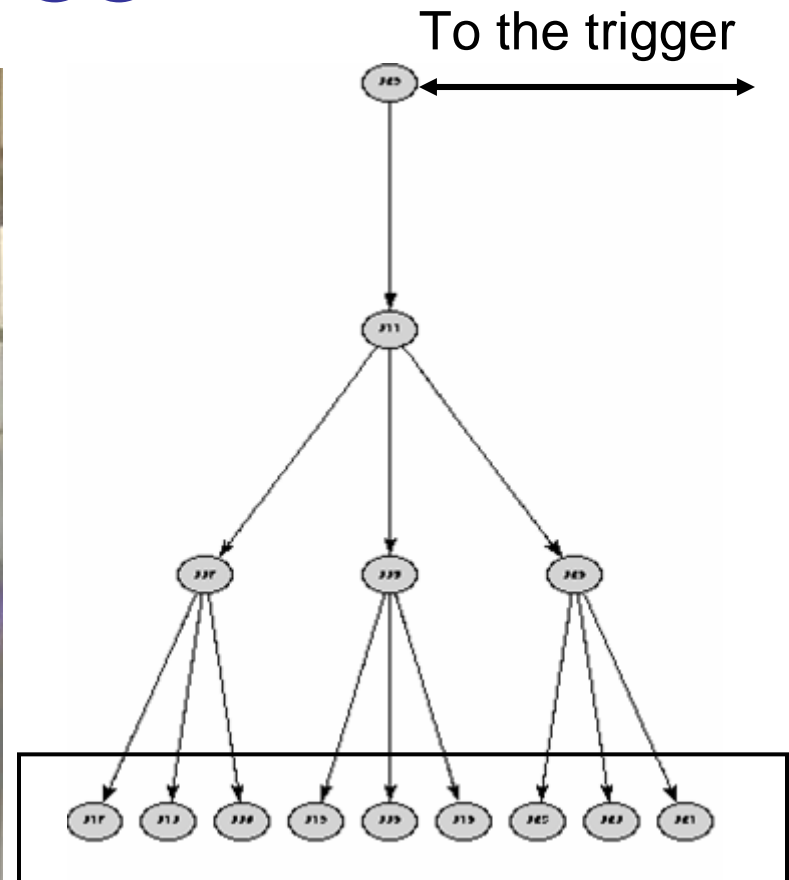


1 crystal needs : 2 ATCA carriers, 1 TCLK, 1 GTS, 7 segment mezzanines

GTS tree



A ternary tree for collecting the trigger requests, and distributing back the validations/rejections to GTS leaves



Max capacity of 2 levels
9 GTS → 6 triple clusters
1 AGAVA

Digital Trigger

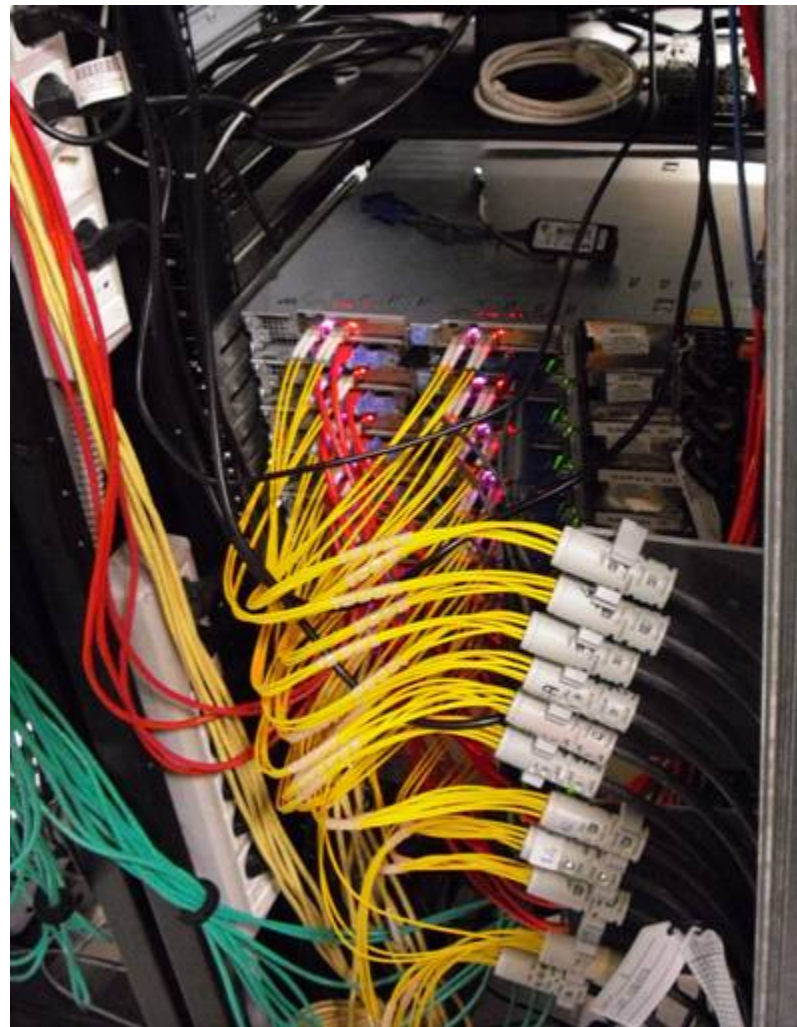


- Implemented by Luciano Berti (LNL) on a PCIe evaluation board with a Virtex4 FX100
 - Partly in firmware (partitions, sumbuses)
 - Partly in software running on the PPC
 - Present version: up to 48 inputs in 2 partitions
 - Each partition has 4 multiplicity thresholds
 - The two partitions can be in coincidence
 - Typically:
 - P1 with the Ge crystals
 - P2 with the ancillary
- Trig1 → $P1 \geq 1$ coinc. with $P2 = 1$
- Trig2 → $P1 \geq 2$

Readout machines in the AGATA PC farm



1 Pizza-box / crystal for :
Readout and local level processing



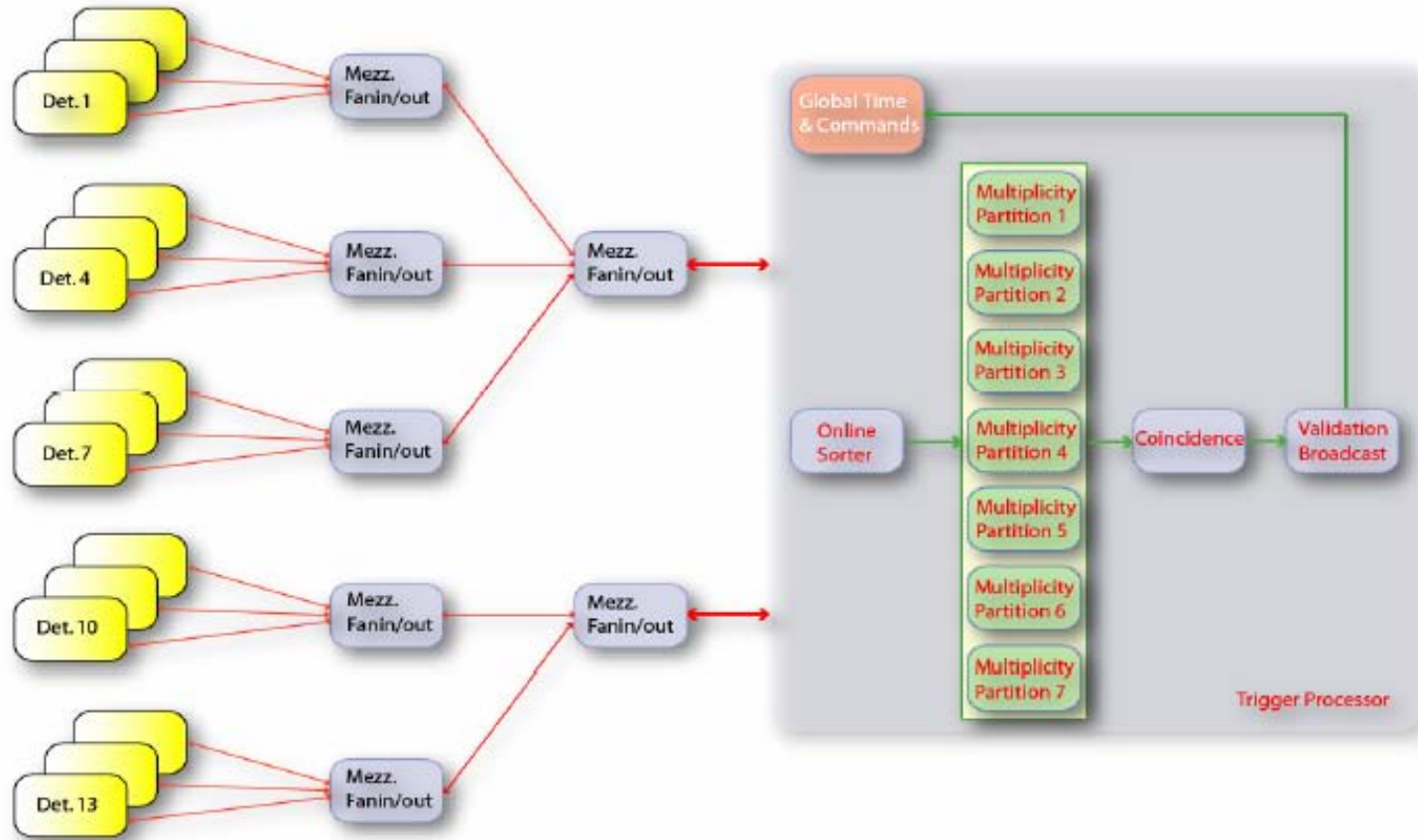
2 LINCO-1 transceivers / crystal

Global Trigger Processor

Joël Chavas

Marco Bellato

Luciano Berti



Max 1 MHz trigger requests/channel

100 kHz coincidences (limited by PPC)

The new GTS Trigger Tree

- The ternary GTS tree is not optimal for a large number of detectors:
 - “waste” of input ports to connect up
 - each new level adds a latency
 - each GTS needs a VME carrier
- A more efficient (“final”?) solution is being developed; prototype in a few months
- Instead of what presented in AW8-Köln:
- Uses the present ATCA carrier
- Using the present GTS-tree firmware
- Only new component is a passive backplane to distribute the clock
- Multiplexing factor is now 16/1
- One full ATCA crate → 200 nodes



Trigger firmware being ported by Luciano in a cheaper, and bigger, Virtex5
Plans to move it further to a Virtex6, with the second level logic in PC's CPU

Vic's

AGATA Digitizer: control @ digitizer1-sc client address is 192.168.170.2

Select Hardware

Digitizer: 7 | FPGA: Core: Main Board | Select | Probe Digitizer Hardware | Read PROM

Select Detector/Crystal/Segment

Detector: 02 | Crystal: G | Segment: - | Select

Restore settings for detector 02_G from the DataBase | Save settings from detector 02_G to the DataBase

Setup

SetUp Current FPGA | SetUp Current Digitizer | SetUp All Digitizers | ReSync Current Digitizer Optical Link | ReSync All Digitizer Optical Links

Check Current Digitizer | Check All Digitizers

Show Session Options

Empty Log Window | Send Log Window to ELog | Reload | Reset | Show Variables | Show Log Window | Enable Logging

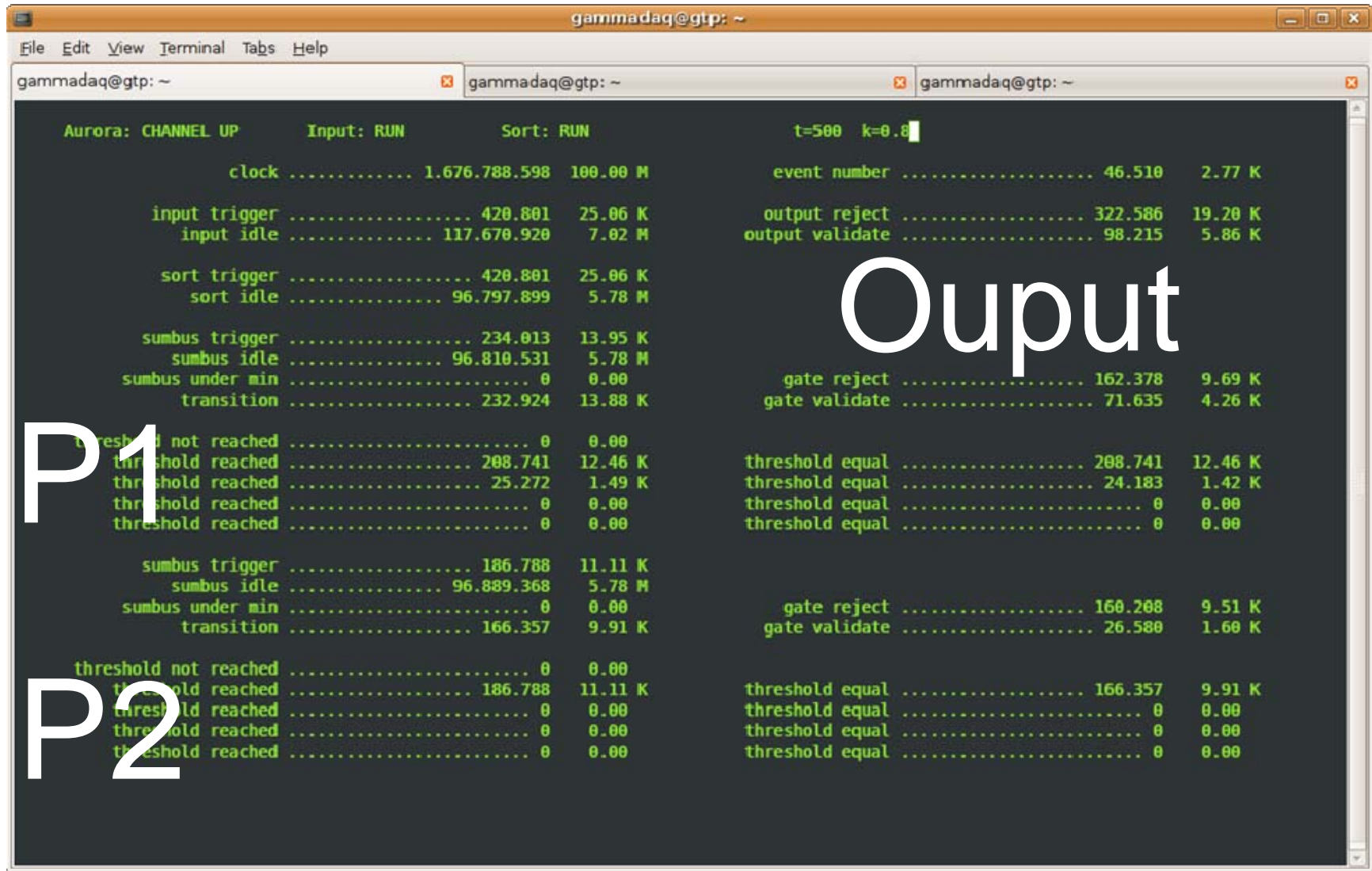
Core Preamp Pulser Control | Core Trigger Block Control | Data Communications Control | Temperature Monitoring | Digitizer Diagnostics | Hardware Configuration

Last Updated: January 19, 2010 13:52:00

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Done

Luciano's



More “visual” diagnostics with spectra of time distributions planned.

Electronics : available and needed

Built by AGATA	Built	Tested	In use (3 TC)	Needed for 6 TC	Needed for 8 TC
Digitiser	18 (+7 new?)	13	9	18	24
ATCA carrier (+tckl)	39	25	18	36	48
GTS mezzanine	20 (+13)	20	15	18+4 ^{&} +2 [#]	24+6 ^{&} +4 [#]
Segment mezzanine	117	110	63	126	168
PCIe adapters	10* (+ 10**)	20*+2**	18*	12* + 12**	24**
PS for digitizers	5	5	3	6	8
Commercial					
ATCA crates	1 / 2TCs		2	3 + 1 ^{&}	4 + 1 ^{&}
Fibres Digi.-Preproc.	7 / TC + 1		42 + 1 + 7	36	
Optical splitters	1 / crystal		9	18	24
Fibres Prepr.-DAQ	1 / crystal		9		
Fibres for trigger-tree	1+ /crystal		13		
Optical transceivers	12+ / crystal		~110		

*LINCO1 2/crystal **LINCO2 1/crystal or 0.5/crystal

& Assuming new trigger tree

#For AGAVA

Status - firmware/software

- Digitizers
 - Mainly done
 - Implementation of ToT processing firmware started at RAL
- ATCA carrier board
 - Main developments done
- Processing mezzanines
 - Basic implementation done
 - Development of new version on going at Orsay
- GTS
 - Trigger tree for up to 9 clusters
- Global trigger
 - In use since almost one year

Todo's for firmware and software

- Remove know bugs
- Reduction of event dead time from 25 μs to $\sim 1 \mu\text{s}$
- Implementation of per-channel setup parameters
- Testing the exponential-average self-triggered blr
- Reduce number of readout samples from 160 to 80
- Verify if possible to use CFD keeping low thresholds
- Improve diagnostics
 - Counters of local triggers, validations, rejections, ...
- Readout of long traces
 - 100 ks if one channel;
 - 10-20 ks if 6 channels in parallel

AGATA week 2009, Köln

Todo's for firmware and software

- Remove bugs
- Reduction of event dead time from $11.5 \mu\text{s}$ to $\sim 2 \mu\text{s}$
 - implies major firmware redesign for the processing mezzanines
- Implementation of per-channel setup parameters
- Testing the exponential-average self-triggered blr
- Reduce number of readout samples from 160 to 80
- Improve diagnostics
 - Counters of local triggers, validations, rejections, ...
- Readout of long traces
 - 100 ks if one channel
 - 10-20 ks if 6 channels in parallel

AGATA week 2010, LNL

General schedule for 2010

- Completion of HW/FW/SW for 5 TC
- Start checking the timing performance
- Development of the final trigger tree
- Implementation of more partitions and coincidences in the digital trigger
- Continue improving firmware and software
- All to be carefully planned because we are facing a phase transition from development real experiments already scheduled
 - 18-23 February
 - 5-7 March
- **Improve controls and monitoring**

Program of the session

- Control and readout of the ATCA electronics
→ Damiano Bortolato
- Preprocessing electronics
→ Nabil Karkour

Electronics : available and needed

Built by AGATA	Built	Who	Needed for 6 TC	Needed for 8 TC
Digitiser	18 (+7 new?)	Strasbourg Daresbury Liverpool	18	24
ATCA carrier (+tckl)	39	Padova Orsay (IPNO)	36	48
GTS mezzanine + Trigger	20 (+13)	Padova / LNL	18+4 ^{&} +2 [#]	24+6 ^{&} +4 [#]
Segment mezzanine	117	Orsay (CSNSM)	126	168
PCIe adapters	10* (+ 10**)	Padova	12* + 12**	24**
PS for digitizers	5	Saclay (CEA)	6	8