Status of the AGAVA Interface

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How to link Trigger and Triggerless DAQs

Ancillary det.
e.g. FRS, PRISMA

Prompt trigger < 500 ns

AGATA

Digitizer

Pre-processing

PSA

Event Builder

Ancillary Merge

Tracking

Data analysis

GTS supervisor

GTS tr.

Ancillary Analogue FEE

Req

Req

Trig-Val/Rej

Ancillary VME

AGAVA

GTS tr.

Slow control:
Kmax, Labview, Midas, etc.

DATA

Tir stamp

Ancillary readout

Pre-processing

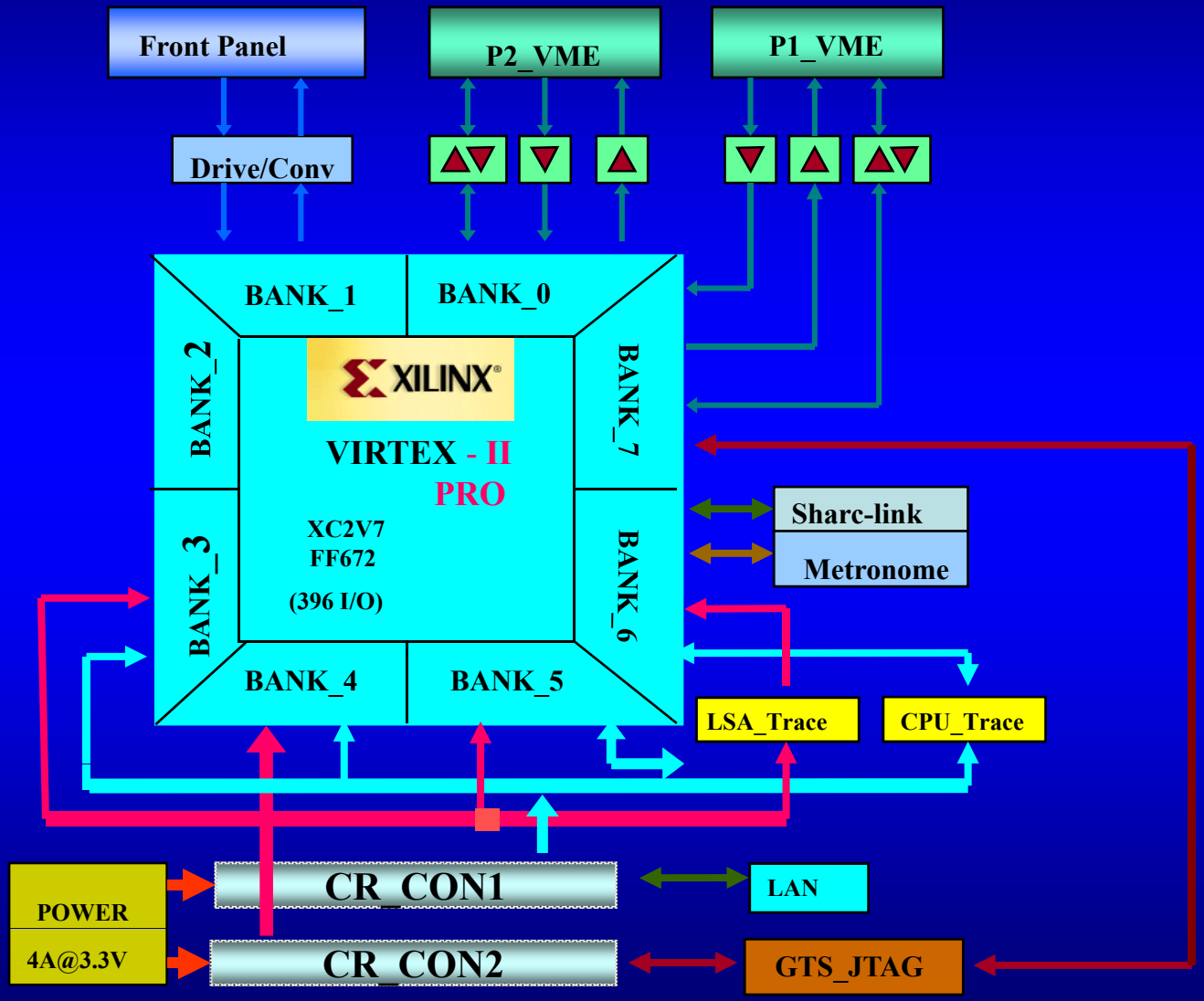
NARVAL producer:
filtering, kinematics reconstr.

AGATA VME ADAPTER

Main AGAVA features

- **Main task of AGAVA is to merge the AGATA triggerless timestamp system with DAQ that uses a trigger.**
- **AGAVA interface is a slave single width VME module.**
- **It is a carrier board for the GTS mezzanine card used in the AGATA experiment for the global clock and timestamp distributions.**
- **Logic of the module is controlled by FPGA Virtex II Pro.**
- **AGAVA works in VME and VXI Exogam-like environments.**

Block diagram of the AGAVA module

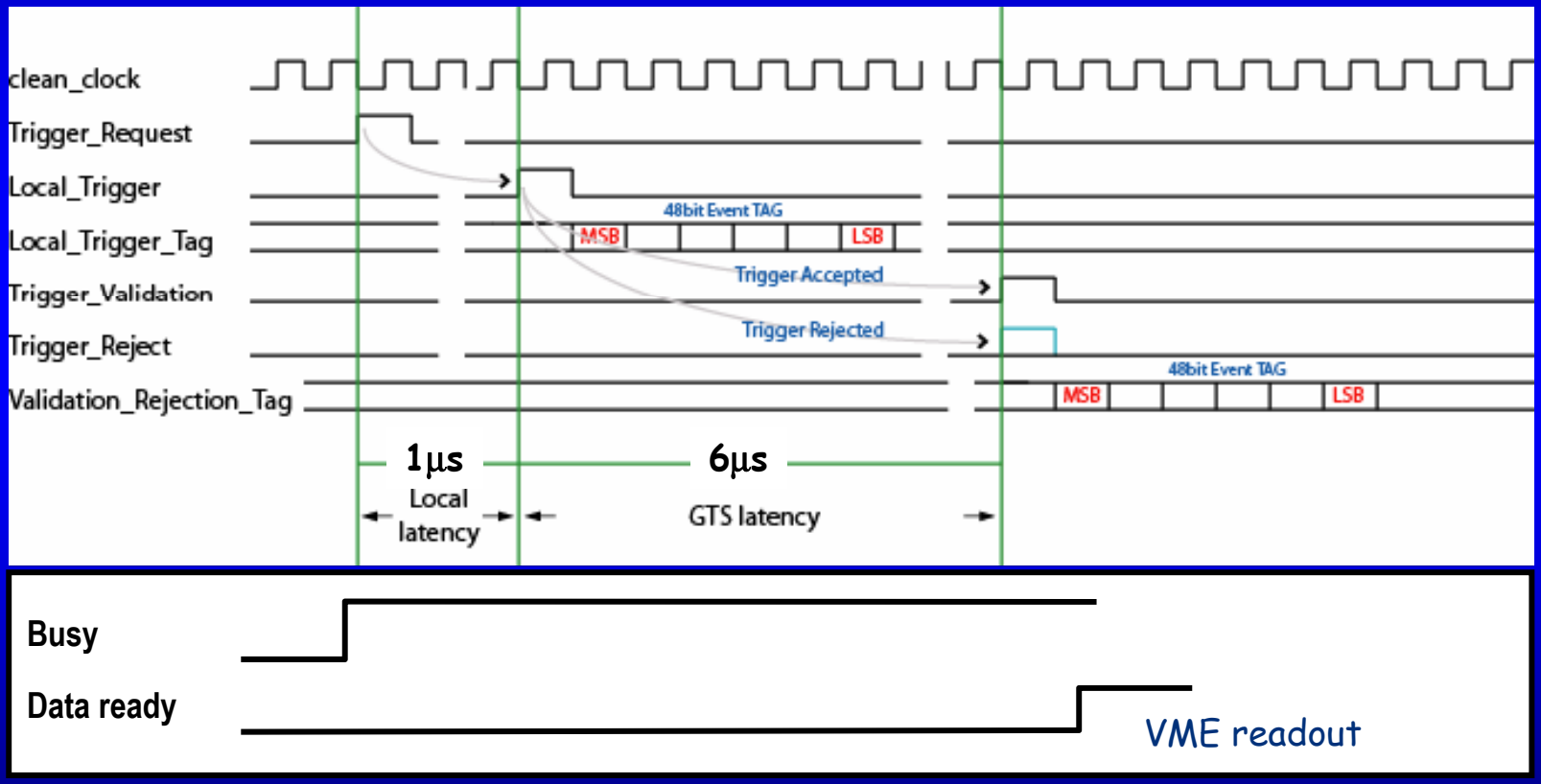


Types of operations in AGAVA „slow trigger mode"

- Standard VME access
- CBLT mode
- VXI EXOGAM-like mode

GTS Trigger request and validation timing diagram

AGAVA respects the GTS protocol:



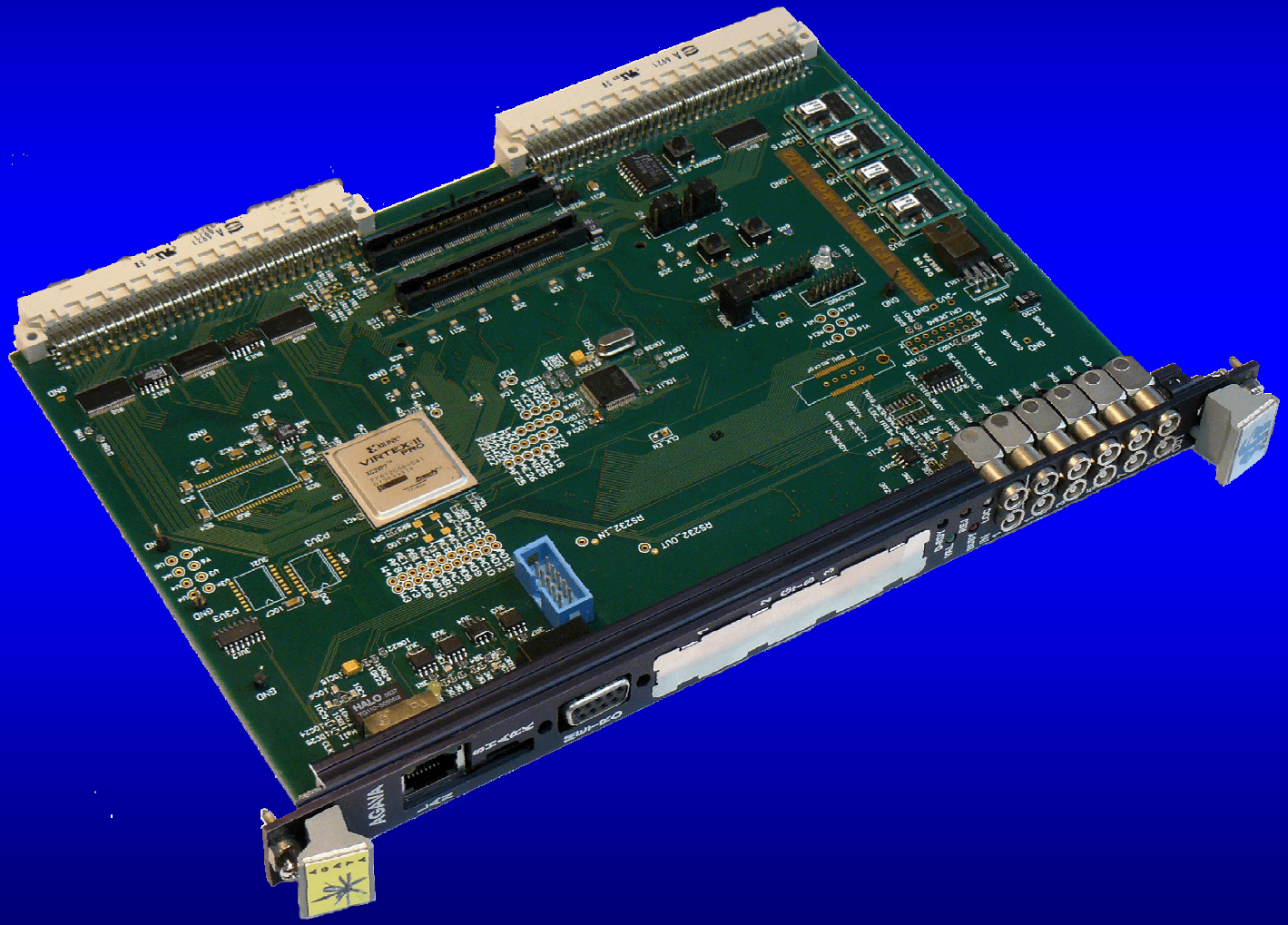
AGAVA registers

- Status Register and counters of Trigger Input, Local Trigger, Validation, Rejection,Timeout
- Group of registers with GTS data:
  - Local Trigger, Validation, Rejection Tag
  - LLP, GTS Status, MSG In
- Group of CBLT control registers
  - CBLT Status, CBLT Address, Header, Trailer
- VXI ID registers
- Inspection line registers
  - Ftrigger, Data ready, Fast Clr, GTS Clock Ok, VXIblt_mode, VME control lines

Readout of the AGAVA module

- A32/D32 VME standard access to the registers:
  - AGAVA status,
  - 32 bit counters for Local Trigger, Validation/Rejection, Timeout
  - Local, Validation, Rejection Tag (48 bit),
  - Event Number (24 bit)
  - GTS status (LLP Status, GTS status, MSG IN) (8 bit)
  - Group of registers to control CBLT data flow
  - Group of 23 VXI ID specific registers
- CBLT mode daisy chain block transfer (14 words)
- VXI Exogam – like mode (23 words)

AGAVA module



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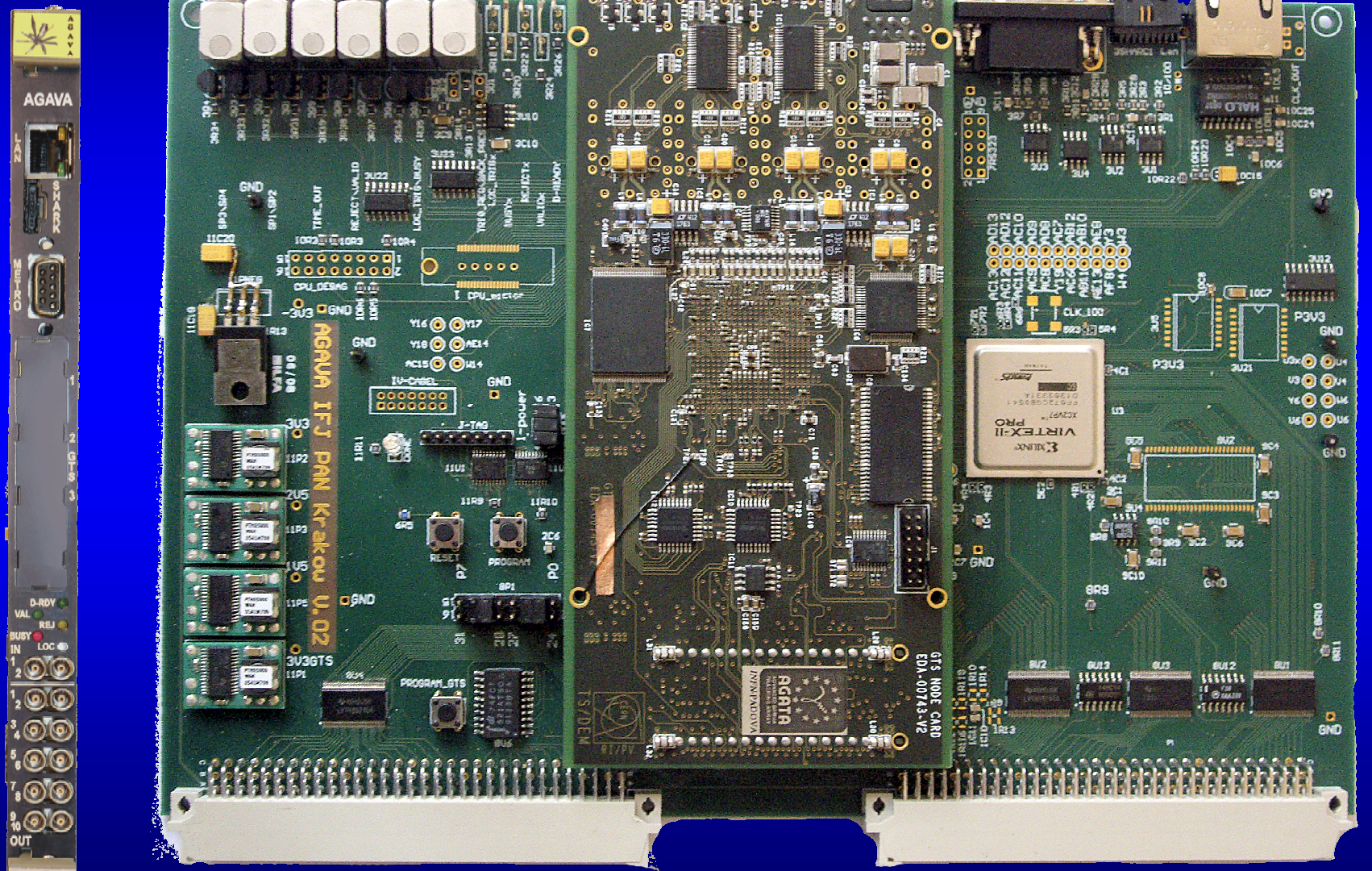
AGAVA with GTS mezzanine



Laboratory tests of the AGAVA module

- CBLT and the standard VME access modes at Legnaro,
  - Compatibility of the new release of AGAVA with the GTS 2 (Virtex 4 , 200MHz) mezzanine card
  - Proper behavior at high external trigger rate
  - Test of the Ethernet connection
- AGAVA in the VXI environment at GANIL

AGAVA test in PRISMA-like VME environment

- VME test bench from INFN Milano
  - STRUCK SIS1100/SIS3100 PCI/cPCI to VME interface (DSP -SHARC ADSP-21062L)
  - AGAVA board release 1 and 2, GTS release 1 and 2
  - CAEN V785 32 channel ADC
  - CAEN V775 32 channel TDC
  - CAEN V538A 8 channel NIM-ECL/ECL-NIM Translator
- CBLT sequence: AGAVA, TDC, ADC
- External trigger
- Kmax dedicated application to control the VME modules, buffers readout and online sorting

Summary of tests

- Acquisition rate ≈ 10 kHz both in single and in CBLT access
- System stability: 8 hours test without any problem (repetitive)
- All of ~300 Mevents were good and well formatted
- Local Trigger Tag / Validation Tag always consistent

In-beam test at PRISMA

System configuration

- 2 AGATA triple clusters, 5 $LaBr_3$
- CAEN V2718 PCI to VME controller and the PRISMA FEE VME electronics

Four days succesfully running

- 5 $LaBr_3$
- 1 DSSD Si detector with 16 segments

3 days running

Summary

- 4 modules tested in a laboratory and in real experiment environment
- AGAVA module fully worked as predicted

Thank you

Preparation for the next step

- It is foreseen to use AGAVA as the AGATA – FRS interface @ PRESPEC in GSI
- Connection with FRS need a few modules of AGAVA

Slow Trigger Mode

- Start with Ancillary Trigger – NIM input or bit in the Status Register
  - Enabled with bit in Status Register
  - Synchronized with 100 MHz clock from GTS mezzanine, 10ns width
- It produce Busy signal (NIM output) and Trigger Request to GTS system
- After less then 1 us GTS mezzanine sends to AGAVA Local Trigger and 48 bits Local Trigger Tag
  - Local Trigger Flag: NIM out , Status Register, LED
- On Trigger Request GTS system sends:
  - Validation signal , 48 bits Validation Tag and 24 bits Event Number
    - AGAVA action - Validation Flag: NIM out , Status Register, LED
      - after 9 clocks Data Ready: Flag Status Register, LED
  - Rejection signal, 48 bits Rejection Tag
    - AGAVA action Rejection Flag: NIM out, Status Register, LED
- AGAVA timeout signals in absence of:
  - Local Trigger (2 us)
  - Validation\Rejection Tag (300 ms)

    Timeout Flag:NIM out, Status Register, LED

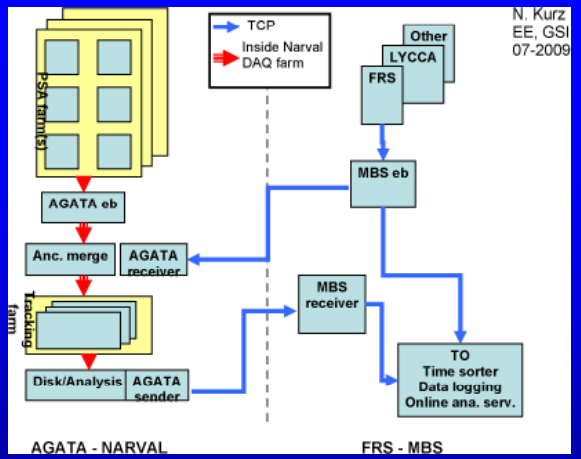
Preparation for the next step

Use several AGAVA-GTS to assure time stamping and trigger synchronization of several VME crates. Replacing the Titris time stamp module

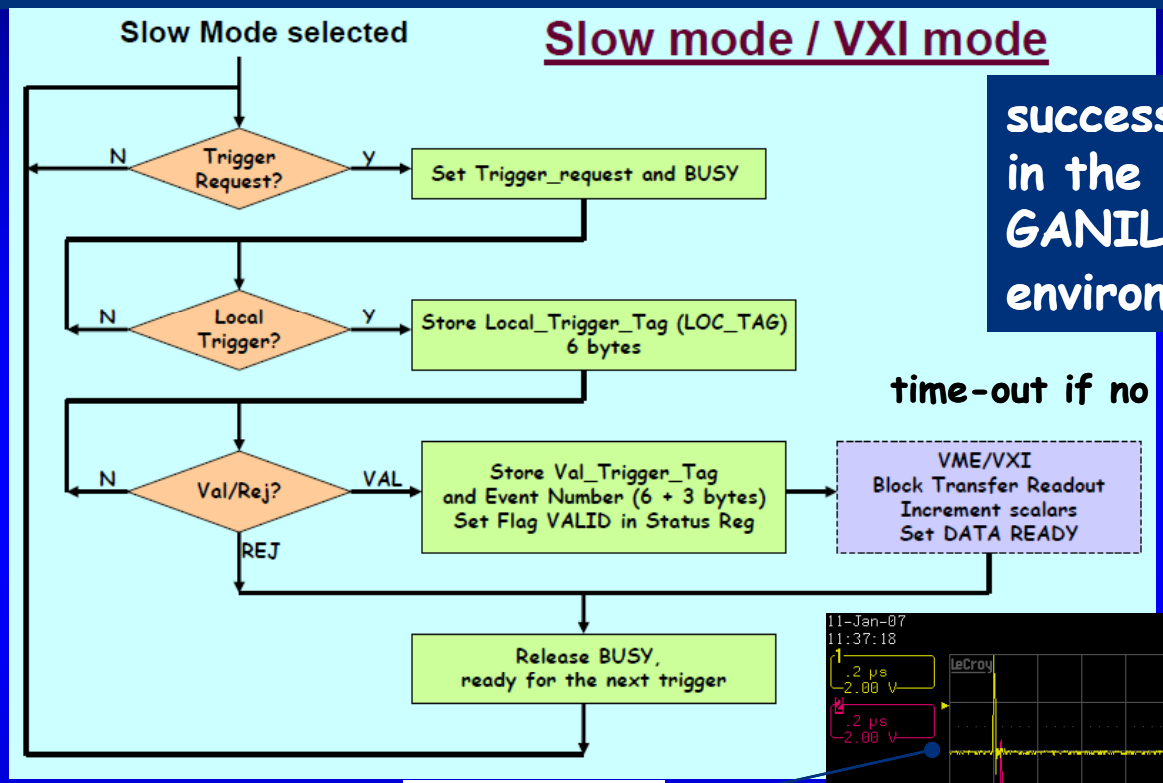
To improve the trigger rate of the GSI system

- to use the multi-event buffers of the CAEN VME module in PRESPEC.
- a firmware upgrade should be made in the AGAVA card. Piotr agreed that the Cracow engineers who developed the AGAVA could perform the change. We should inform them with enough notice.

Another request related to the AGAVA and generating from GSI is the possibility to connect it to a BuTiS clock. The way to do it, the efforts and a schedule has to be defined



The slow operation mode



successfully tested in the LNL-VME and GANIL-VXI environments

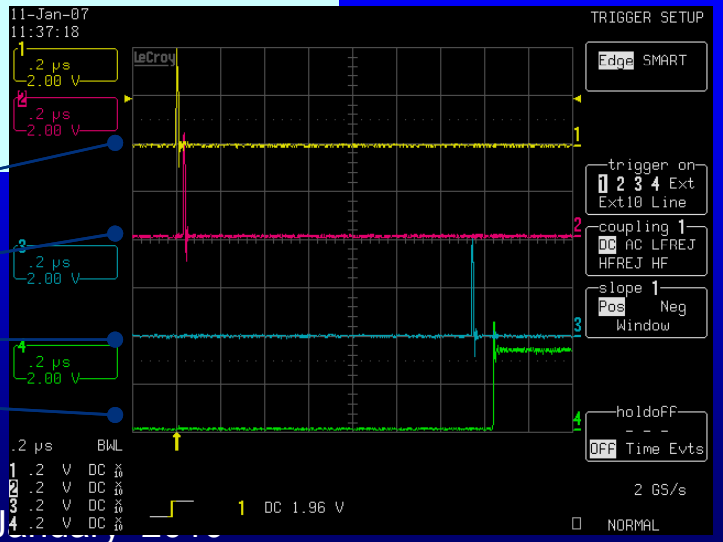
time-out if no Val/Rej

Trigger req.

Local Trigger

Validation Trigger

Data ready

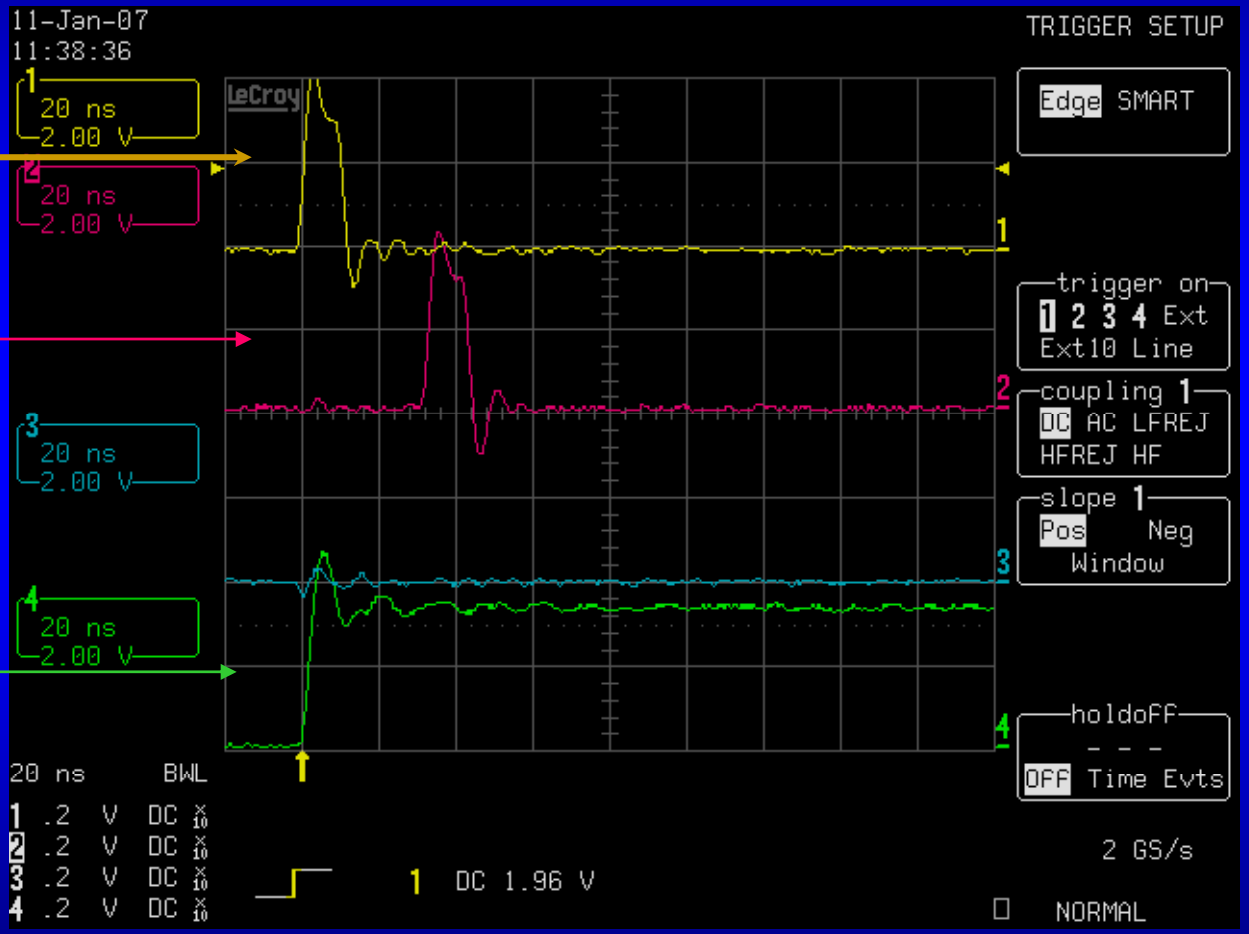


Timing of important signals

Internal Trigger

Local Trigger

Busy



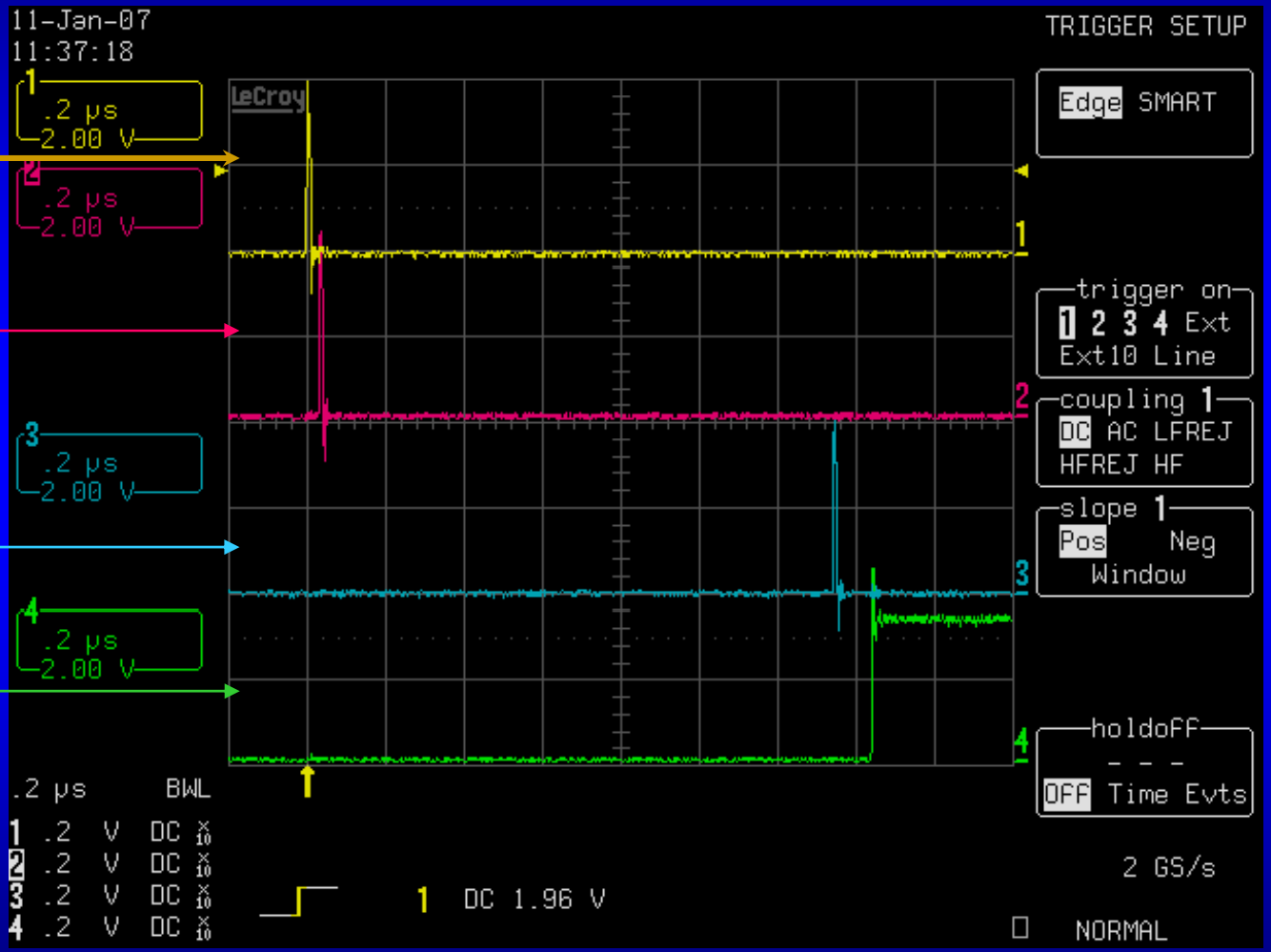
Continuation

Internal Trigger

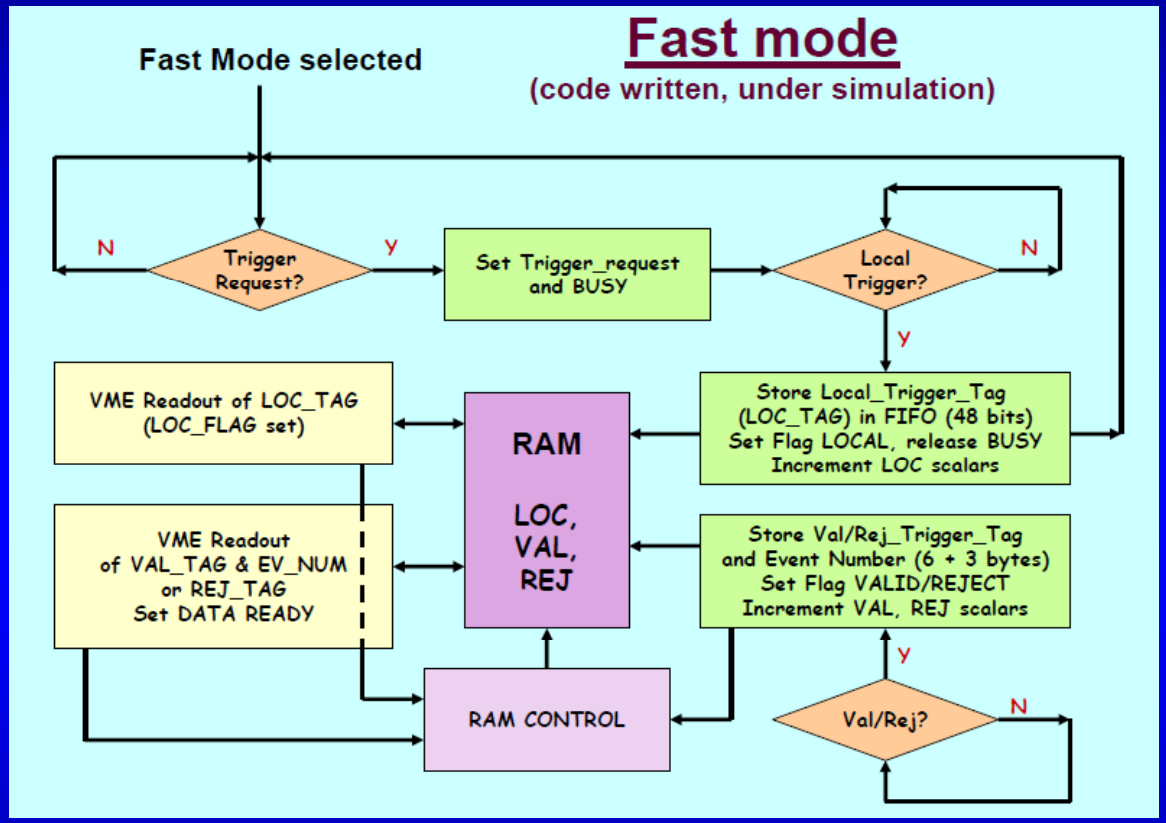
Local Trigger

Validation Trigger

Data ready



The fast operation mode

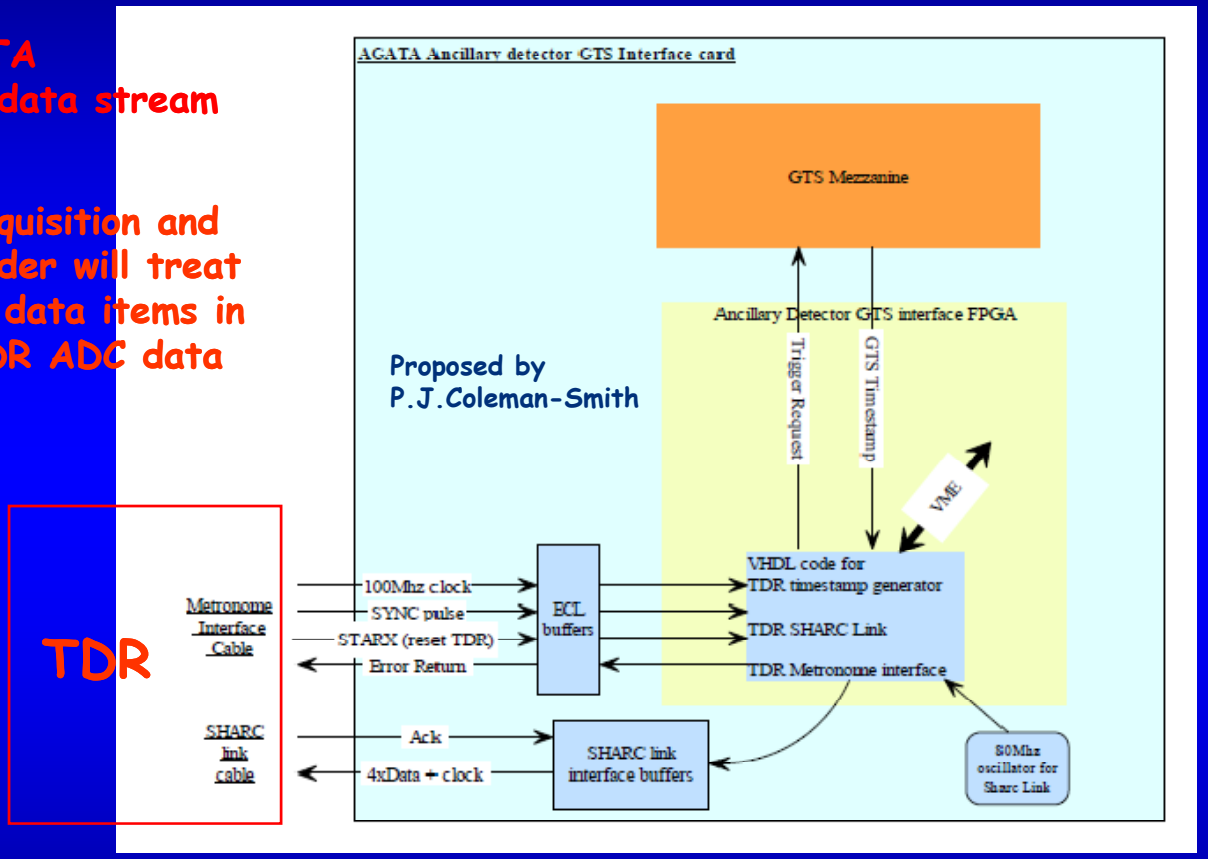


Idea:

- **Do not wait for the whole Loc_Trig-Val./Rej. sequence**
- **Read out the two Tags independently**
- **Synchronize and filter data stored in a memory**

Connection to TDR

- Idea: insert the AGATA timestamp into the TDR data stream
- The TDR data acquisition and Software Event builder will treat the GTS timestamp data items in the same way as TDR ADC data items.



Hardware prepared, but not tested