Preliminary studies on PSD components

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Simulation of light propagation inside the scintillator tiles

- Optimization of SiPM number and position
- Comparison between different types (size and number of cells)

Test on tile prototypes

- Scintillator tiles preparation
- SiPM board design
- DAQ chain setup

Simulation of light propagation

The light propagation inside the scintillator (reflection and attenuation) has been simulated using the *historical* GUIDE7 program (CERN, 1976)

Scintillator tiles of 5x5 cm² and 10x10 cm² have been simulated (0.5 cm thickness)

The photons are generated along the track of a single *m.i.p.* crossing the tile perpendicularly

The number of photons collected by a single SiPM **strongly** depends on the track and SiPM positions

The average over a conveniently large number of tracks, randomly distributed on the tile surface, is considered

The signal given by the (normalized) sum of one or more SiPMs (n=1, 2, 3,...) is analysed

The goal is to find the configuration with smaller amplitude spread, to reduce the geometrical dependence



Amplitude spread for a 4-SiPM geometry – single SiPM readout

read SiPM



(perpendicular m.i.p. track)

Amplitude spread for a 4-SiPM geometry – multiple SiPMs readout

read SiPM



toph1+toph2+toph3+toph4+both1+both2+both3+both4

⁽perpendicular m.i.p. track)

Amplitude spread for a 3-SiPM geometry

read SiPM



⁽perpendicular m.i.p. track)

Comparison between 3 and 4 SiPMs geometries (5x5 cm² tile)



3x3 mm² SiPMs 50 μ m pitch λ_{att} = 380 cm

(perpendicular m.i.p. track)

Note: the number of collected photons is higher in the 3 SiPMs geometry, because the total reflecting area (on the tile's edges) is larger

10x10 cm² tile (with the same "proportions" as the 5x5 cm² one)



Comparison between all the simulated geometries



Remarks:

- the signal spread decreases with increasing number of SiPM
- the double-side readout don't produces relevant improvements (compare the 3 and 4 SiPM with 6 and 8 SiPM configuration)
- the 10x10 tile is only slightly worse than the 5x5 one

Hardware in Pavia

Test on tile prototypes

A certain amount of scintillator is available to build some prototypes

Planned size: 5x5 cm², 10x10 cm² (and eventually also 10x20 cm²) (0.5 cm thickness)

Different 3x3 mm² SiPM available: Hamamatsu S12572-050P (50 μm pitch) AdvanSiD RGB (40 μm pitch) AdvanSiD NUV (40 μm pitch)

SiPM board already designed with multiple soldering pads, to allow different geometric arrangements with 1, 2, 3 or 4 (and even more...) SiPM

2 different sizes: $5x0.5 \text{ cm}^2$ and $10x0.5 \text{ cm}^2$

Advan PO# h	SiD 4	Pcs A2		
SIPM Size O 1x1 O 1.2c S 3x3 O 4x4 O	Package 158. CSP O Die O TO O Socket O	SIPM Type SA, RGB O NUV Microcell Aloum O	and a second	



AdvanSiD NUV $3x3 \text{ mm}^2 40\mu \text{m}$ cells

Advans	SiD RGB
$3x3 \text{ mm}^2$	40µm cells

Type No. S12572-050P	Precaution for use
Guantity[pc] 100	
Serial No. 3128 ~ 3227	
Lot No.	
HAMAMATSU	
MADE IN JAPAN	

HAMAMATSU S12572-050P $3x3 \text{ mm}^2$ 50µm cells



SiPM positions (mm) (x2 for the 10x10 cm² tile)

printed board layout (parallel connections)



Read out hardware in Pavia

DAQ chain (2 possibilities):

CAEN V1751 module (8 channels, 10 bit, 1 GS/s) connected to
 Linux server with CONET2 optical link (80 MB/s)
 OR

Digital oscilloscope

Availability of a small 90 Sr source (~0.5 MeV β^{-})

Printed Circuits

- Using a 2018 order still open, we prepared a layout suitable for 10cm scintillator readable side
- The layout is compatible to the devices we have in Pavia: 3 x 3 mm², Hamamatsu (S12572-050P, 50um cells) and Advansid (NUV and RGB, 40um cell)



SiPm mounting

Considering the parallel connection, we decided design only one kind of layout and then to mount just few SiPM each board in order to investigate all the configurations.

On the right some solutions that can be used.



Production of printed circuits

- Printed circuits are on production by Phoenix S.r.l. Via Burolo 22, 10015 Ivrea and will be ready by the end of this week
- Selection of SiPM (based on breakdown voltage) and group them in order to have the same working point will be done this week

On July, 8 th, SiPM will be inserted in the oven for baking at 60°C for a couple of days and then stored in vacuum bag for transport.
On July 11 or 12 th, SiPM will be carried to Me-Electronics S.r.l. (Montaggi Elettronici) Via Levrini, 4, 25080 Levrini BS in order to solder SiPM on the boards at low Temperature to avoid damage on SiPM windows.

•X-ray control of the solder

Scintillator in Pavia

- In Pavia we have two scintillators bars of EJ-200 of the following dimenstions:
 - 1000 x 100 x 10 mm3
 - 500 x 100 x 10 mm3
- From the second one, we cut 2 pieces :
 - 100x 100 x 5 mm3
 - 150 x 100 x 5 mm3
- The 100mm side is the one that will be read with SiPM printed circuit
- Optical coupling between Scintillator and SiPM printed circuit will be done with optical grease

