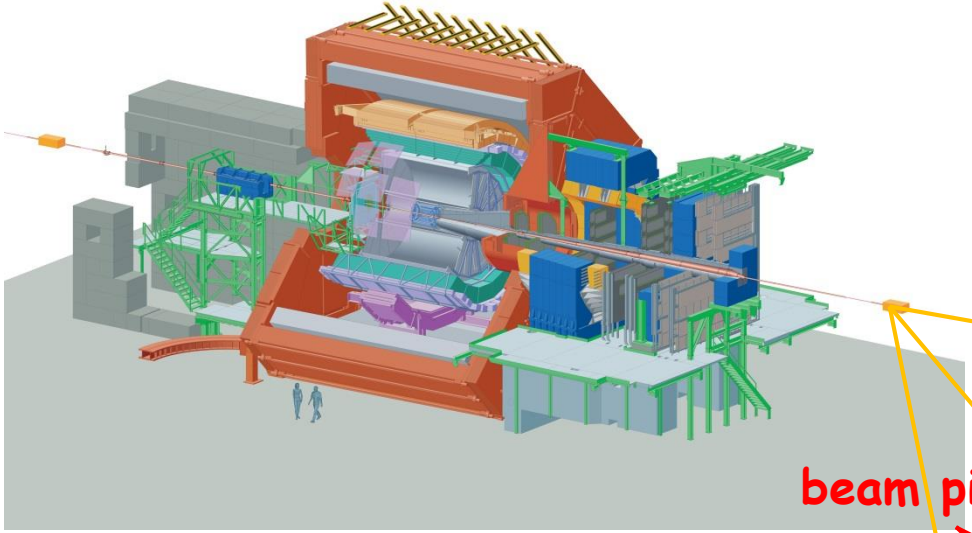
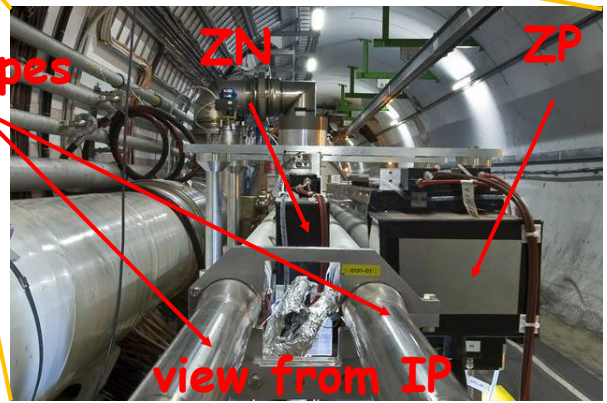
ALICE/ZDC



Progetto 100% INFN
Sezione INFN Cagliari
Sezione INFN Torino
(istituti di Alessandria e Torino)



Il progetto ZDC consiste in 2 coppie di calorimetri adronici (112.5 m da IP2) e una coppia di calorimetri elettromagnetici (7.5 m da IP2).

ZDC in PbPb2018

The ZDC was fully operational during the Pb-Pb run in November-December 2018 thanks to the fact that ALICE agreed with LHC a low crossing angle (+/-60 microrad).

During this period the ZDC operated as
- the ALICE luminometer, measuring the rate of neutron emission in e.m. dissociation + hadronic interactions -> ZNC signal (σ = 213 b)
- trigger detector providing:
  - the (ZNA and ZNC) signal, which tagged essentially neutrons emitted in hadronic interactions and was used to increase the purity of the sample of minimum bias events
  - the (ZNA or ZNC) signal, which tagged essentially neutrons emitted in EMD interactions.

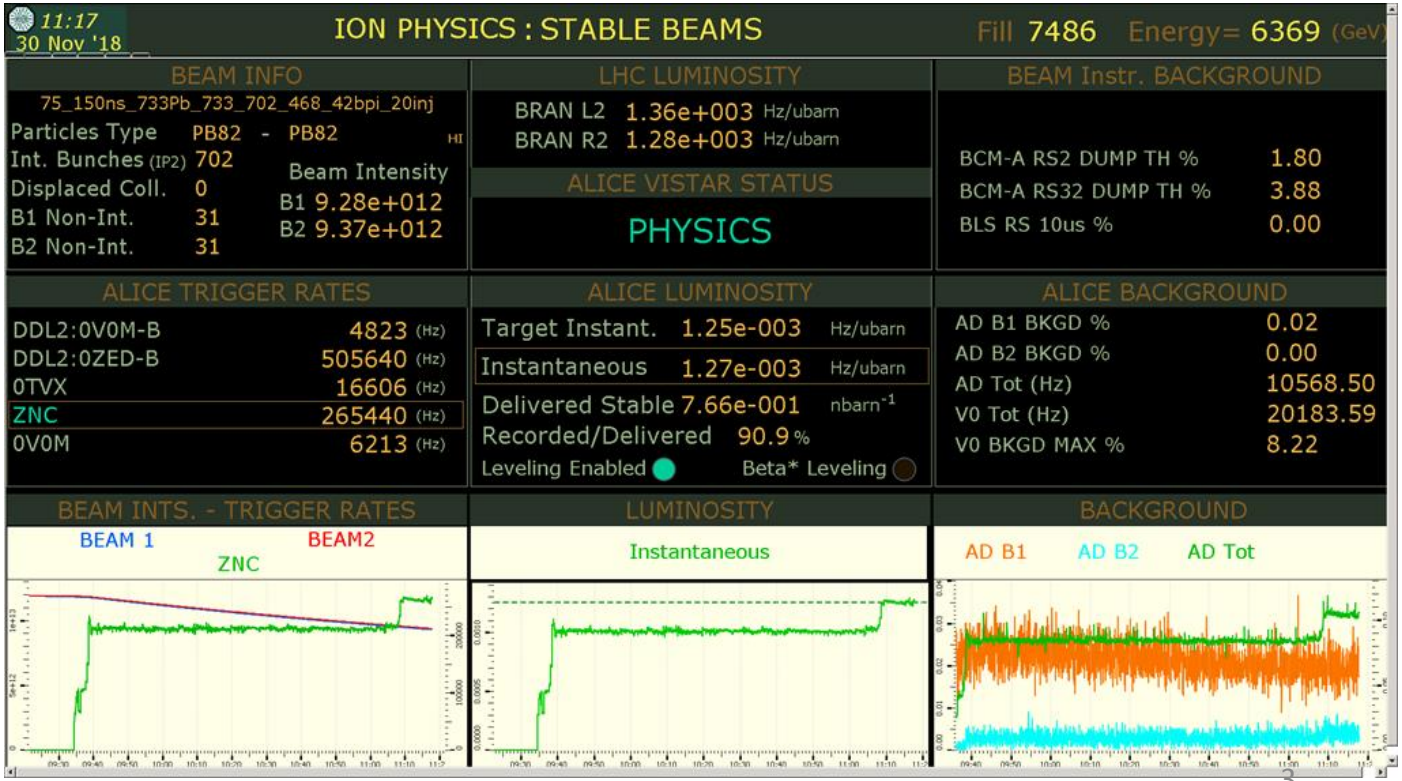
The TDC informations coming from the ZDC are used in physics selection to remove satellite collisions.

ZNC as luminomiter

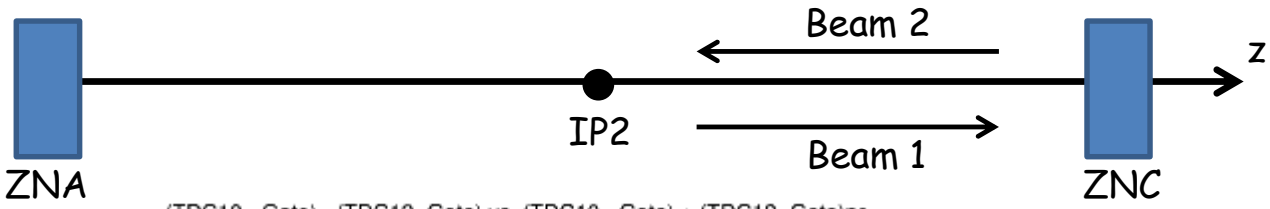
Absolute luminosity

$Rate_{ZNC}$ is given by EMD plus hadronic interactions.

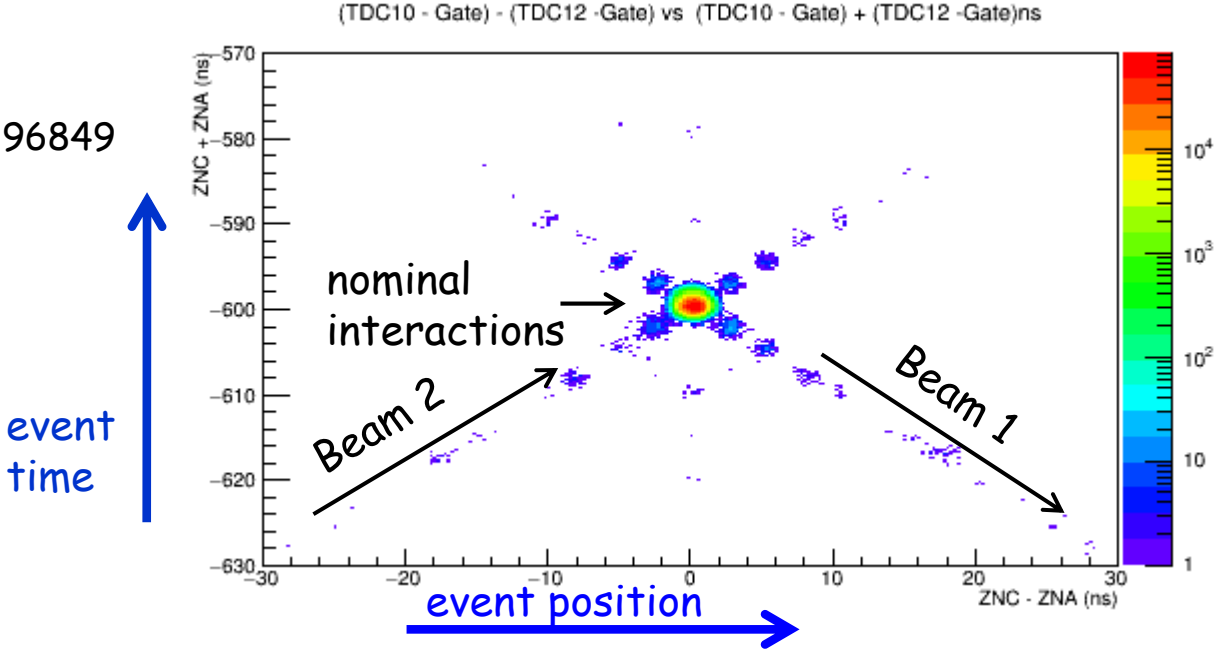
$L \sim Rate_{ZNC}/213$ b (RELDIS prediction)



Sum vs Difference of times recorded by the 2 ZNs



Run 296849



ZNs identify displaced collisions.

Large cluster -> collisions between ions in the nominal RF buckets of each beam
Small clusters -> collisions in which one of the ions is displaced by one or more RF buckets.

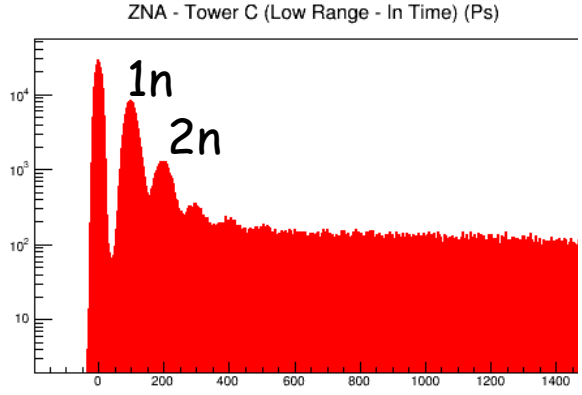
EMD measurement

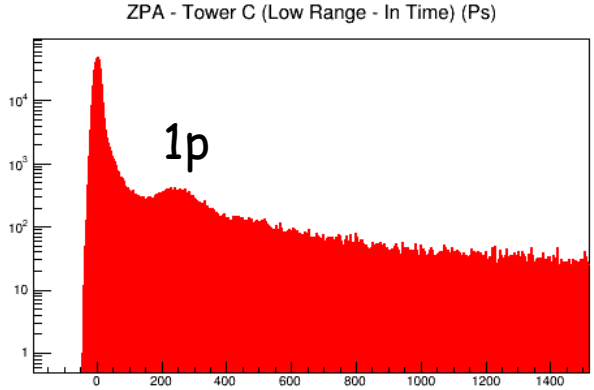
Physics_1 297328, 297331
At low lumi (0,2 Hz/b/bunch)

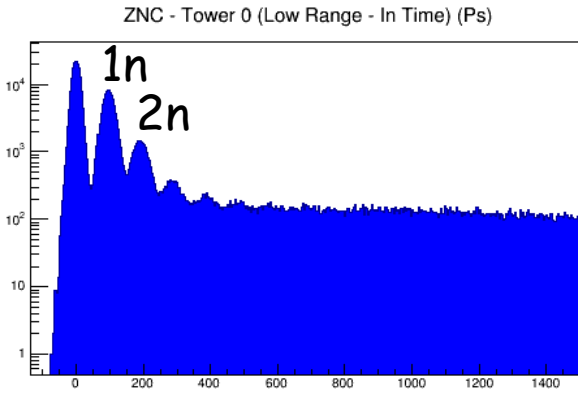
Readout detectors:
ZDC, V0, SPD

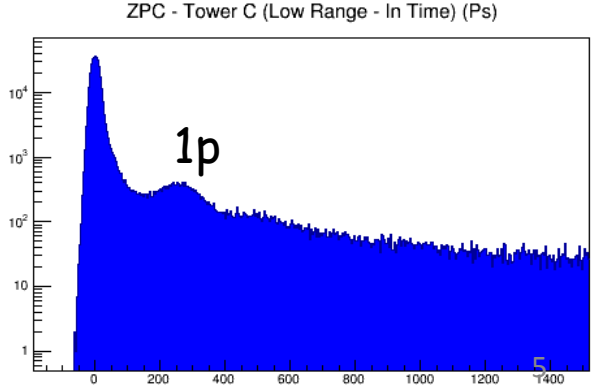
Trigger:
1ZED (ZNA or ZNC)
1ZPP (ZPA or ZPC)

~ 2 10^6 1ZED and
~ 0,5 10^6 1ZPP
events recorded









Attivita' ZDC 2019-2020

- Manutenzione ordinaria e straordinaria delle piattaforme ZDC (problemi con motore piattaforma ZPC)
- Smontaggio dal mainfraime antistante le porte di L3 del calorimetro elettromagnetico ZEM

- Rinnovo dell'elettronica di controllo delle piattaforme dei calorimetri adronici e il loro successivo commissioning movimentando le piattaforme
- Sostituzione dei PMT comuni dei due calorimetri per neutroni e dei due calorimetri per protoni posti nel tunnel concordando con LHC il periodo esatto
- Rinnovo dei due patch panel in vetronite per interfaccia HV dei calorimetri adronici nel tunnel e preparazione di un patch panel per i segnali e cavi HV dello ZEM
- Rimontaggio e allineamento nel nuovo mainframe antistante le porte di L3 del calorimetro elettromagnetico ZEM

Richieste ZDC 2020

M&OB ZDC 2020
13 KCHF -> 11,5 KE

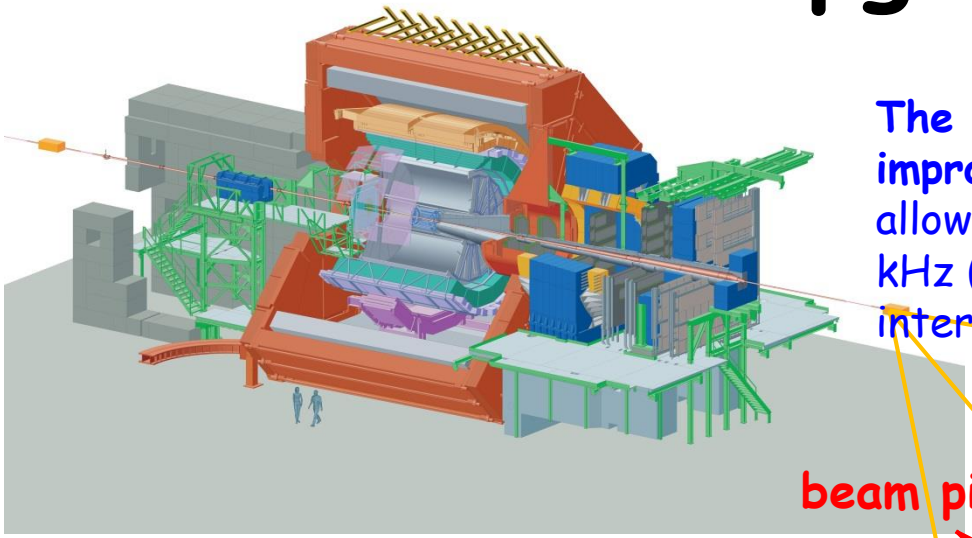
Missioni estere
Richiesta ZDC 2020
3 KE per sostituzione patch pannels ZNs, ZPs, ZEM e riposizionamento cavi HVs;
1 KE per rimontaggio e allineamento nel mainframe del calorimetro ZEM;

Consumo
Richiesta ZDC 2020
4 KE Connettori e cavi HV per rifacimento patch panels ZNs, ZPs e ZEM;

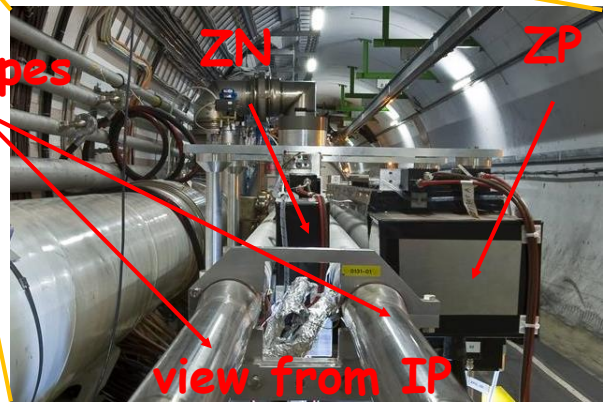
M&OB ZDC (KCHF)

Ref.	Description	2020	2021	2022	2023
A01	Mechanics		1	1	1
A02	Gas Systems				
A03	Cooling Systems				
A04	FEE spares		2	2	2
A05.1	Standard Electronics LV/HV PS				
A05.2	Standard Electronics Crates				
A05.3	Standard Electronics R/O modules		2	2	2
A06	Controls (DCS & DSS)				
A07	Sub-Detector spares				
A08	Areas				
A09	Communications	**1**	1	1	1
A10	Store Items	2	2	2	2
A11.1	Technical Manpower @ CERN: Industrial Support				
A11.3	Technical Manpower @ CERN from Collaborating Institutes	**10**	8	8	8
Total		13	16	16	16

ZDC upgrade



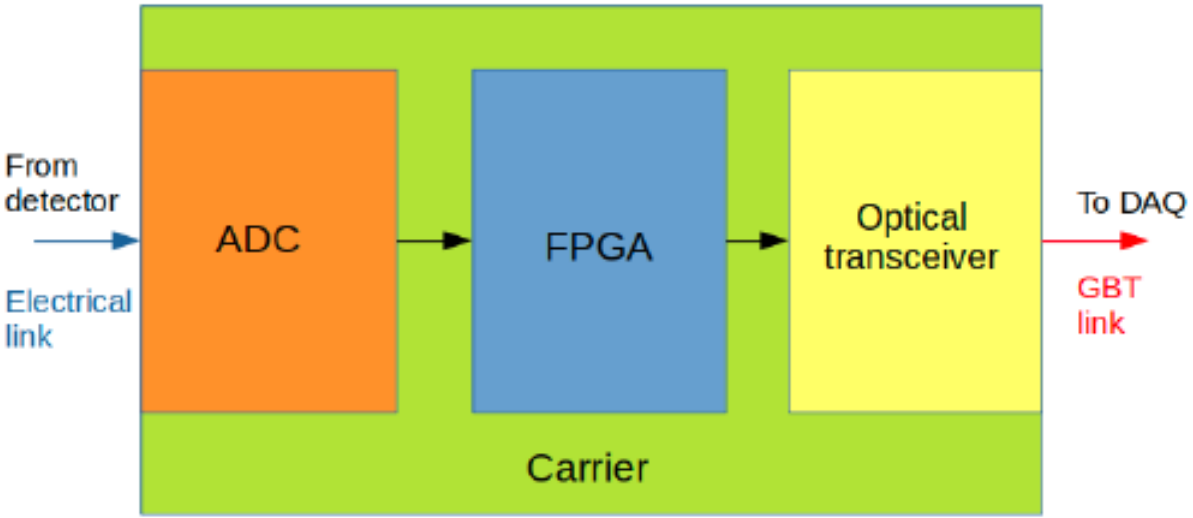
The main target of ZDC upgrade is the improvement of the readout performance, allowing to read out the detector at 100 kHz (safety factor of 2) of PbPb hadronic interactions without dead time.



The continuous readout mode without dead time is very challenging for the ZDC

The design readout rate in Pb-Pb collisions of ~100 kHz of hadronic interactions on detectors on both sides means for ZDC additional 2.6 MHz on one side and 2.6 MHz uncorrelated on the opposite side of e.m. interactions (not seen from ALICE barrel).

ZDC new readout architecture

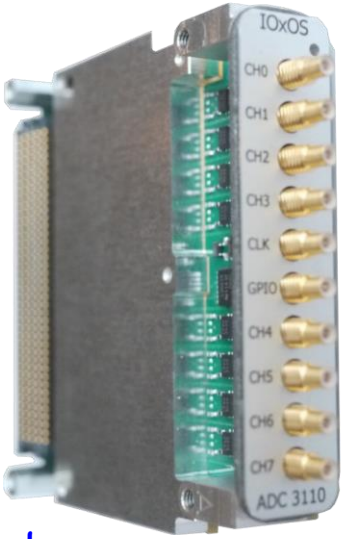


- **Data from detector are sampled with a 12 bits, 1 GS/s FMC digitizer** -> high bandwith to FPGA
- FPGA: reduce the data flow to DAQ (data compression and waveform analysis)
  - trigger processing or autotrigger
  - timing and signal integration
  - data transmission over Gigabit Transceiver (GBT): 4,8 Gb/s per link.

Final FMC digitizer and Carrier

IOxOS ADC 3112

- 4 channels, 12 bit
- ~1 GSps
- input coupling: **true DC**
- LVDS parallel interface



FMC carrier

- First integration performed in Torino lab. with a Virtex6 evaluation board in order to test the ADC performance

- Final carrier: **IOxOS IFC_1211 VME board**

Attivita' upgrade 2018-2019

- Implementazione del firmware del digitalizzatore IOxOS ADC_3112 (DC input) su Virtex 6 board
- Studio delle performance in laboratorio del ADC_3112 presentate al EDR meeting a Giugno e Luglio 2018 al Cern.
- A Novembre fatto studio delle performance del ADC_31112 al Cern durante le collisioni Pb-Pb, usando due acquisizioni parallele
  - ADC_3112 letto attraverso evaluation board e carrier IOxOS (IFC_1210 board).
  - Identificata configurazione del chip ADC (hardware down-sampling by a factor 2 with low-pass filtering).
- Implementazione del link GBT tramite due evaluation boards di test e attivita' relativa al recovery e alla distribuzione del clock.

Ancora da fare nel 2019:

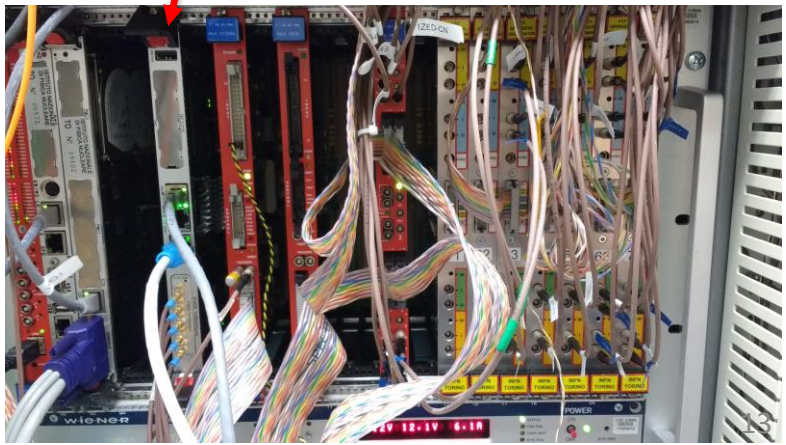
- Implementazione nel FPGA del carrier IOxOS dell'algoritmo di autotrigger e del link GBT
- IOxOS -> codice vhdl riguardante la parte di readout piu' legata all'hardware

ZDC upgrade

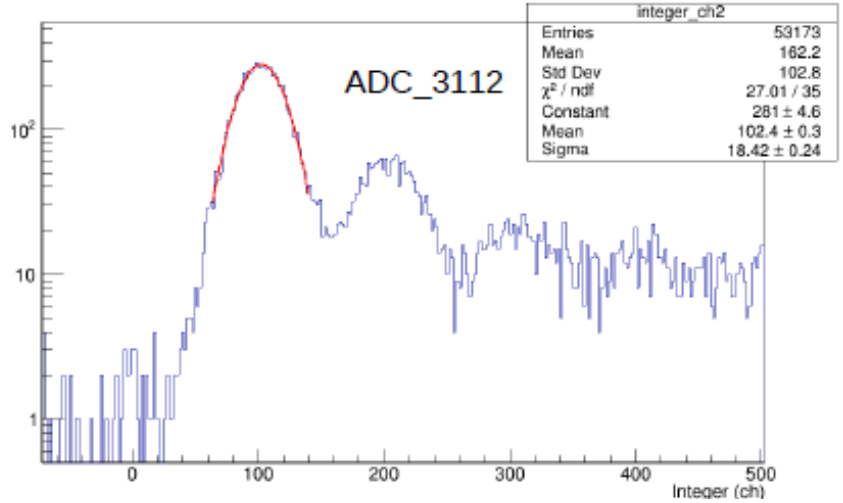
Test of the performance of the upgrade electronics during the Pb-Pb run with 2 parallel acquisitions: 4 ZDC signals acquired (external trigger L0)

Evaluation board Virtex 6 (ML605) +
FMC IOxOS ADC_3112

VME board IFC_1210 IOxOS plugged in ZDC electronics +
FMC IOxOS ADC_3112

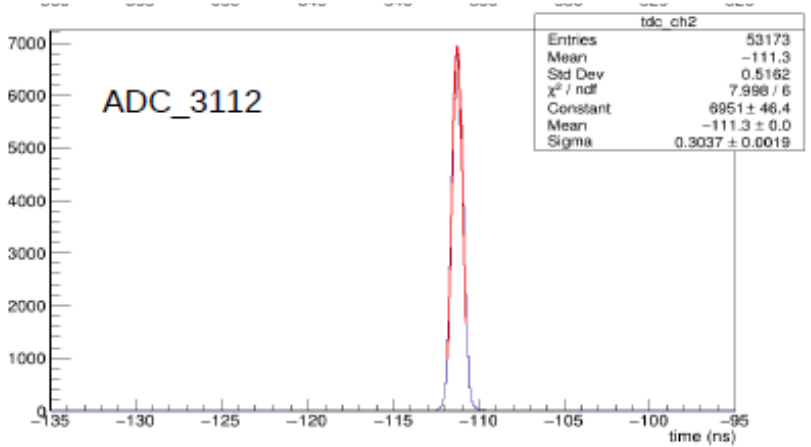


ZDC upgrade performance



1n peak resolution : ~18%
better w.r.t. current electronics

time resolution ~0,30 ns
comparable to the
current electronics



Attivita' upgrade nel 2020

Una volta terminato lo sviluppo del firmware le attivita' previste nel 2020 sono le seguenti:

Prove in laboratorio del sistema di acquisizione e trasferimento dati via GBT link per 1 FMC+Carrier in modalita' autotrigger fino alla CRU con clock dato dalla LTU

Prove in laboratorio delle 8 coppie FMC+Carrier.

Integrazione del sistema di configurazione dell'elettronica in ALICE

Installazione e inizio commissioning del sistema di acquisizione al Cern.

Milestones

Milestones Concordate 2019

30/6/2019 Definizione dell'architettura della configurazione dell'elettronica a inizio run: 20%

31/12/2019 Implementazione del sistema di acquisizione e trasferimento dati via GBT link per un FMC in modalita' autotrigger: 20%

Milestones Proposte 2020

30/9/2020 Prove in laboratorio delle 8 coppie FMC+Carrier

31/12/2020 Installazione e inizio commissioning del sistema di acquisizione al Cern

Richieste upgrade ZDC Apparati

Profilo temporale (KE)

Apparato	2014	2015	2016	2017	2018	2019	2020	Tot(KE)	FMC+Carrier
ZDC	19	0	0	16	18,5	**100**		153,5	IOxOS

MoU(opzione "triggered mode") -> 163 KCHF.

Upgrade ZDC 2019-> richiesto a Giugno sblocco di **68 kE s.j.** per acquisto di
8+1 carriers IOxOS (**57,5 KE**) +
8+2 FMC SFP (link ottico, **8,5 KE**) +
30 transceivers ottici (**2 KE**)

Richieste upgrade ZDC 2020

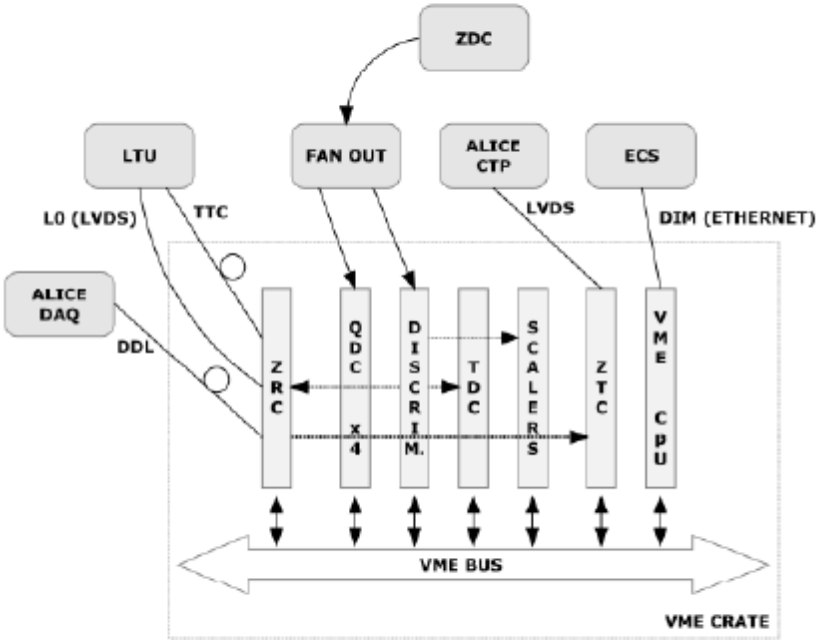
Missioni estere -> **Richiesta upgrade ZDC 2020**

4 KE per contatti con esperti per commissioning del link GBT-CRU-LTU
4 KE per contatti con ditta IOxOS
8 KE per test nuova elettronica di readout in CR4

BACKUP

Current DAQ system

The current DAQ system is:



- CAEN V965 QDCs (12 bit)
- CAEN V1290 TDCs
- CAEN V830 SCALERs (32 bit)
- Custom Differential Discriminators (precise triggering)
- NIM modules
- Custom Trigger Card (ZTC)
- Custom Readout Card (ZRC)

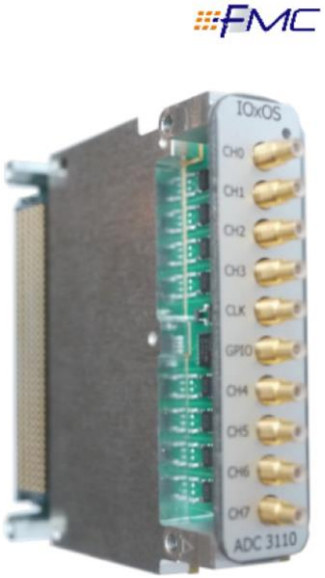
The present acquisition system is able to sustain a L2a rate of ~11KHz in the ZDC limited by

V965 QDCs conversion time of 10 μs → L0 of 100 kHz
VME transfer rate from V965 (D32 with BLT) → L2a of 11 KHz

10

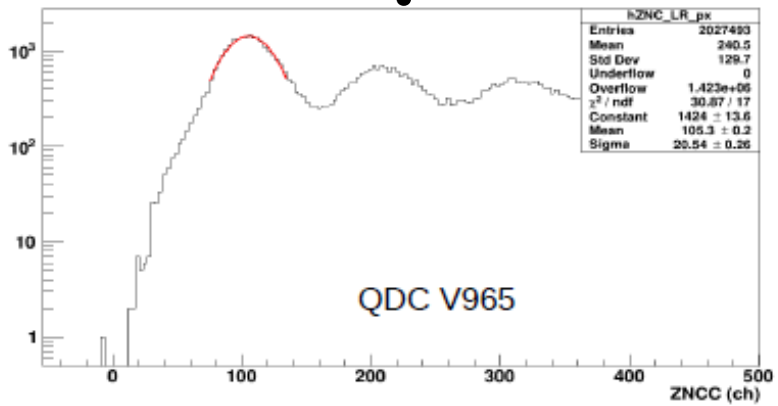
ZDC – Upgrade
FMC: IOXOS ADC_3112

Equipped with two ADCs ADS5409, 12 bit, 900(1000) MSps



	ADC_3112
sample rate (MSps)	900 (1000)
resolution depth (b)	12
module price (KCHF)	5
channel number	4
input coupling	DC
input voltage (Vpp)	500 mV
enob ~1GHz (b)	9,8

1n peak resolution

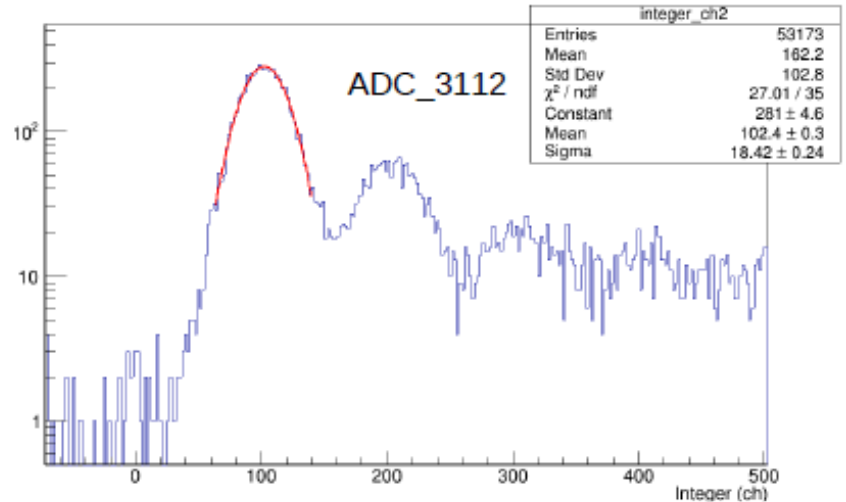


QDC V965:

- Integration of the signal over 68 ns

$$R = \frac{20,54}{105,3} = (19,51 \pm 0,01)\,\%$$

current electronics



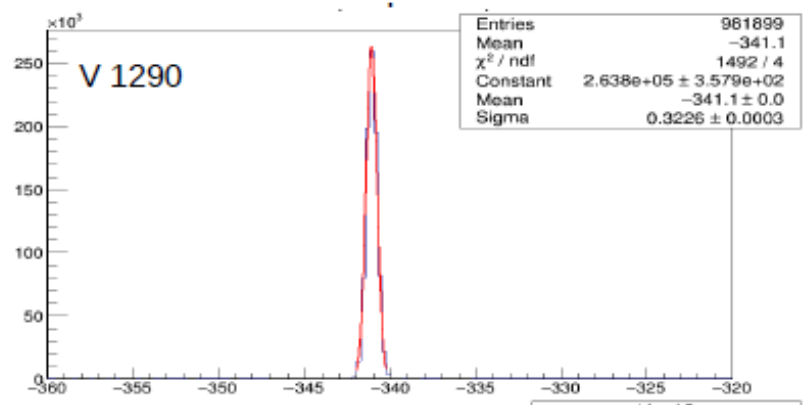
ADC_3112:

- Integration of the signal over 25 ns (duration of every bunch crossing at LHC) starting 5 ns before signal maximum

$$R = \frac{18,42}{102,4} = (17,99 \pm 0,01)\,\%$$

new electronics

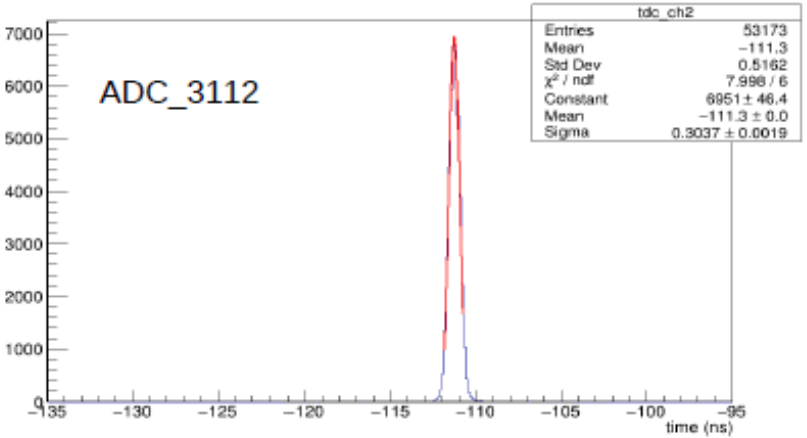
Time resolution



TDC V 1290

$R = \sigma = (0{,}3226 \pm 0{,}0003)\,ns$

current electronics



ADC_3112

$R = \sigma = (0{,}304 \pm 0{,}002)\,ns$

new electronics