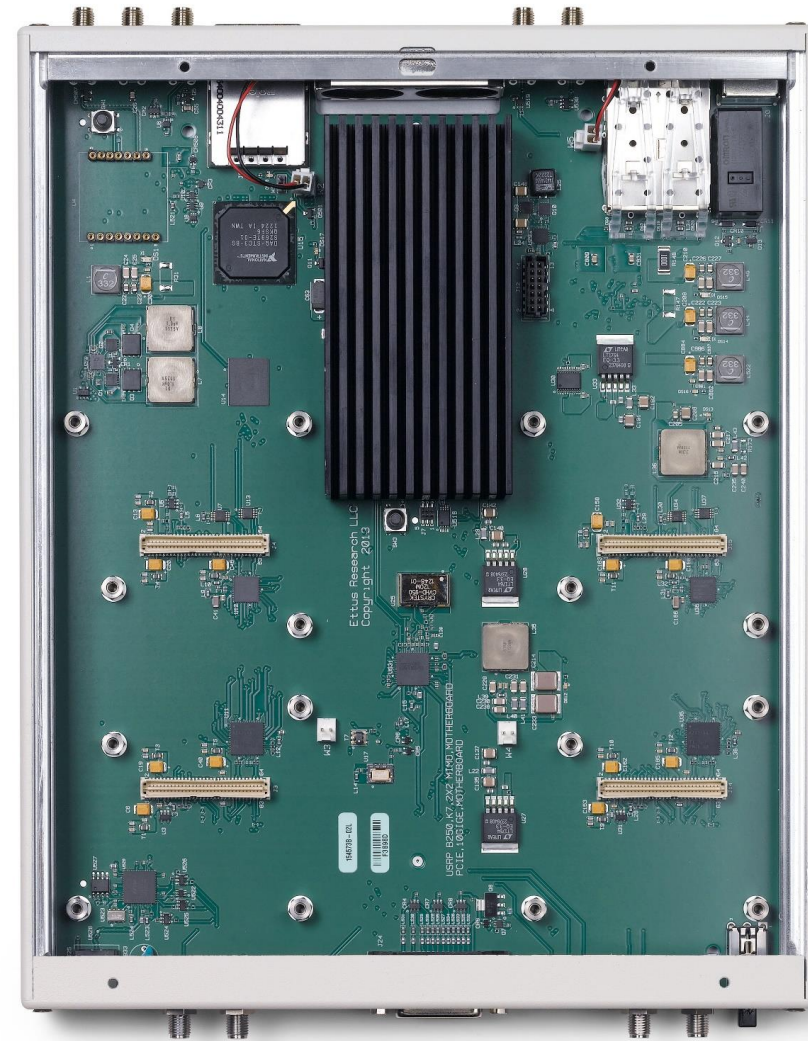


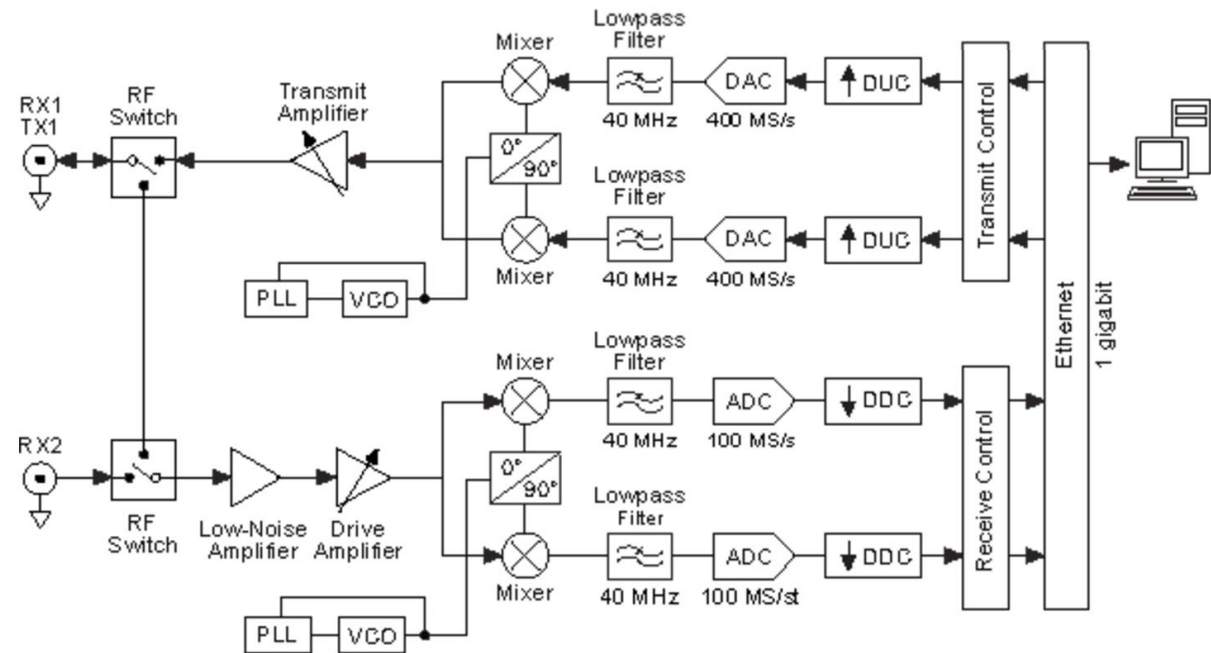
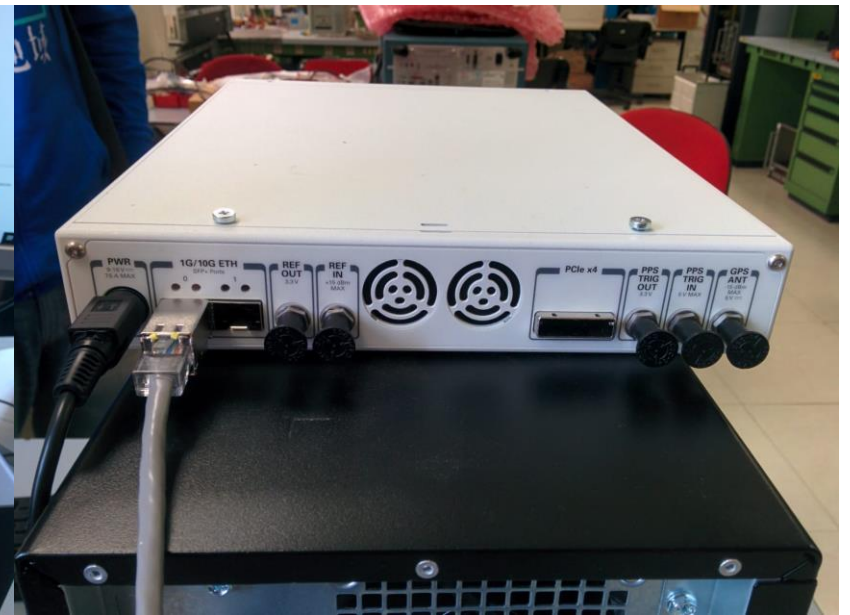


# USRP X310

high-performance, scalable  
software defined radio



# Setup sperimentale



# Istallazione

- Microsoft Windows (7, 8, 8.1, 10)
- UHD library
- GNU Radio opensource software
- Microsoft Visual Studio (2013, 2015, 2017)
- CMake (2.8.0 or later)
- Boost (1.53 or later)
- LibUSB (1.0 or later)
- Python (2.7.x)
- Mako (0.5.0 or later)
- Doxygen (1.8 or later, optional)
- NSIS (2.50 or later, optional)
- 7zip (<http://www.7-zip.org/download.html>)
- msysGit (<https://gitforwindows.org/>)

# Bulding

- Compilato UHD con Open Visual Studio 2017 and open the UHD project file generated by CMake.
- Scaricato firmware FPGA e caricato sull'hardware (non grazie alla rete Ethernet del lab)



# Comunicazione driver

- Ping
- uhd\_find\_device -> la libreria usb funziona
- uhd\_ursp\_probe -> siamo in grado di creare piccoli programmi e lancialli tramite python da terminale

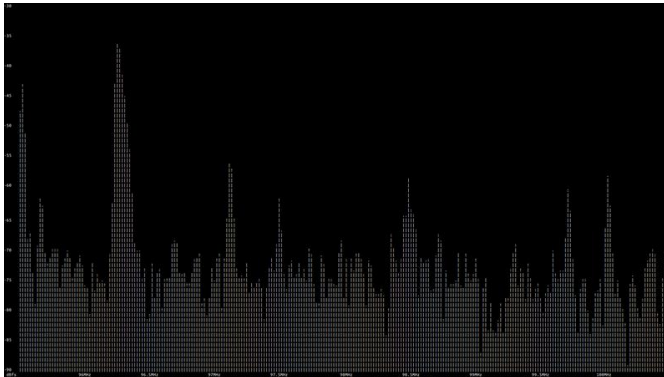
```
Prompt dei comandi
Microsoft Windows [Versione 10.0.17763.903]
(c) 2018 Microsoft Corporation. Tutti i diritti sono riservati.

C:\Users\F.Iacoangeli>ping 192.168.10.2

Esecuzione di Ping 192.168.10.2 con 32 byte di dati:
Risposta da 192.168.10.2: byte=32 durata=1ms TTL=32
Risposta da 192.168.10.2: byte=32 durata=1ms TTL=32
Risposta da 192.168.10.2: byte=32 durata=1ms TTL=32
Risposta da 192.168.10.2: byte=32 durata=1ms TTL=32

Statistiche Ping per 192.168.10.2:
    Pacchetti: Trasmessi = 4, Ricevuti = 4,
    Persi = 0 (0% persi),
    Tempo approssimativo percorsi andata/ritorno in millisecondi:
        Minimo = 0ms, Massimo = 1ms, Medio = 0ms

C:\Users\F.Iacoangeli>
```



```
Device: X-Series Device

Board: X310
revisions: 11
revision_compat: 7
product: 30018
mac-addr0: 00:00:2f:22:f4:44
mac-addr1: 00:00:2f:22:f4:45
gateway: 192.168.10.1
ip-addr0: 192.168.10.2
subnet0: 255.255.255.0
ip-addr1: 192.168.20.2
subnet1: 255.255.255.0
ip-addr2: 192.168.30.2
subnet2: 255.255.255.0
ip-addr3: 192.168.40.2
subnet3: 255.255.255.0
serial: 3176080
FW Version: 6.0
FPGA Version: 35.1
FPGA git hash: 4c165as
RFNOC capable: Yes

Time sources: internal, external, gpsdo
Clock sources: internal, external, gpsdo
Sensors: ref_locked

RX Dboard: A
ID: LF RX (00000f)
Serial: 315F3A0

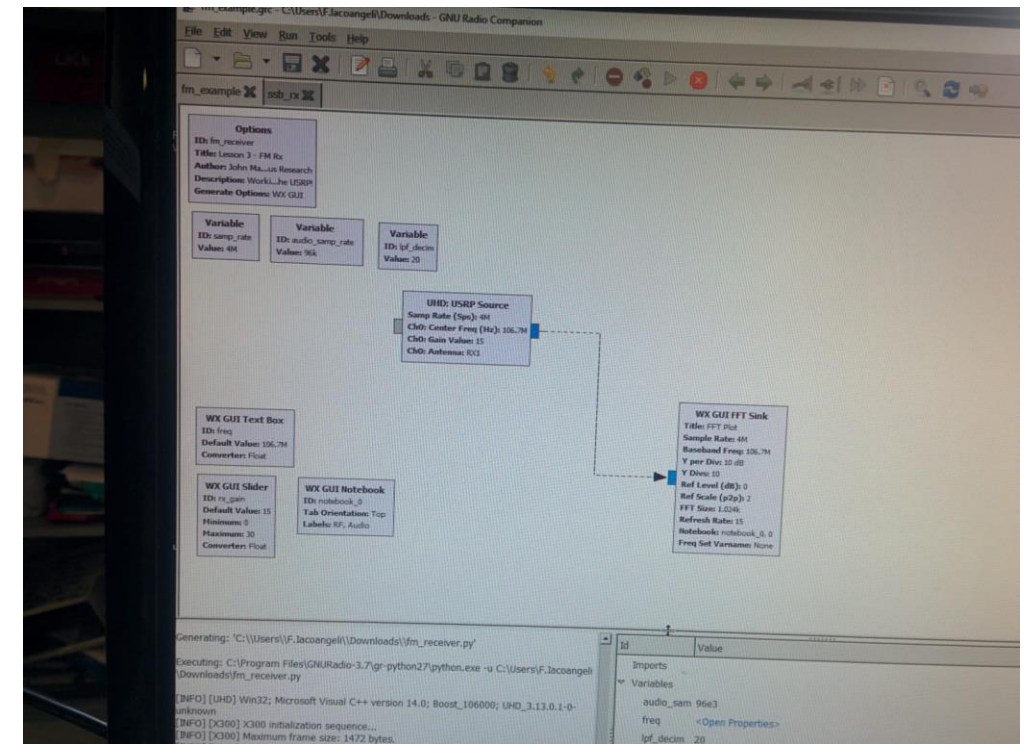
RX Frontend: AB
Name: LFRX (AB)
Antennas: AB, BA, A, B
Sensors:
Freq range: -32.000 to 32.000 MHz
Gain Elements: None
Bandwidth range: 64000000.0 to 64000000.0 step 0.0 Hz
Connection Type: IQ
Uses LO offset: No

RX Frontend: BA
Name: LFRX (BA)
Antennas: AB, BA, A, B
Sensors:
Freq range: -32.000 to 32.000 MHz
Gain Elements: None
Bandwidth range: 64000000.0 to 64000000.0 step 0.0 Hz
Connection Type: IQ
Uses LO offset: No

RX Frontend: A
Name: LFRX (A)
Antennas: AB, BA, A, B
Sensors:
Freq range: -32.000 to 32.000 MHz
Gain Elements: None
```

# Gnu Radio

- Abbiamo installato GNU Radio, programma opensource per elaborare il segnale con un linguaggio visuale a blocchi
- Attualmente ancora non riesce a comunicare bene con USRP x310 per un problema di upgrade tra firmware dell'FPGA e versione driver di
- Probabile soluzione con l'upgrade UHD or downgrade the FPGA image



```
[INFO] [X300] Radio 1X CLOCK: 200 MHz
[INFO] [0/DmaFIFO_0] Initializing block control (NOC ID: 0xF1F0D00000000000)
[ERROR] [0/DmaFIFO_0] Major compat number mismatch for noc_shell: Expecting 2, got 5.
Traceback (most recent call last):
  File "C:\Users\F.Iacoangeli\Downloads\fm_receiver.py", line 173, in <module>
    main()
  File "C:\Users\F.Iacoangeli\Downloads\fm_receiver.py", line 167, in main
    tb = top_block_cls()
  File "C:\Users\F.Iacoangeli\Downloads\fm_receiver.py", line 110, in __init__
    channels=range(1),
  File "C:\Program Files\GNURadio-3.7\lib\site-packages\gnuradio\uhd\__init__.py", line 122,
in constructor_interceptor
    return old_constructor(*args)
  File "C:\Program Files\GNURadio-3.7\lib\site-packages\gnuradio\uhd\uhd_swig.py", line
2783, in make
    return _uhd_swig.usrp_source_make(*args)
RuntimeError: RuntimeError: FPGA component `noc_shell' is revision 5 and UHD supports
revision 2. Please either upgrade UHD (recommended) or downgrade the FPGA image.
```