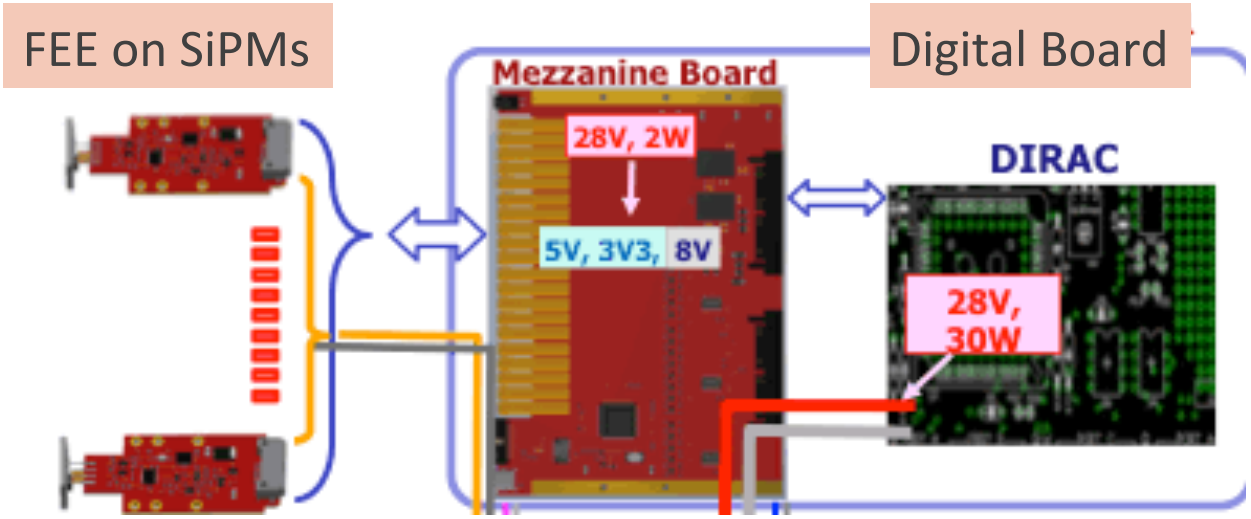
Status of electronics: FEE/MB/DIRAC

- 1 FEE /SiPM
  20 FEE/MB+DIRAC board
- 2017 Test beam done with FEE-V1 + CAEN digitizer
- 2017-2018 spent to make rad-hard FEE and rad-hard DIRAC



- **For the CRR mechanics, and this meeting, we did not go through a full discussion of the electronics but we are planning next a PCB/CRR and a dedicated presentation**

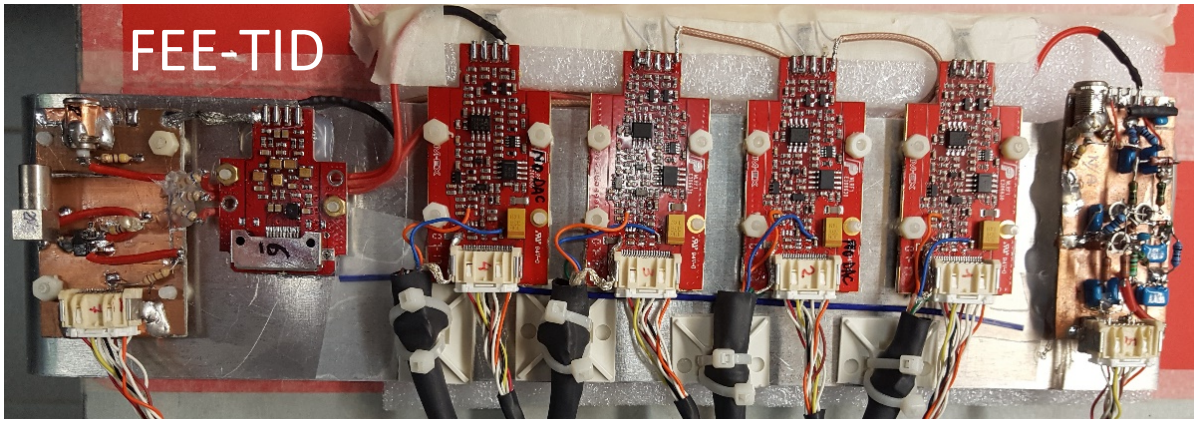
However we have completed the following tests/decisions:

→ size and position of electronics on calorimeter model
→ all mech. Interferences of boards in crate , solved and tested
→ tests of single component prototypes in rad-environment
→ cable type selection, cable length and determined their routing path
→ stable estimate of power dissipation and cooling needs

Development of RAD-Hard electronics

Long irradiation campaign carried out:

- ➔ Neutrons in FNG(Italy) HZDR(Germany)
- ➔ Dose in Calliope (Italy)
- ➔ SEU in Warrenville (USA)



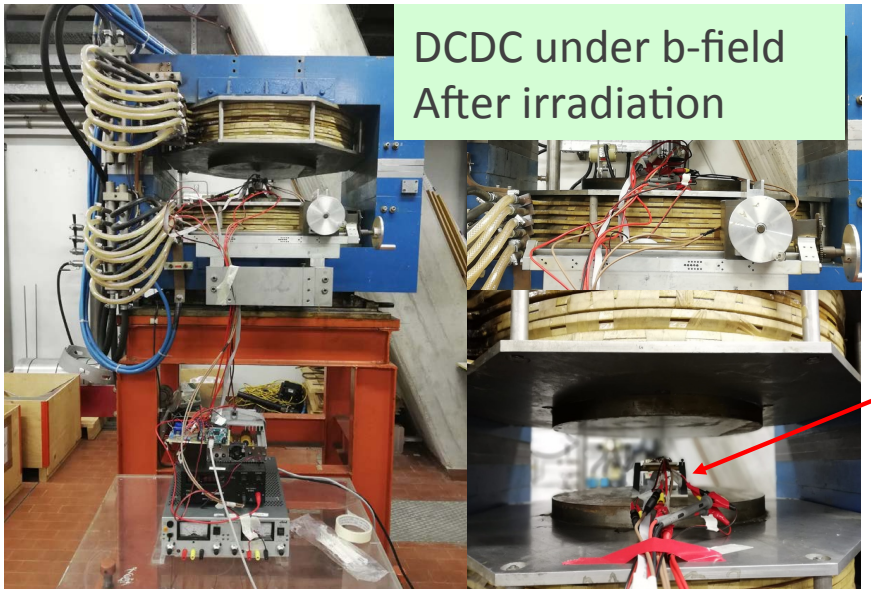
Results:

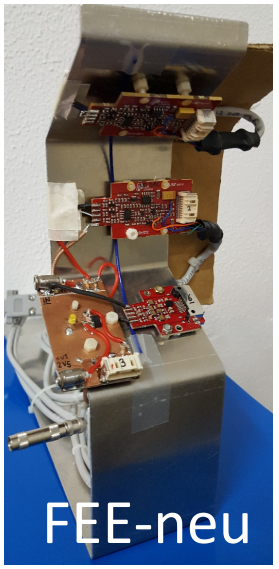
1) Final rad-hard components selected
2) FEE v3 OK
3) DC-DC converter OK

4) FPGA/ADC/DDR sections of DIRAC tested

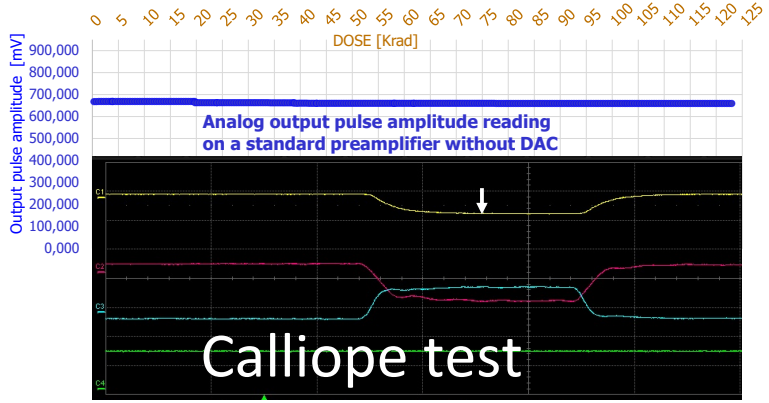
→ SEU test almost completed

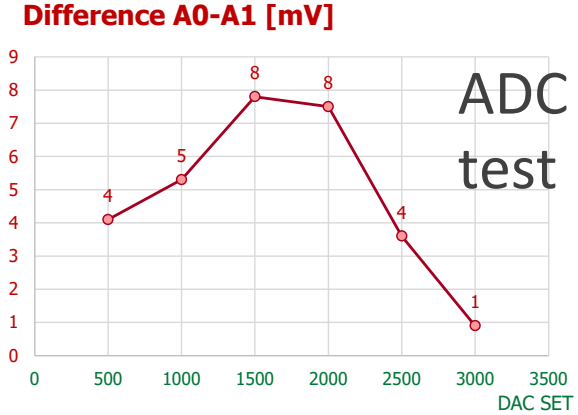
→ Dirac V2 design almost completed



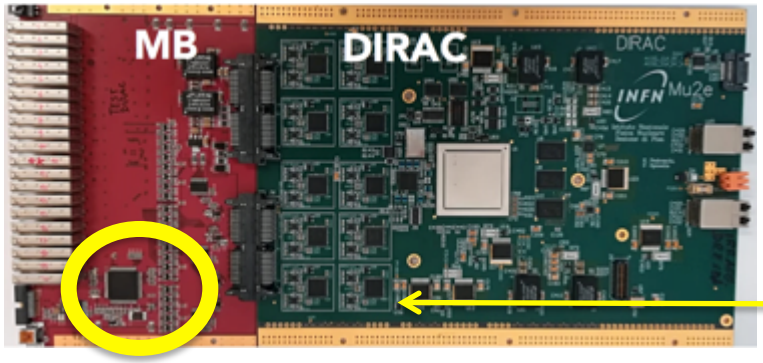


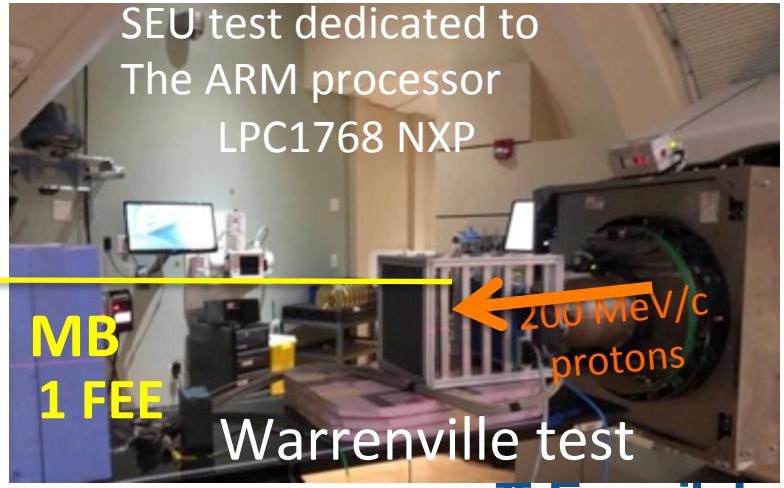
Electronics: FEE test up to 120 krad





- All analog parts of Amplifier and HV regulator now OK after changing Voltage reference chip
- LT ADC/DAC of digital parts suffering from 10-15 krad
- New rad-hard ADC/DAC identified from Texas Instrument
- PCB with new TI ADC/DAC done 28 January, OK ➔ new protocol required 6 pairs/wire, new cable





Few SEU observed up to $1.5E^{10}$ p/cm^2 due to Ethernet connection. Repeat with final MB

Vertical slice test (N. 3)

- First vertical slice test (w.o. DIRAC) in May 2017, Module-0
- Second vertical slice test Amp V1 w DIRAC V1 in Sep. 2018
- Third vertical slice test with Amp V2, MB V2 and Dirac V1, May 2019

Readout of 4 channels at low rate with LED and CR data taking.

→ Good comparison of shapes DIRAC vs CAEN digitizer

→ Data analysis in progress

→ Next step is readout of 20 channels in Module-0

- Next/last vertical slice test w DIRAC will need DIRAC V2 and TDAQ readout
- Discussion in progress to see if a new Test beam is needed