Data Readout for AGATA using Future Electronics (STARE) Hardware and Firmware

AGATA

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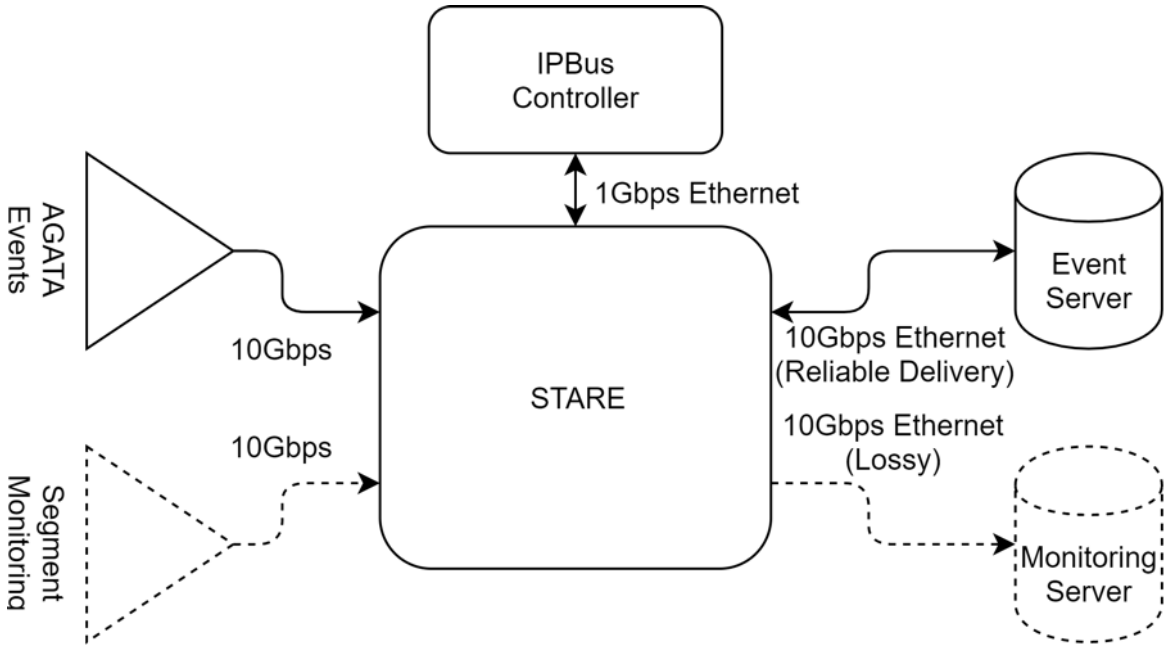
X. Lafay, **N. Karkour**, D. Linget and **G. Vinther-Jørgensen**

IFIC/MILANO/CSNSM/IPHC Collaboration

The STARE Concept

- Decoupling the custom hardware from the server farm
- Input through FMC
  - 4 Transceivers
  - 20 LVDS Pairs
- Ethernet output
  - 4 SFP+ links
  - UDP Transport
- IPBus slow control



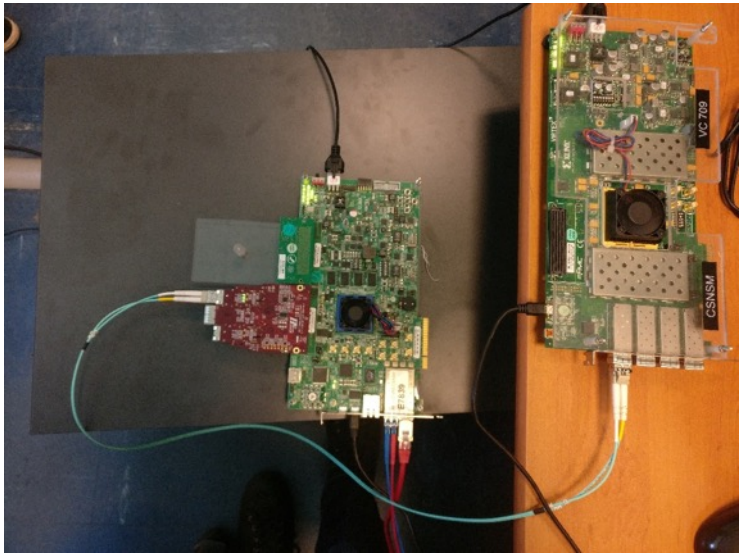
Current firmware functionality

Recent firmware developments

- Status in February 2019
  - The parts where there
    (IPBus and 10 Gbps Network Stack)
  - Conflicts between the IPBus and the Network Stack
  - Unnecessary features
  - Obsolete hardware
- Progress
  - Removed TCP implementation from the Network Stack
    - External memory
  - Ported the Network Stack from Virtex 7 to Kintex Ultrascale
  - Merged the IPBus and Network Stack projects
  - Tested protocols for data input
  - Managed to transfer custom data from the Kintex Ultrascale to server via Ethernet

Current Firmware Status

- Working prototype on KCU105 with VC709 as data generator.
  - Based on code provided by David Sidler (ETH Zurich) and IPBus firmware from CERN
  - Event splicing/reconstruction
  - UDP transmission
  - Package loss
  - IPBus implemented
  - Successfully tested with pre-processing prototype from University of Valencia
- Simple server application checking data integrity



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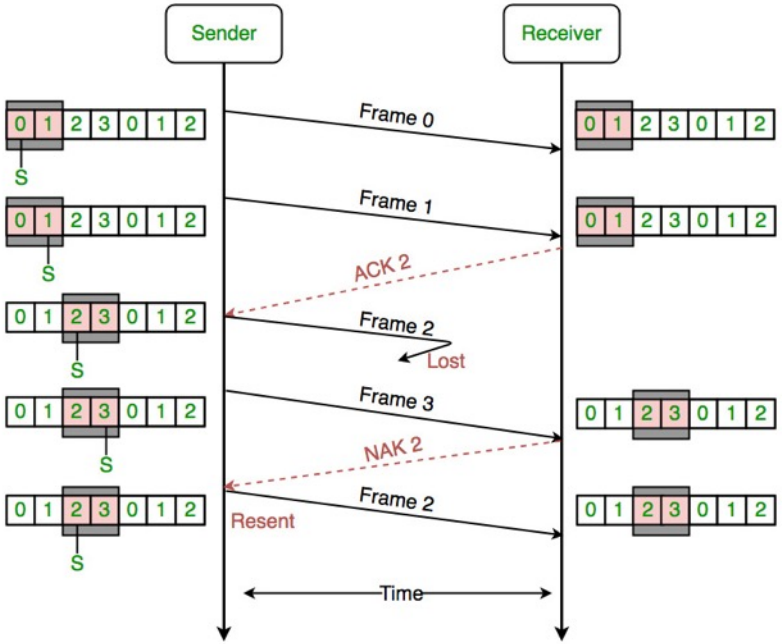
Next Steps

- Ensuring data reaches the server
  - Overlaying protocol is needed to guarantee delivery
  - Needs external memory on the KCU105 board
- Improving usability
  - Using the features of IPBus
  - Documentation
- Testing
  - Improved server side program
  - More complex network structure



https://www.geeksforgeeks.org/sliding-window-protocol-set-3-selective-repeat/

STARE HARDWARE

- **What has been done:**

- Bought a VC709 Xilinx evaluation board to qualify the initial code.

- Interface the evaluation board with the CSNSM 10 Gbps network data flow and validate the UDP for AGATA DAQ.

- Bought a KCU105 Xilinx evaluation board to simulate the pre-processing module.

- The firmware was initially tested with the VC709 evaluation board.

- During Firmware development issues and hardware constraints were discovered on the VC709 FPGA (old FPGA technology, less development library tools, less clock distribution facilities, no SOM modules in the market etc...).

- Since the KCU105 uses a recent KU040 FPGA (more flexibility in clock management, more development tools options, more high speed TX/RX, SOM modules are available etc…)

STARE HARDWARE

- **What was done (cont.):**

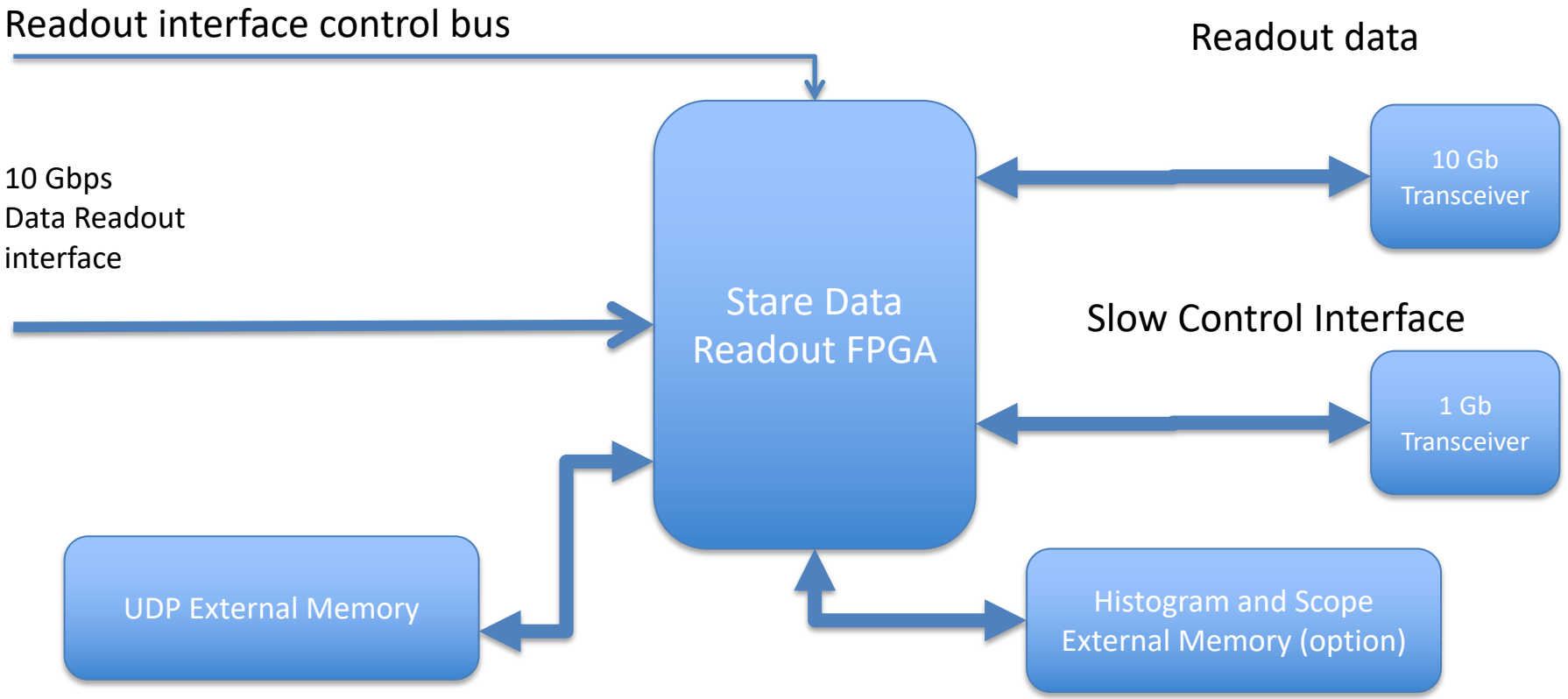
- A decision was taken to port the code from the VC709 to the KCU105.
- Done (see Gustav Presentation).
- The KCU105 became the STARE and the VC709 the pre-processing module simulator.
- As decided by the FEE WG, the future AGATA electronics will be based on the SOM technology plus dedicated carrier boards.
- STARE will be composed of a KU040 SOM module plus an FMC based dedicated carrier board.

- **What was needed: MANPOWER :**
  - **2018, 3 months engineering student Melissa: integration of the IPBUS interface on the VC709 and partial integration of the network stack code with IPBUS.**
  - **Feb 2019, 9 months student from Denmark (Gustav): (see his presentation)**
  - **June 2019, 3 months intern student (Nicolas): design, schematics and requirement documents. Component selection and tests for the STARE carrier board (validation of the Mux, DC-DC converter, Pinouts definition between SOM and the carrier). 3 Weeks Proof of Concept participation**
  - **starting September 2019: 3 years half time engineer student specialized in embedded electronics.**

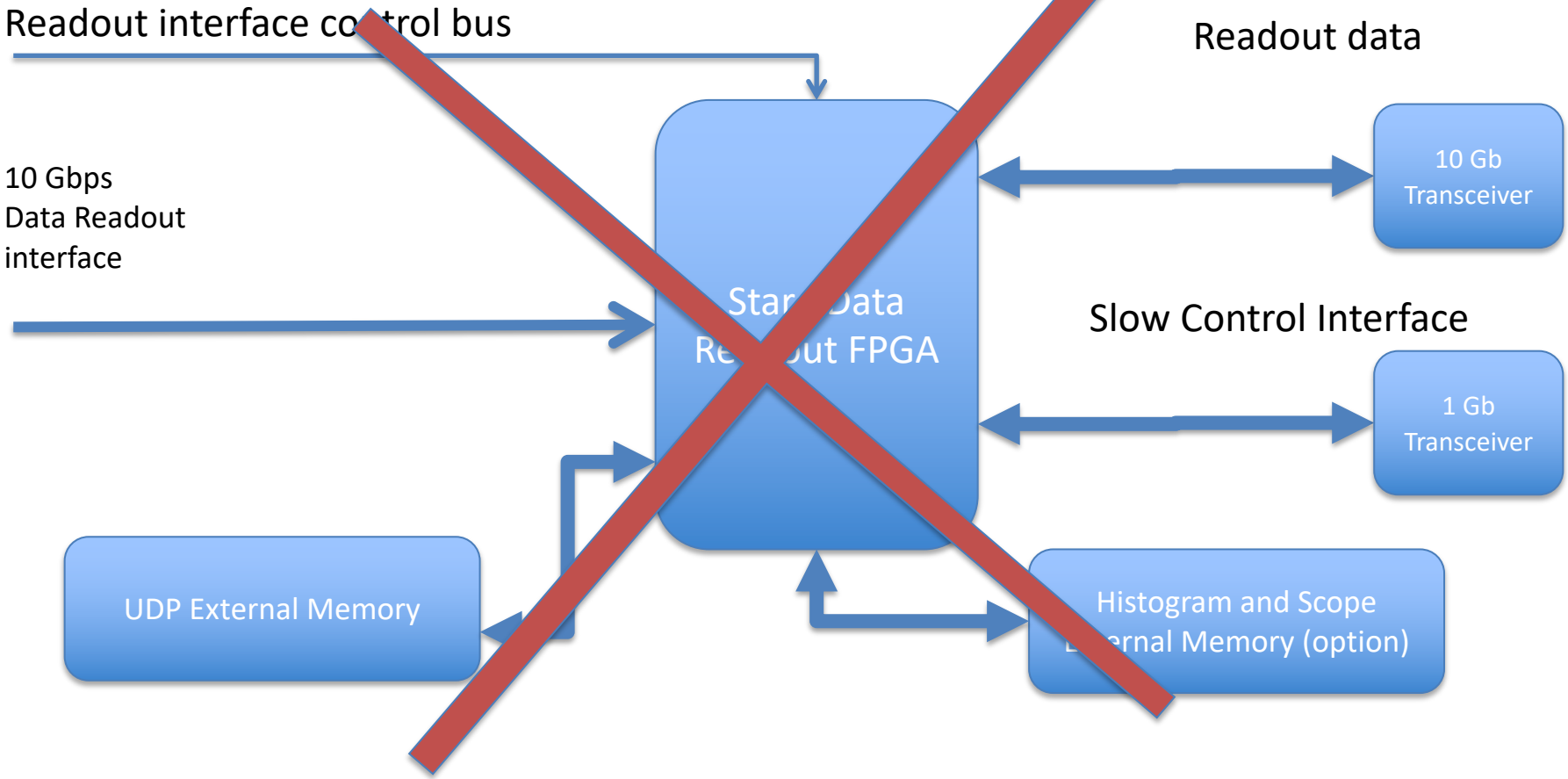
AGATA readout Requirements

- Network Band Width : 10 Gbps = 640 M words of 16 bits.
- Full FPGA online Monitoring (Chipscope on Ethernet)
- It is important to have spy eyes on all the data processing from Preamplifier to Data Flow
- But but but.
- After the first tests with the firmware 10 Gbps was not possible to achieve completely.
  - Any other activity on the server causes package loss.
- To achieve continuous and comfortable 10 Gbps with monitoring and online analysis, multiple 10 Gbps Tx/Rx is needed.
- New STARE architecture is under design.

STARE Initial Block Diagram



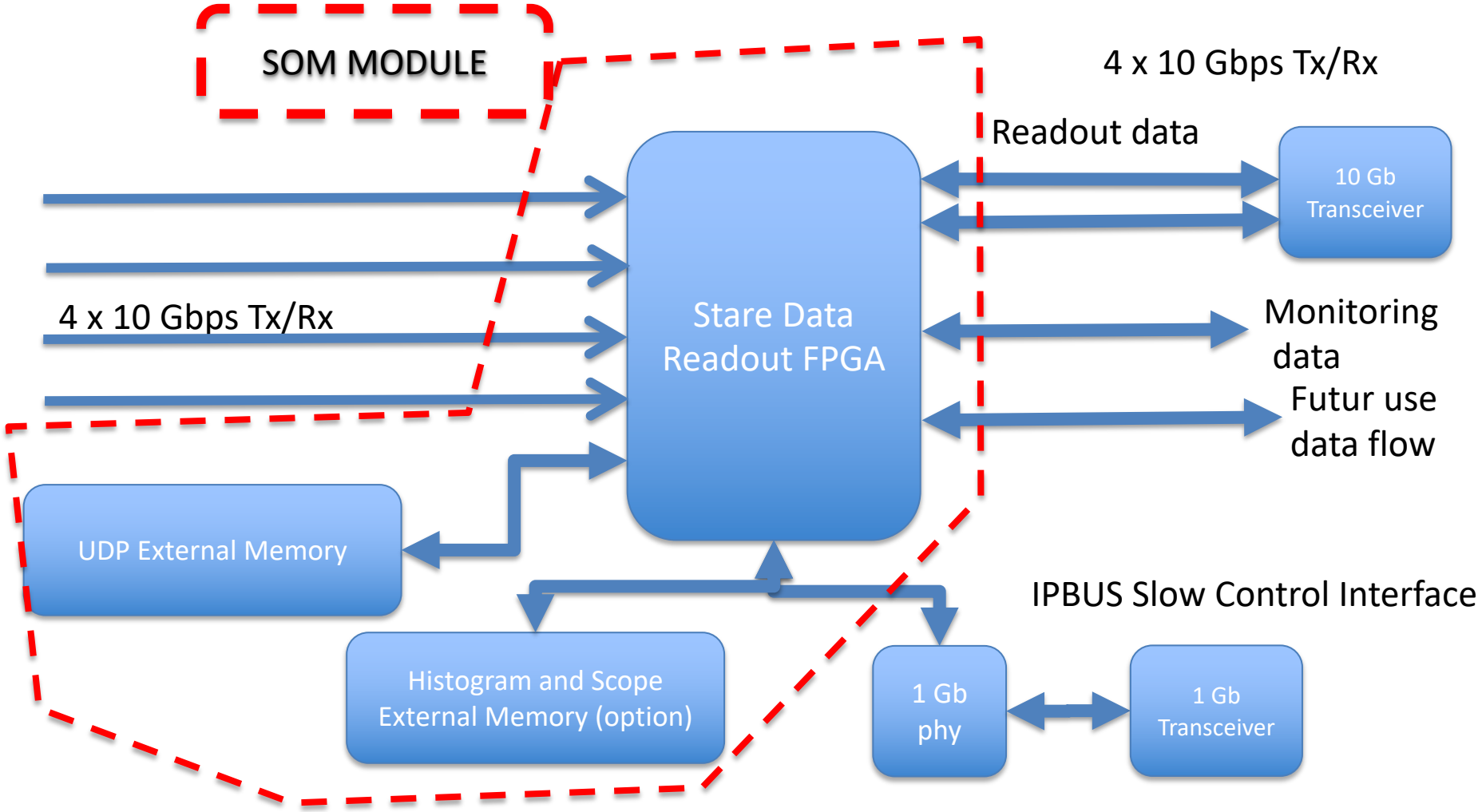
STARE Initial Block Diagram



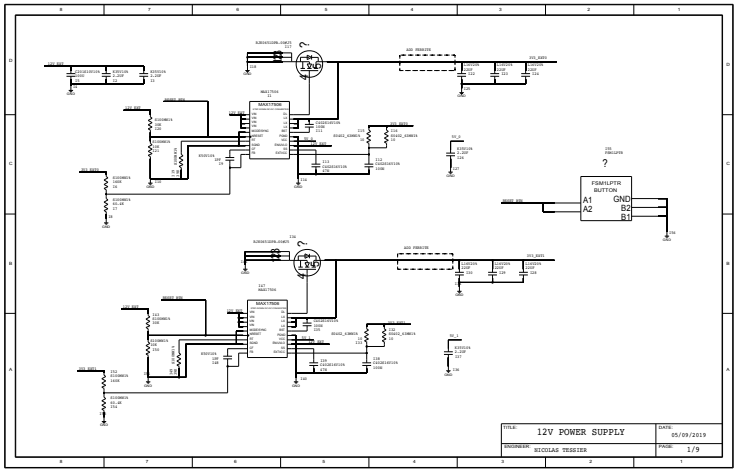
STARE Characteristics

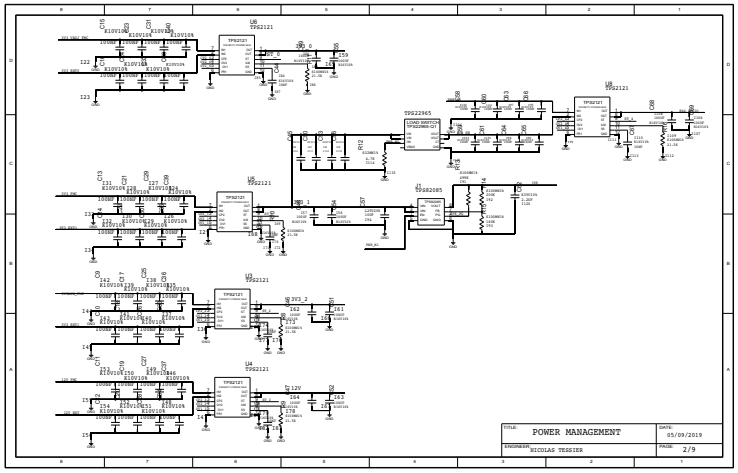
- Input data rate from pre-processing : 4 x 10 Gbps (2 for data 1 for monitoring 1 spare).
- 2 Power supply sources (Internal and external PSU using hot swap mux)
- Spare LVDS I/O with the pre-processing for future use
- Full clock management inside the SOM and the FMC carrier.
- Network Bandwidth up to 4 x 10 Gbps in parallel.
- 1 Gbps IPBus for slow control.
- Some on board facilities to make local comparisons with the DAQ (raw data storage, local Histograms etc...) .
- With this configuration it is absolutely easy to achieve continuous and comfortable 10 Gbps with monitoring and online analysis using multiple 10 Gbps Tx/Rx.
- Only the Hardware side is presented. Nothing on the software side yet (on-going discussion with computer team).

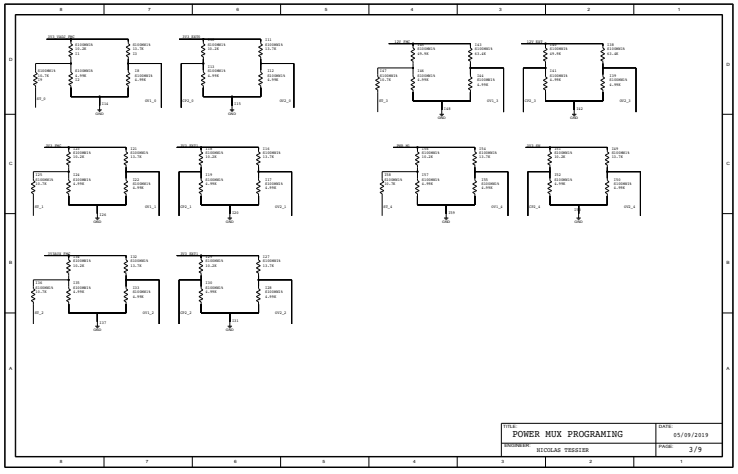
STARE New Block Diagram

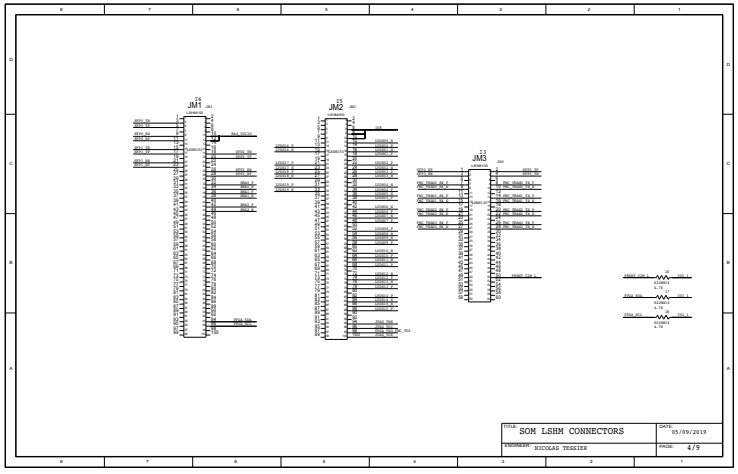


STARE Carrier Board Schematics ongoing

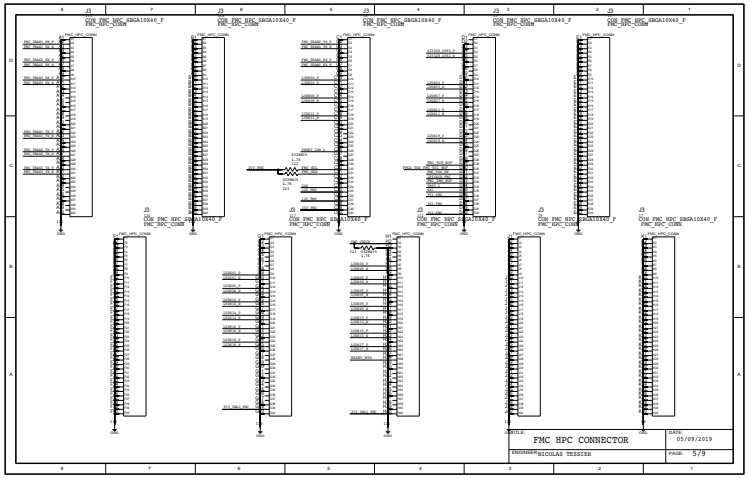


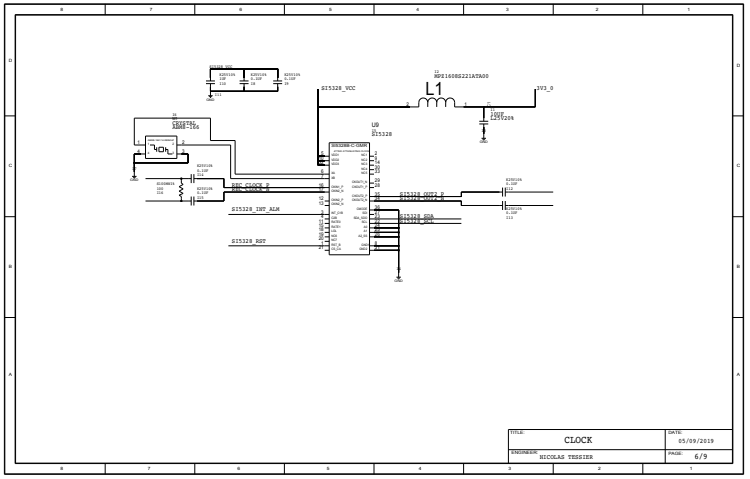


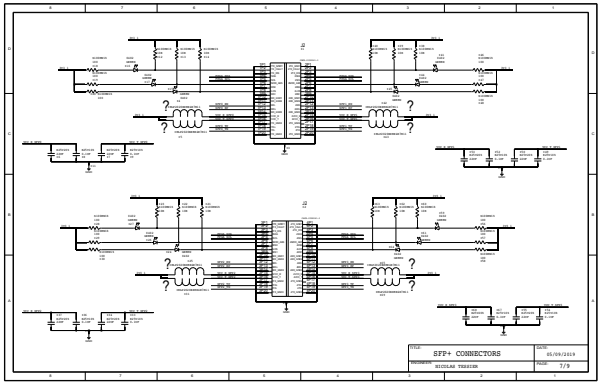


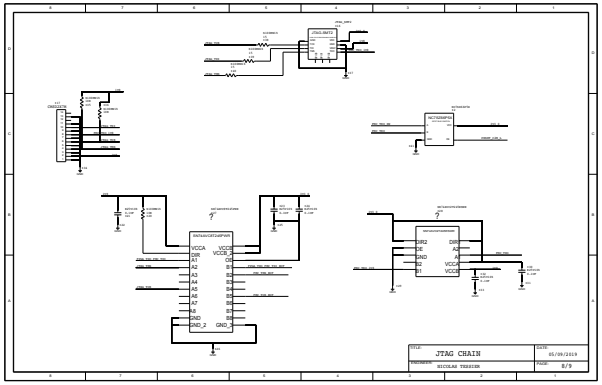


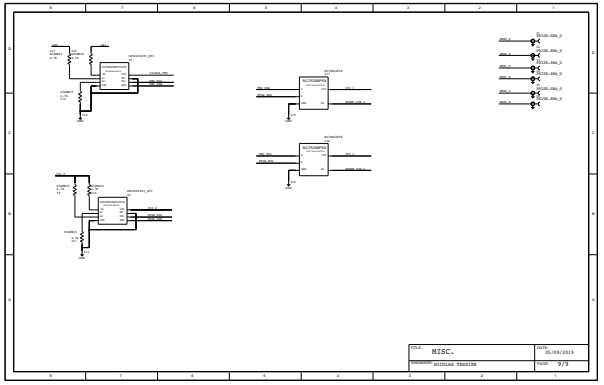
STARE Carrier Board Schematics ongoing











STARE Hardware Future Plans

- Schematics design finishing, CAD routing and manufacturing files (Q1 2020)
- Preseries production (Q2 2020)
- Preseries Tests with Valencia team (Q4 2020)
- Production (Q2 2021)

STARE Firmware Future Plans

- Firmware ongoing (See Gustav presentation)
- Slow Control Software to be defined and designed (6 months intern student TBD)
- Firmware Update (6 months intern TBD)
- Production test bench to be designed (6 months intern TBD).
- Built-in Self Test for 100 % assembly and design coverage (6 months intern TBD).
- Documentations (Q4 2020)
- Maintenance Contract

- Thank you