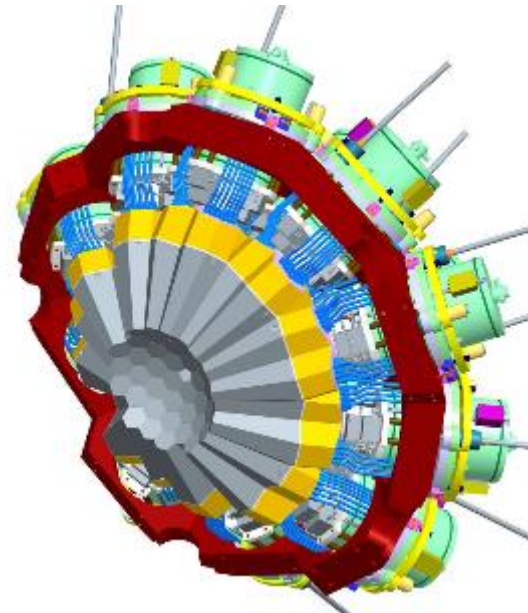
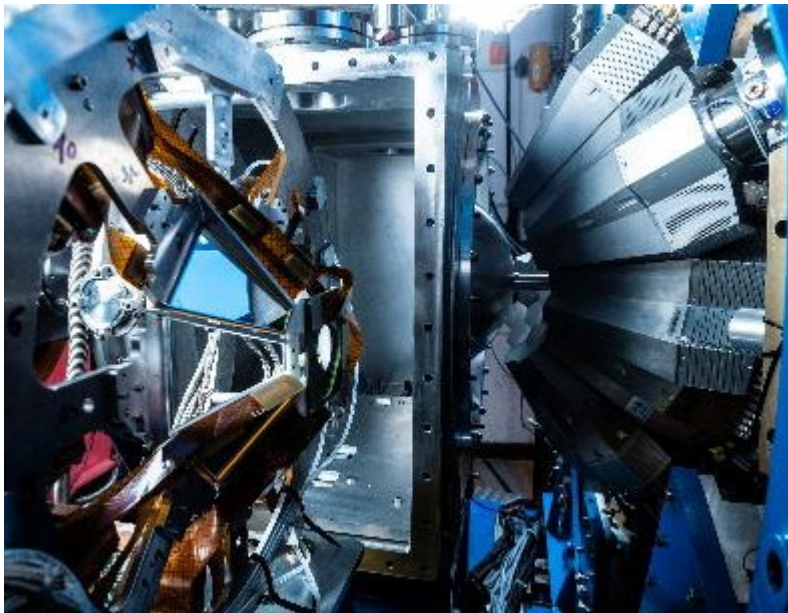


AGATA Electronics Maintenance Report: September 2019



On behalf of the AGATA Collaboration Electronics W.G.



20th AGATA Week, INFN-Laboratori Nazionali di Legnaro, (Padova), Italy
17th – 19th September 2019

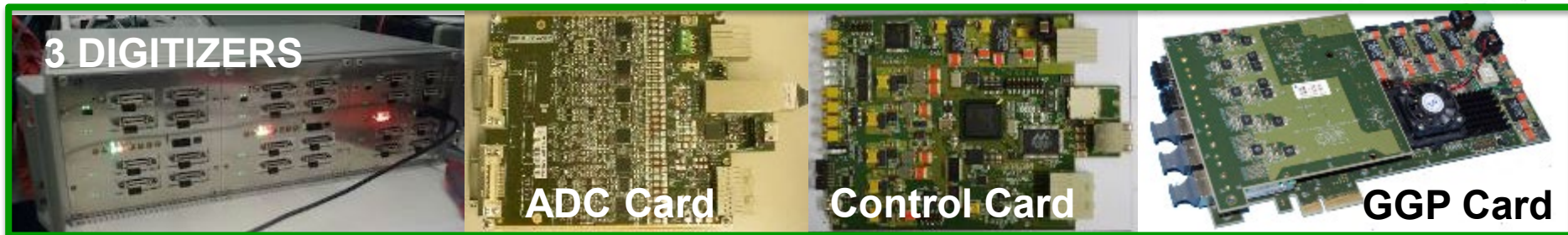


AGATA Electronics Phase 0/Early1



24 channels available and working: obsolescence
Communication Synchronization issues in DIGITIZER cards

AGATA Electronics Advanced Phase 1



From 1st production batch only 10 GGP & 13 Digitizers available
(only 6 out of 14 AGATA GGPs).

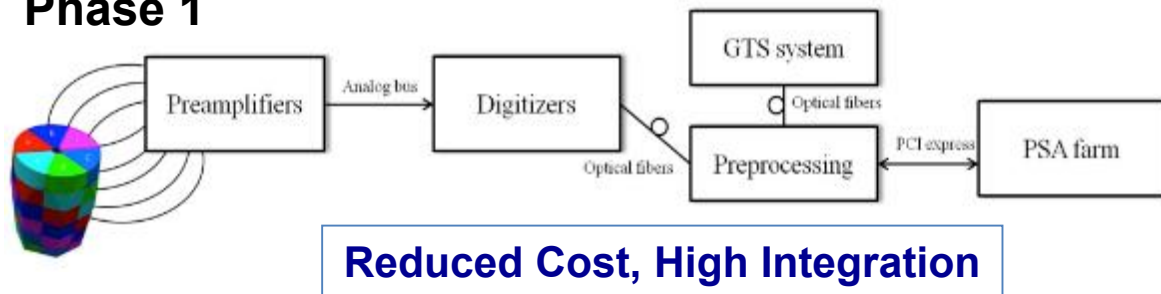
From 2nd production 13 GGP (total 14) and 14 Digitizers (total 15) available

Phase 0 Digitisers

- Preprocessing sends 100MHz clock over fibre
- Digitiser distributes 100MHz internally (sine wave)
- Digitiser FPGAs generate serial data stream (2GHz)
- Data stream doesn't send commas. Relies on clocks staying in phase (Start and resync send commas)
- In 3/27 digitisers (5,7,15) low gain data stream loses sync.
- Why do clocks go out of phase? Theories:
 - Fibres (Dirt or ageing of fibre or xceivers?)
 - Xceiver very sensitive to power fluctuations (report from mezz)
 - Why only low gain? Signal position in fibre? FPGA code? Or??
- Next steps following 14th Aug 2019 tests by PCS
 - New digitiser test firmware with more clock diagnostics (2011code loaded during test- still loses sync)
 - Possibly replace xceivers (expensive: \$16k for 20 xceivers)
 - Recommend regular audit temp scans (several close to 40C)

Advanced Phase 1 Electronics

Phase 1



PCI Pre-Processing Card GGP



ADC Card



Control Card



- Aiming to complete 45 channels for the GANIL setup + Spares
- Delivery performed early 2019
- DIGIOPT12-DIGITIZERS (INFN-Milano, ETSE-Valencia): 14 Delivered in January and early February 2019.
- GGPs (INFN-Padova): 13 GGPs delivered and installed at GANIL on February 2019
- Mounting all spare GGP motherboards to replace non working GGPs
- Digitizers cooling enhanced by ETSE.

D. Barrientos, et al., IEEE TRANS. NS

INFN-Padova INFN-Milano INFN-LNL
IFIC-Valencia ETSE-Uni.Valencia