Dual Readout: electronics option

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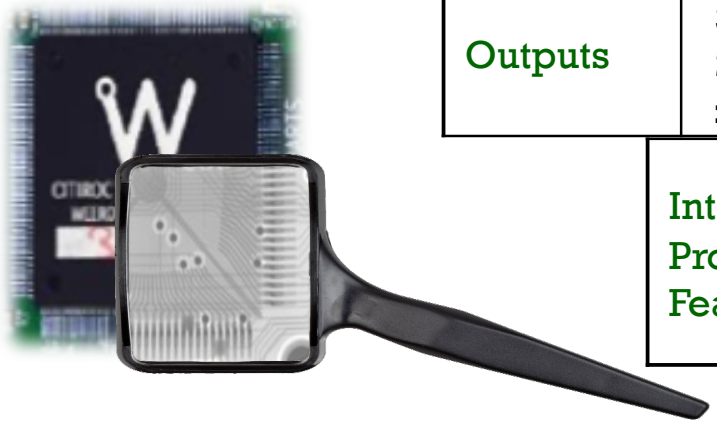
Outline

- The ASIC: Citiroc1A
- The evaluation boards (DT5702 / DT5550W)
- Possible solution for a “medium-size” calorimeter

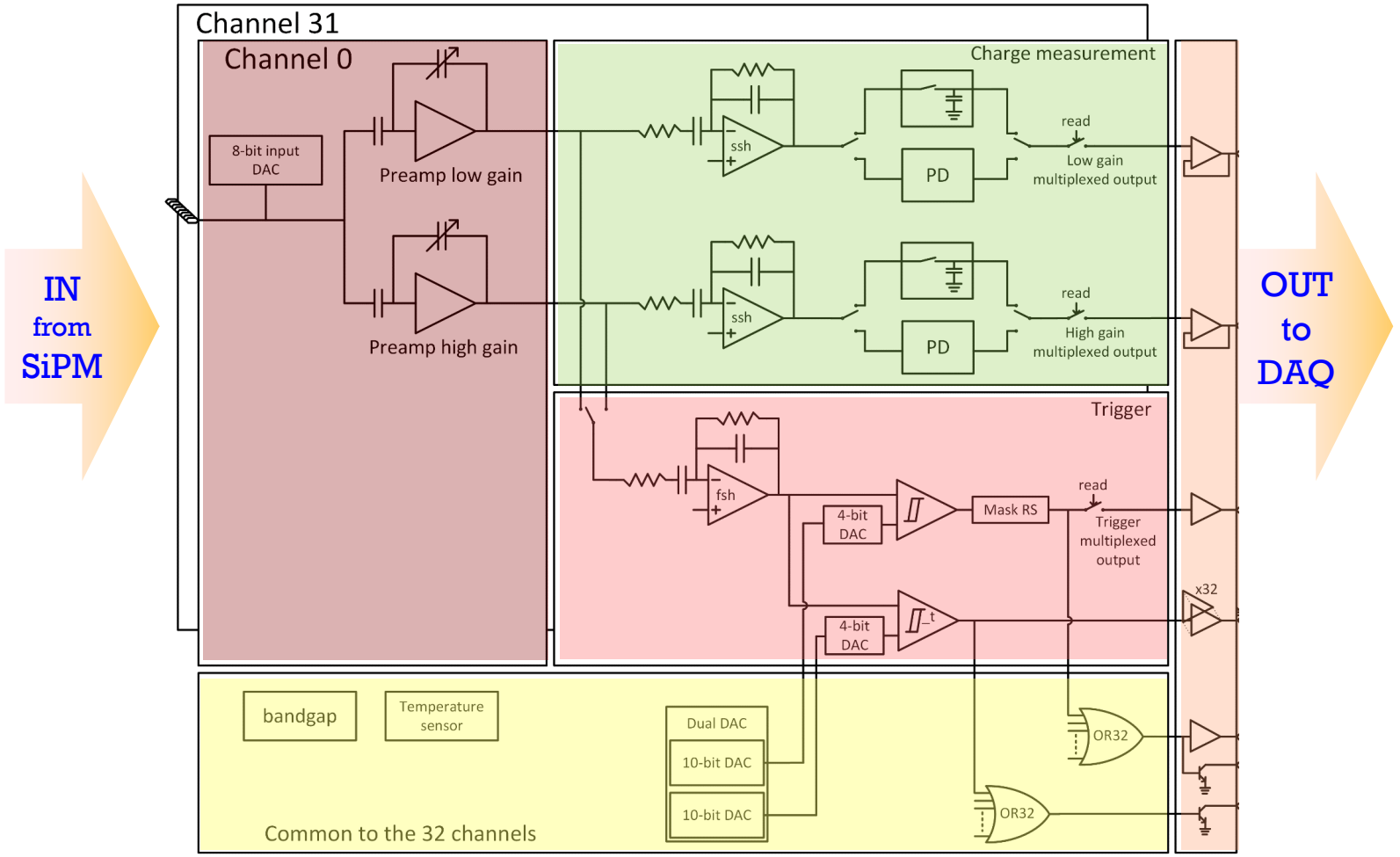
Citiroc1A

weeroc

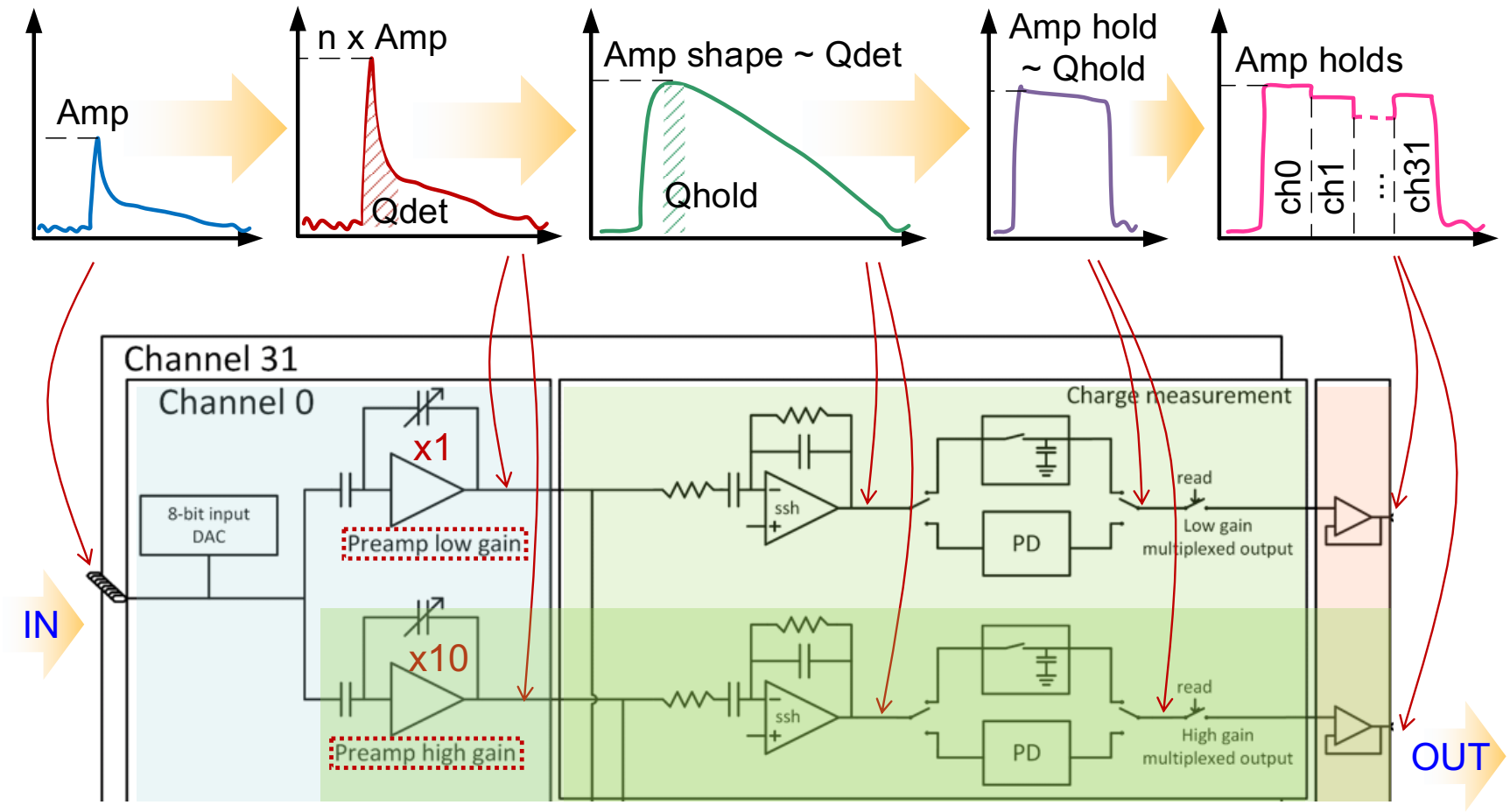
Detector Read-Out	SiPM, SiPM array
Number of Channels	**32**
Signal Polarity	Positive
Sensitivity	Trigger on **1/3 of photo-electron**
Timing Resolution	Better than **100 ps RMS** on single photo-electron
Dynamic Range	0-400 pC i.e. 2500 photo-electrons @ 10^6 SIPM gain
Packaging & Dimension	TQFP160-TFBGA353
Power Consumption	225mW - Supply voltage: 3.3V
Inputs	32 voltage **inputs with independent SiPM HV adjustments**
Outputs	**32 digital outputs (for timing)** **2** multiplexed **charge output, 1** multiplexed **hit register and 2 trigger outputs**
Internal Program. Features	32 HV adjustment for SiPM (32x8bits), Trigger Threshold Adjustment, channel by channel gain tuning, 32 Trigger Masks, Trigger Latch, internal temperature sensor



Citiroc1A: block scheme

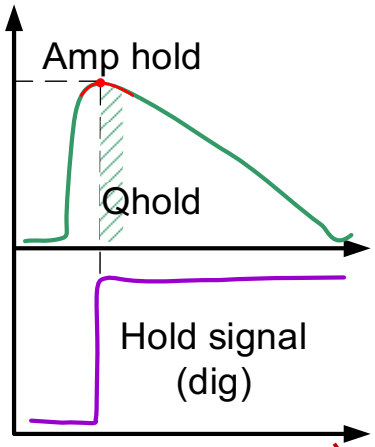


Citiroc1A: charge measurements (I)

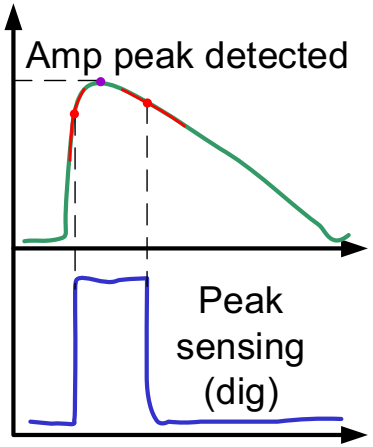


Citiroc1A: charge measurements (II)

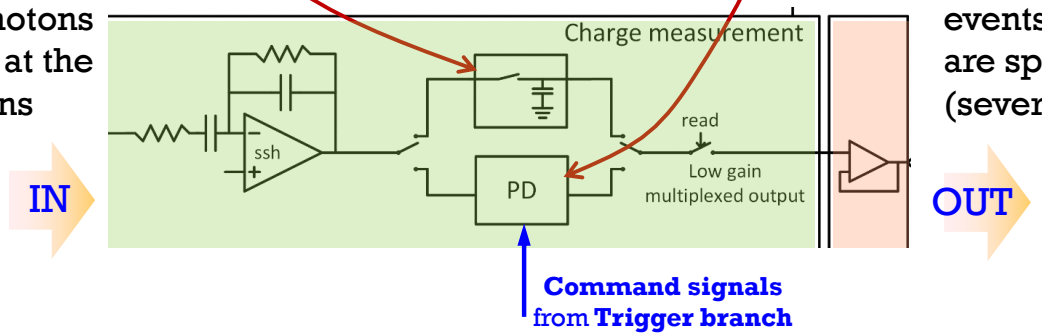
Two techniques implemented to measure the amplitude: Track & Hold and Peak Detector



The choice of the **best peak sampling** solution depends on the final application.

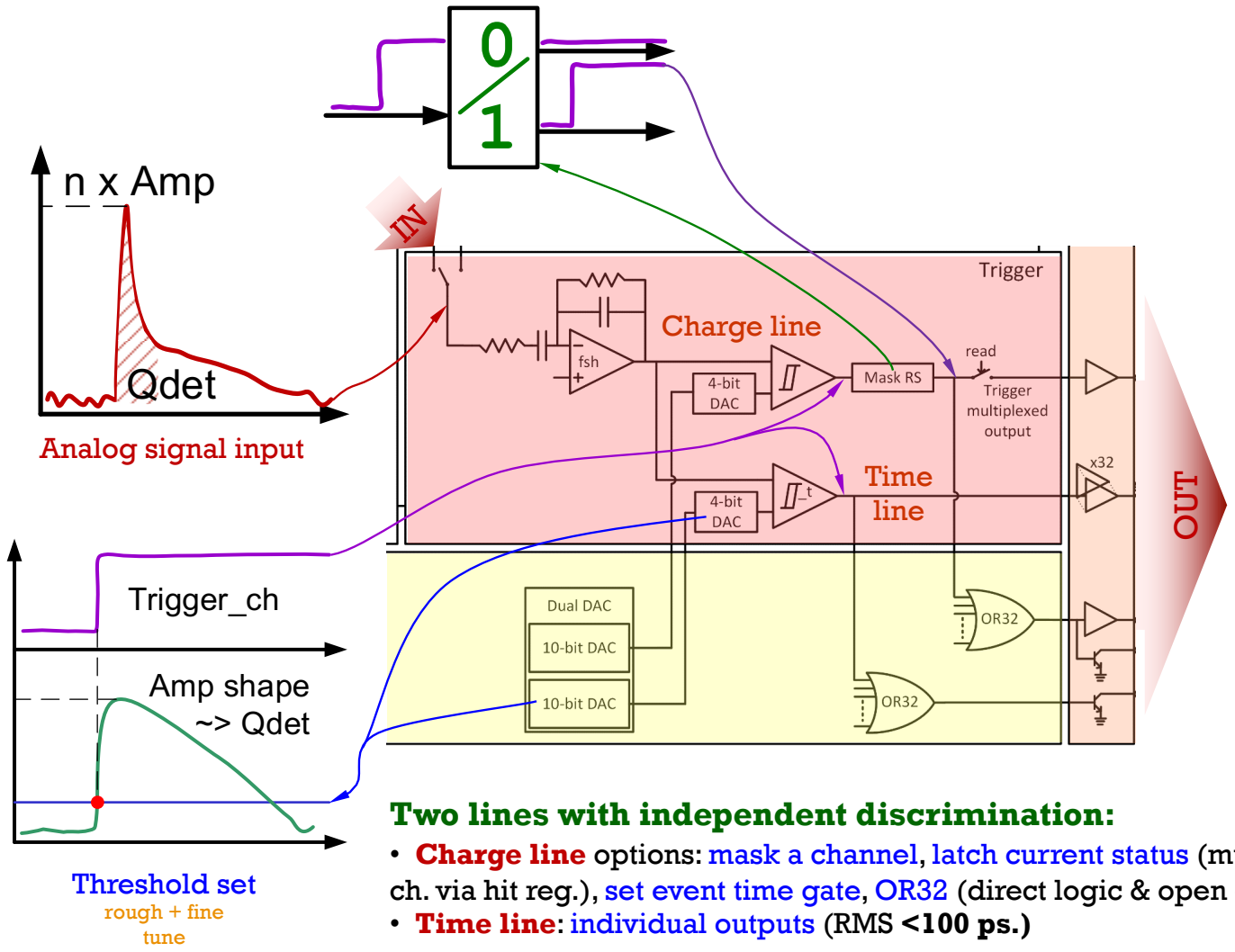


- **Track & hold** is more suitable for events where photons are all detected at the same time (few ns spread)



- **Peak detector** is more suitable for events where photons are spread in time (several 10 or 100ns)

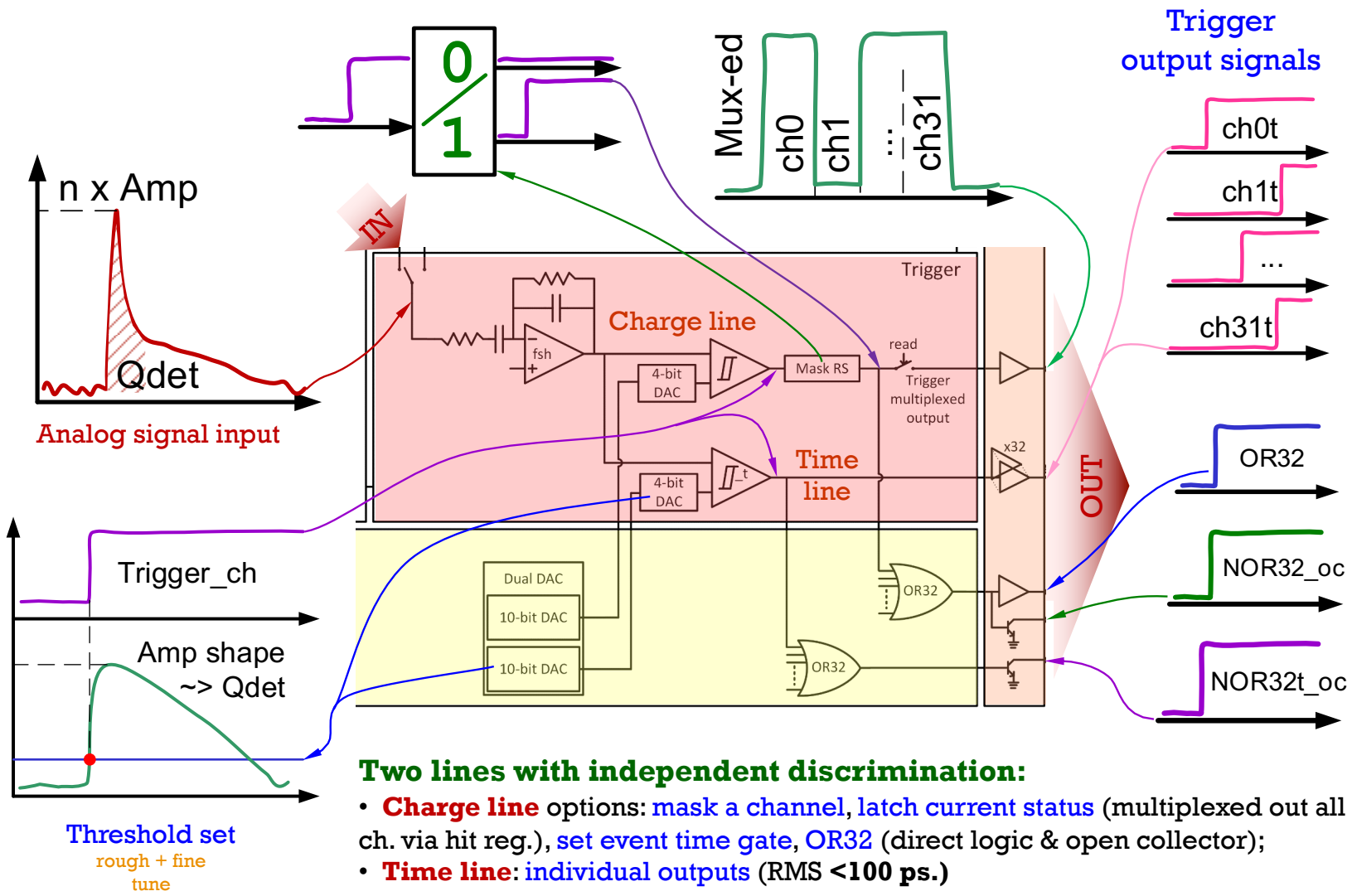
Citiroc1A: trigger and timing



Two lines with independent discrimination:

- **Charge line** options: mask a channel, latch current status (multiplexed out all ch. via hit reg.), set event time gate, OR32 (direct logic & open collector);
- **Time line**: individual outputs (RMS **<100 ps.)**

Citiroc1A: trigger and timing



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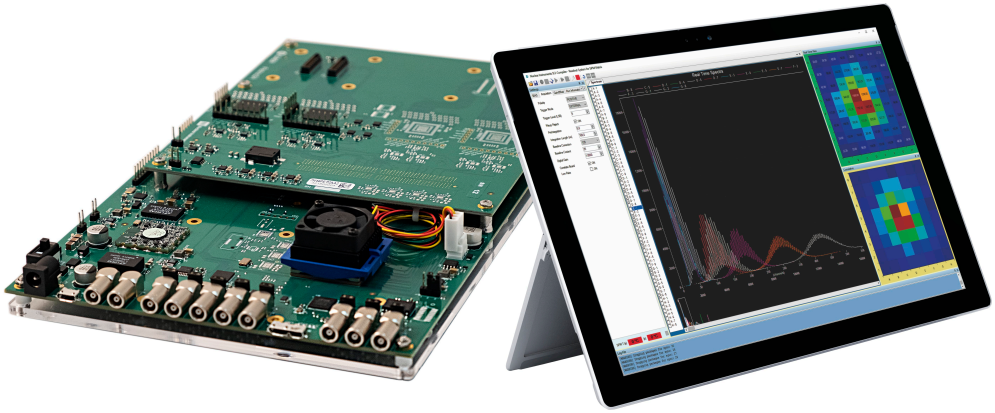
The evaluation boards

A1702 / DT5702

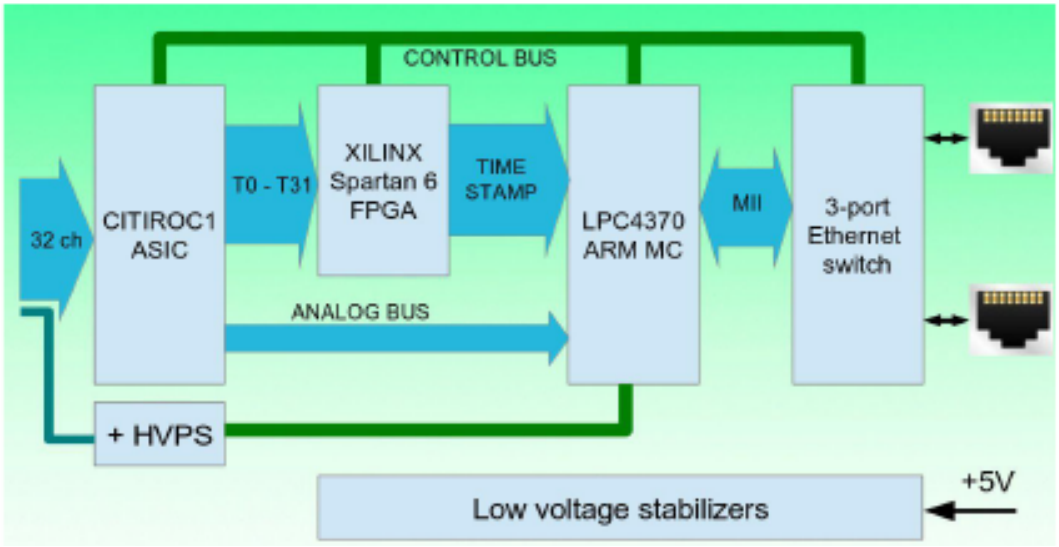
DT5550W



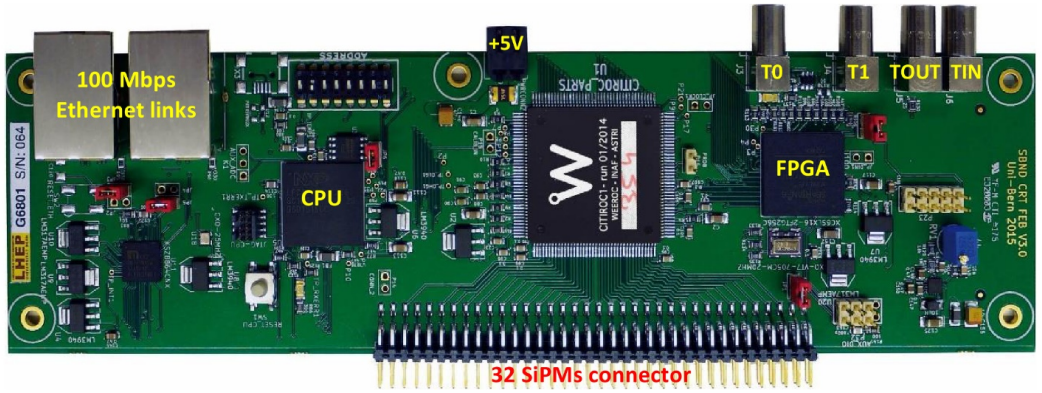
DT5702: general description

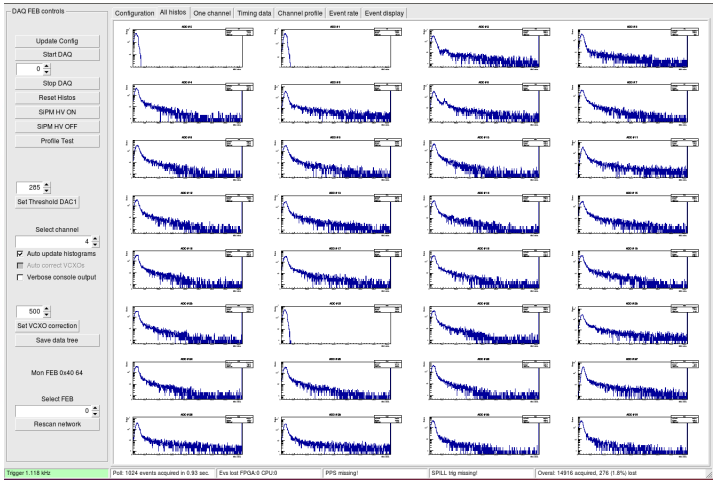
- Provides the bias voltage in the range of 20-90 V. The HV fine adjustment is performed by the ASIC (0.5-4.5V)
- Allows to probe the analogue signal for debug purpose (1ch at the time)
- Provides the signal timestamp (measured in the FPGA) with a resolution of 1ns
- Trigger logic (coincidence of adjacent channels, OR –logic among selected channels), while the possibility of using an external trigger is not implemented
- Daisy chain of up to 256 boards into one network interface

DT5720: block scheme



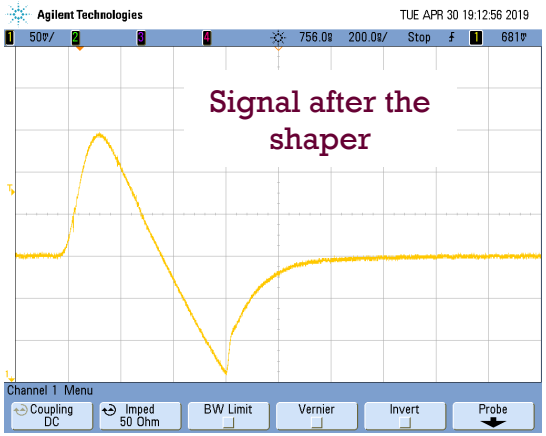
DaQ based on Root script





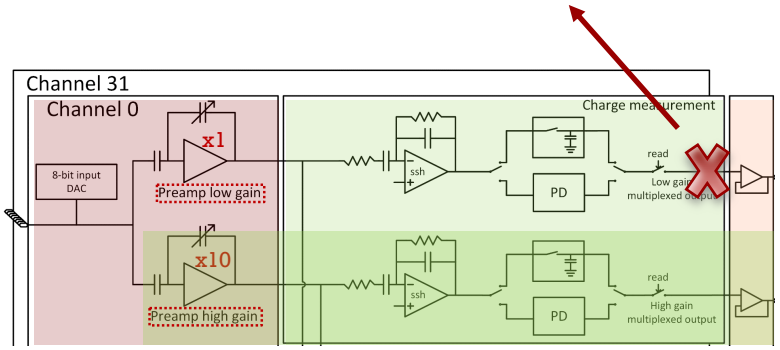
Signal qualification

Typical response to a fast LED using the



Hmamatsu SiPM:
1.3 x 1.3 mm²
50mu cell size

The low gain branch is not accessible in this board



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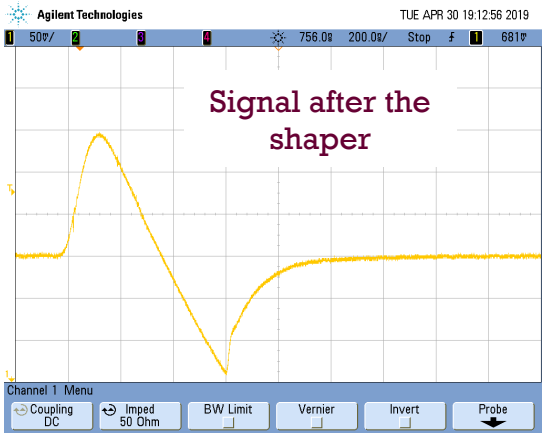

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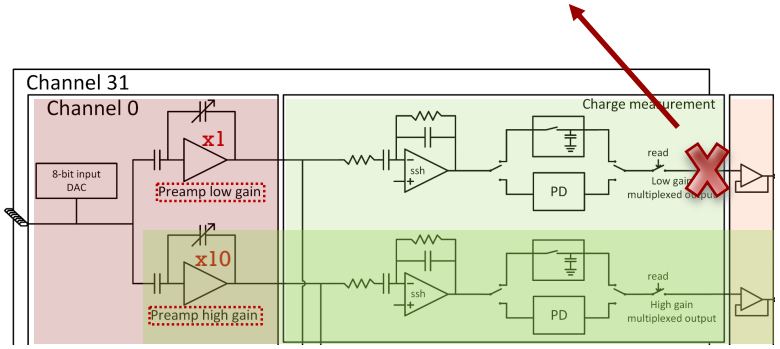
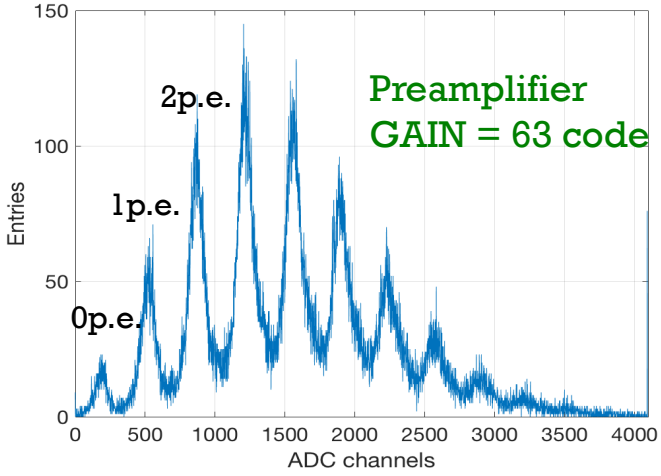
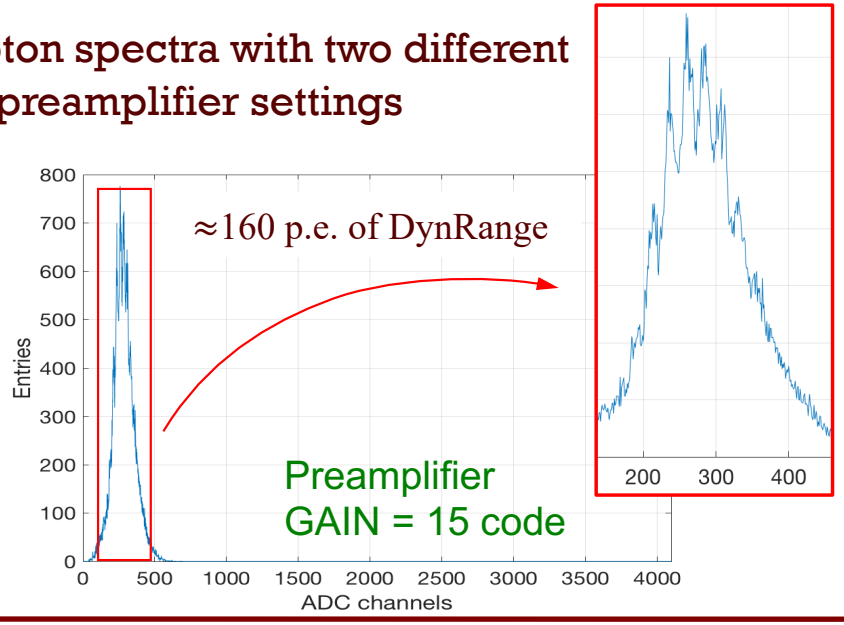


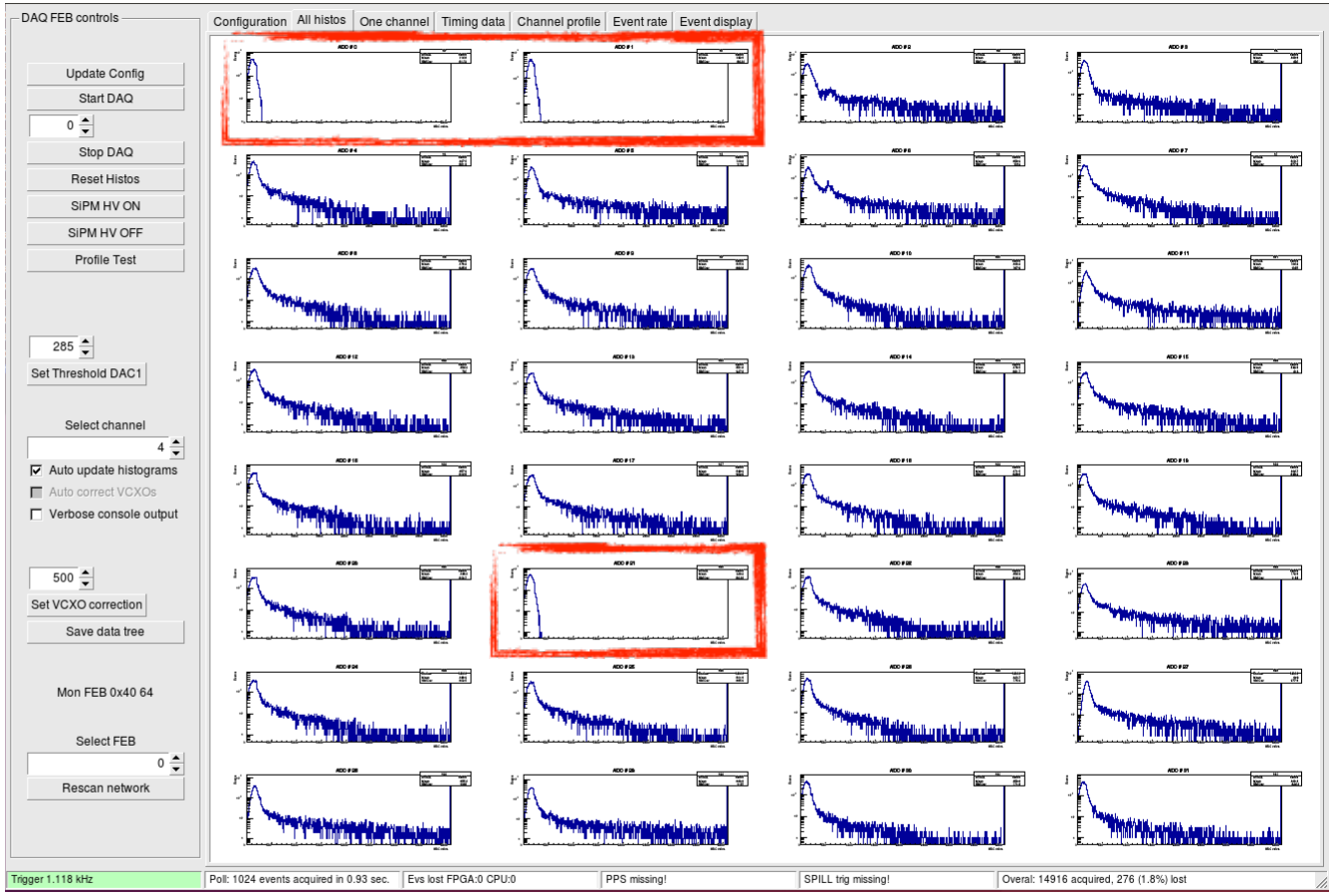
Multiphoton spectra with two different preamplifier settings





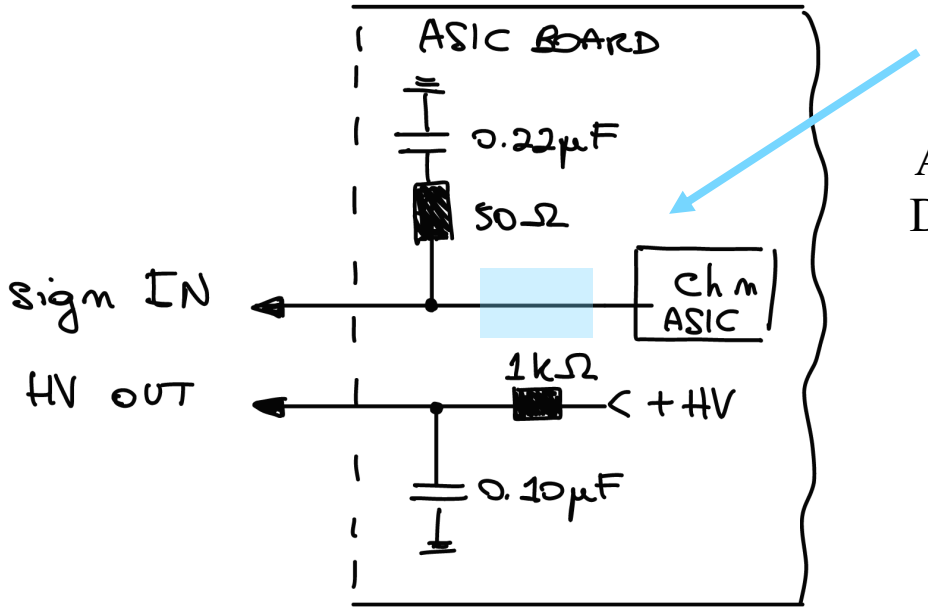
The full system

32 SiPM 1.3x1.3 + LYSO crystal



Almost all channels are working …

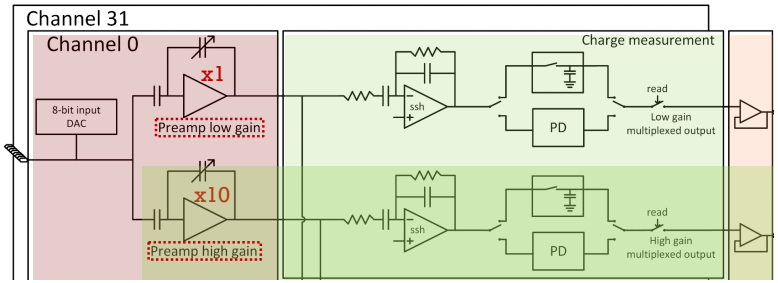
A deeper investigation …



There is no protection along this line

A bad connection or short may destroy the DAC at the input of the channel. The DAC sets the fine voltage regulation

If this happen, the bias applied to the channels will be not the proper one



Few considerations

A good tool for training but we observed few limitations. This is the reason why we still want continue the study of the all Citiroc1A potentialities:

- The dynamic range overlap between the two branches of the same channel
- The ultimate time performance
- The comparison between the track and hold and the peak finder method for the charge measurement
- The use of an external trigger

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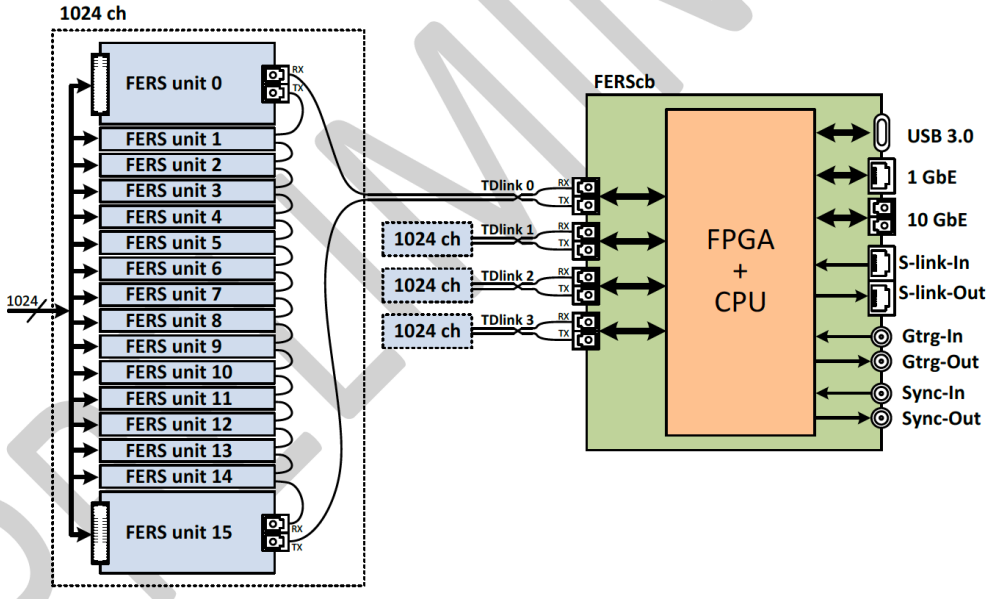
Hopefully the DT5550V board will allows us to investigate all the functionalities

But it is still not what we need for a test on beam!

DT5550W

How to handle a "medium-size" calorimeter?

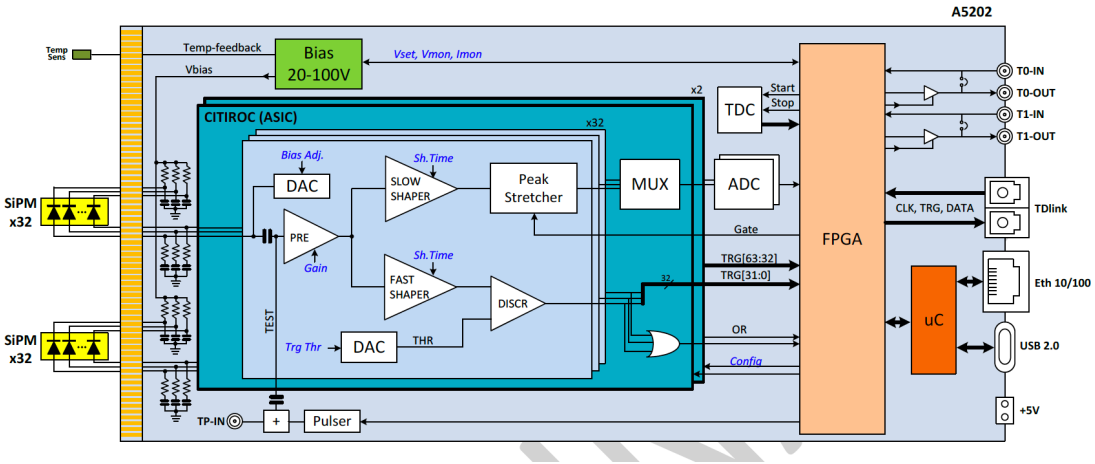
If the Citirorc1A qualification will fulfils our requirements we still need a compact and scalable solution for a test beam



The basic principle

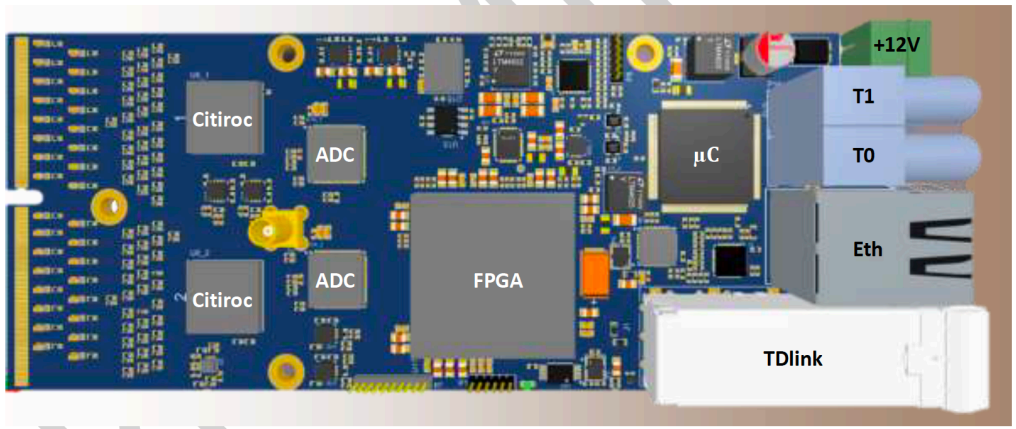
- FERS-unit can be used in standalone or connected to the system
- Up to 16 FERS-unit can be connected in daisy-chain (FERSnet)
- The FERSnet data throughput is up to 200 MB/s
- The FERScb is a data collector housing 4 high speed optical link (TDLink)
- The connection to the host PC is performed with a 10 Gbit ethernet
- The FERScb has an embedded ARM processor (Quad Core) running Linux for data processing / data compression

FERS unit - Citirorc: block scheme



The basic principle

- 2 Citiroc1A (64 ch)
- Timing with a TDC implemented into the FPGA (≈ 0.5 ns)
- 2 ADC to measure the charge
- 1 HV power supply (20 – 100V) with temperature compensation
- Interface for readout



60 mm

150 mm

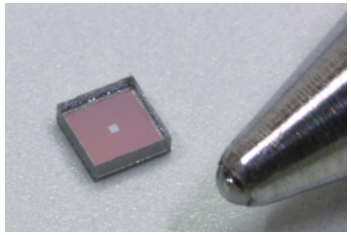
In short

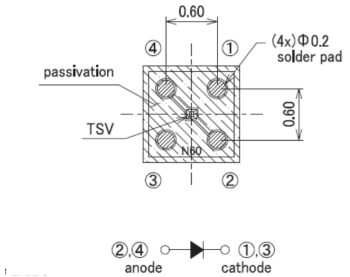
- The Citiroc1A still looks a good candidate for the readout, but the full qualification is not completed
- By the end of June we should receive the DT5550W. This board should allow us to qualify the missing points
- The solution with the FERS could be a good possibility for a future test beam
- We will qualify a first board as soon as it will be available (hopefully is September 2019)

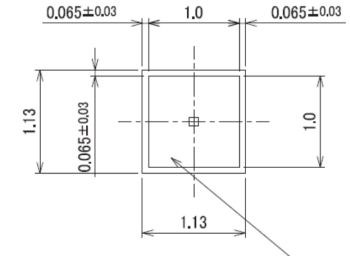
Backup

The chosen SiPM

The sensor in use has 25 μm cell pitch (S13615-1025)





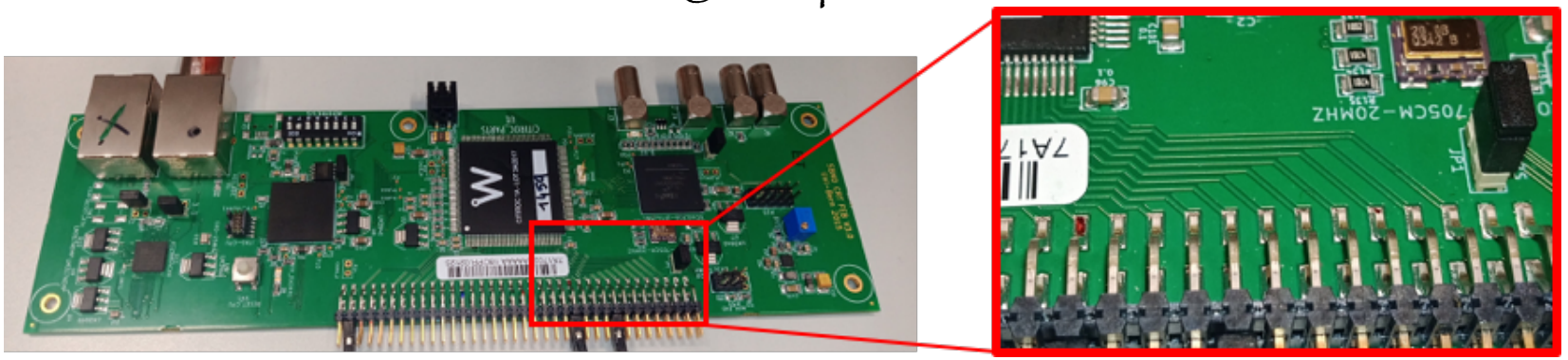


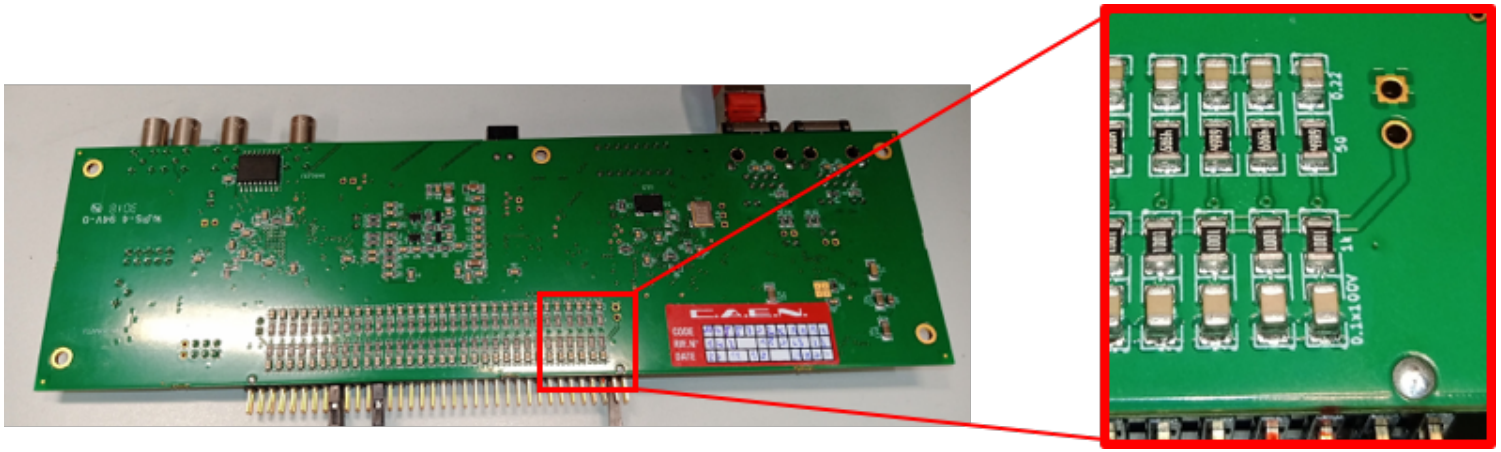
Parameters	S13615		Unit
	-1025	-1050	
Effective photosensitive area	1.0x1.0		mm^2
Pixel pitch	25	50	μm
Number of pixels / channel	1584	396	-
Geometrical fill factor	47	74	%

Parameters		Symbol	S13615		Unit
			-1025	-1050	
Spectral response range		λ	320 to 900		nm
Peak sensitivity wavelength		λp	450		nm
Photon detection efficiency at λp[*3]		PDE	25	40	%
Breakdown voltage		V_{BR}	53 ±5		V
Recommended operating voltage[*4]		V_{op}	V_{BR} + 5	V_{BR} + 3	V
Dark Count	Typ.	-	50		kcps
	Max.		150		
Crosstalk probability	Typ.	-	1	3	%
Terminal capacitance		Ct	40		pF
Gain[*5]		M	$7.0x10^5$	$1.7x10^6$	-

asic board DT5702

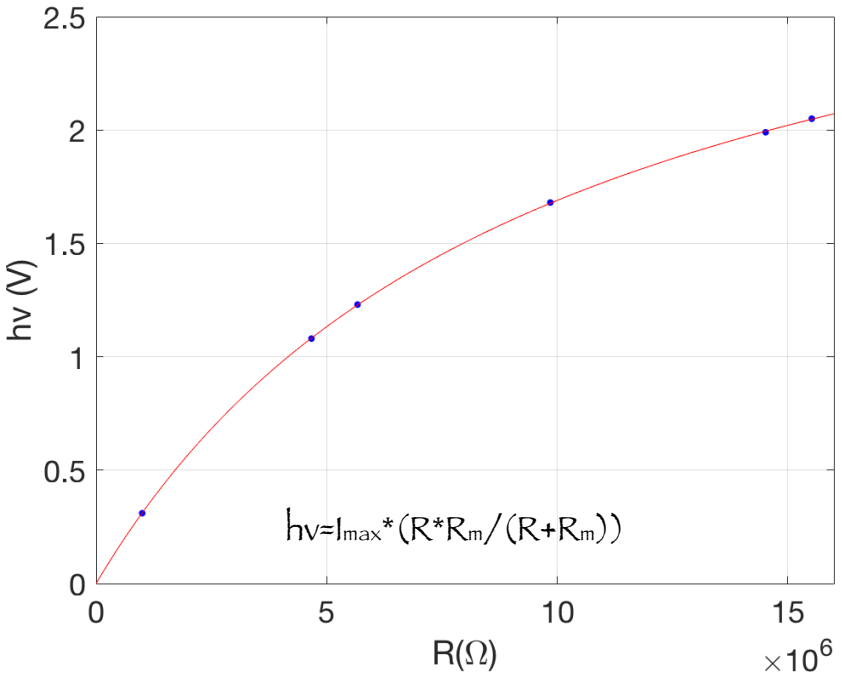
We have started investigating the front-end board: parts of HV outputs and signal inputs



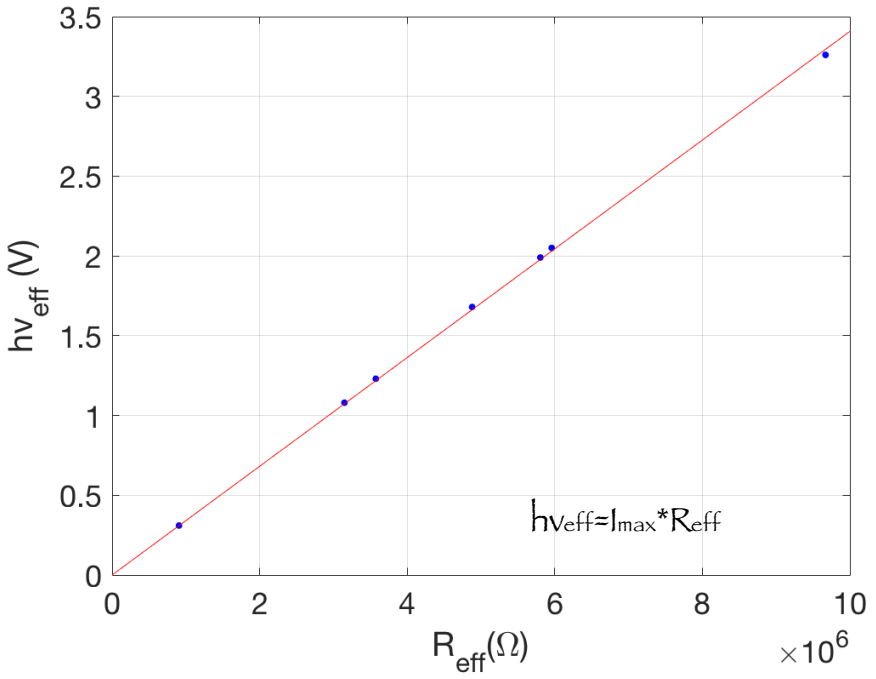


current of dac

We don't connect the array but we put different resistance between input of DAC and ground



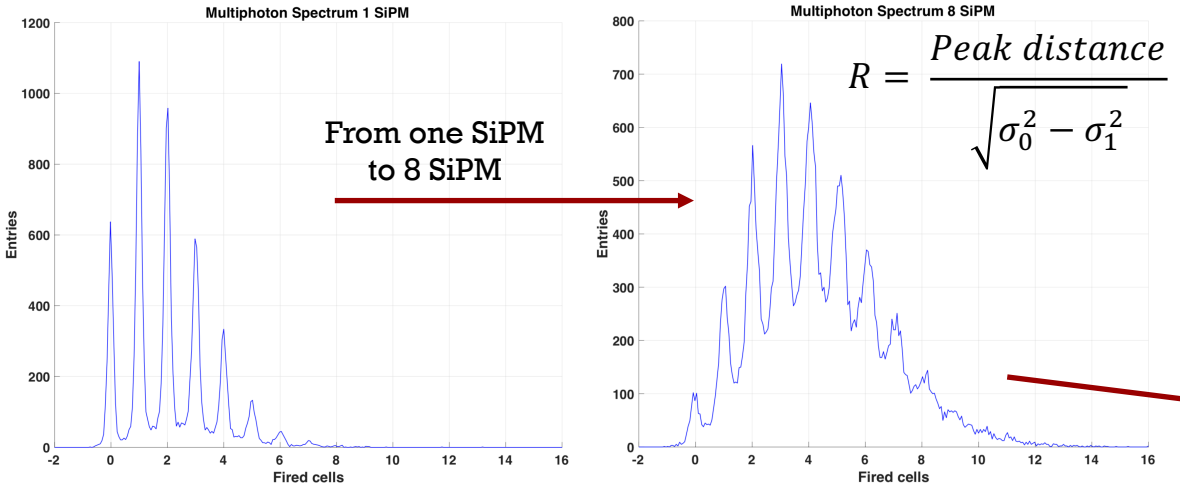
Imax=0.3436μA
Rm=9.673MΩ



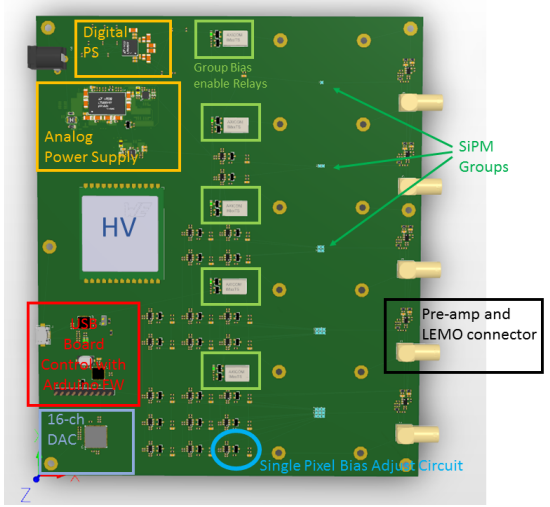
Imax=0.3408μA

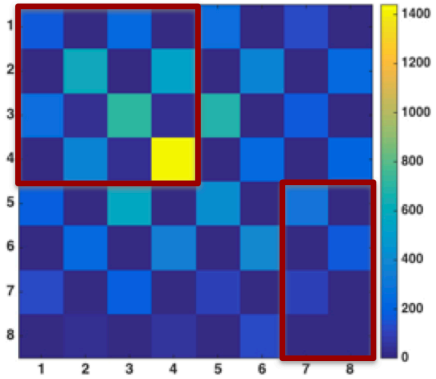
Signal Grouping

- This board allows to investigate the SiPM performances when the signals are grouped analogically (from 1 to 9 SiPMs)
- Each SiPM is individually biased
- Same FEE used in the test beam



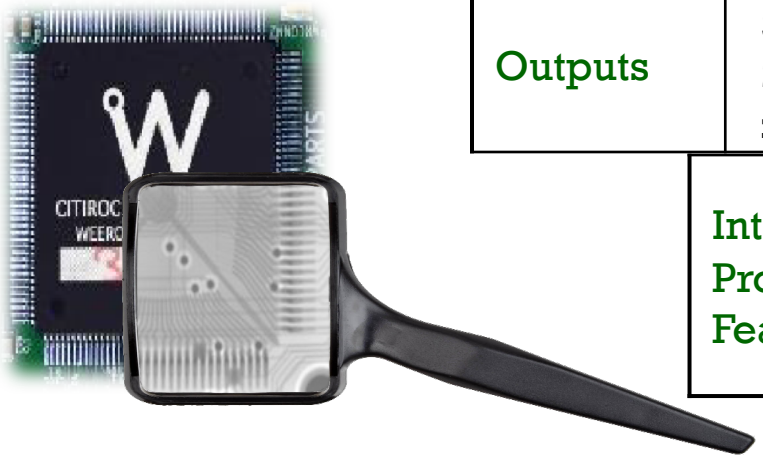
$$R = \frac{Peak\ distance}{\sqrt{\sigma_0^2 - \sigma_1^2}}$$

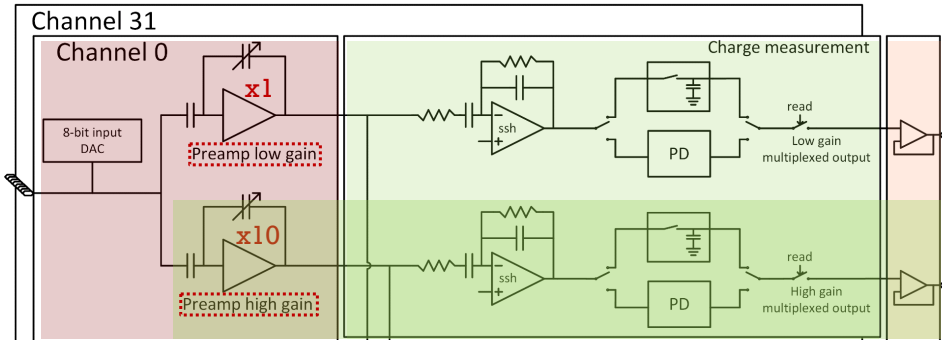


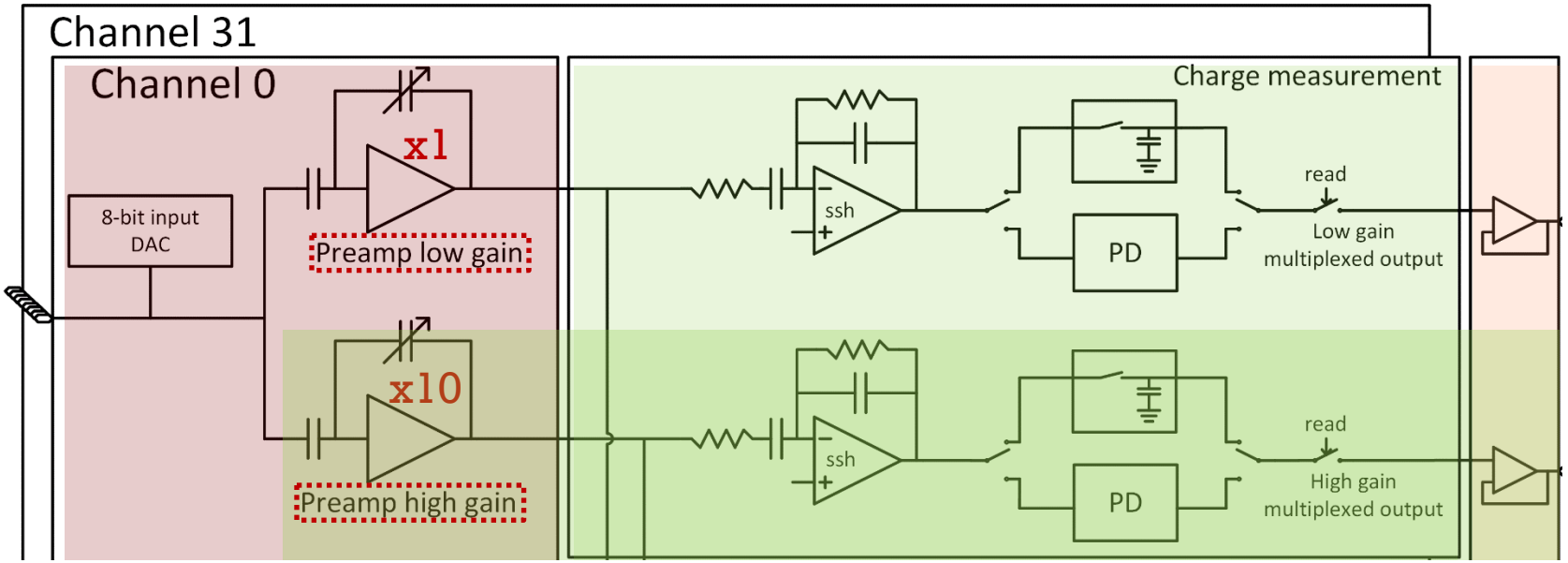


	1 SiPM	4 SiPM	8 SiPM
R = resolving power (ph-e)	24.5	16.6	10.0
Space granularity (mm^2)	≈4.5	≈18	≈36

Detector Read-Out	SiPM, SiPM array
Number of Channels	**32**
Signal Polarity	Positive
Sensitivity	Trigger on **1/3 of photo-electron**
Timing Resolution	Better than **100 ps RMS** on single photo-electron
Dynamic Range	0-400 pC i.e. 2500 photo-electrons @ 10^6 SIPM gain
Packaging & Dimension	TQFP160-TFBGA353
Power Consumption	225mW - Supply voltage: 3.3V
Inputs	32 voltage **inputs with independent SiPM HV adjustments**
Outputs	**32 digital outputs (for timing)** **2** multiplexed **charge output, 1** multiplexed **hit register and 2 trigger outputs**
Internal Program. Features	32 HV adjustment for SiPM (32x8bits), Trigger Threshold Adjustment, channel by channel gain tuning, 32 Trigger Masks, Trigger Latch, internal temperature sensor




Channel 31
Channel 0
x1
8-bit input DAC
Preamp low gain
x10
Preamp high gain
Charge measurement
ssh
PD
read
Low gain multiplexed output
High gain multiplexed output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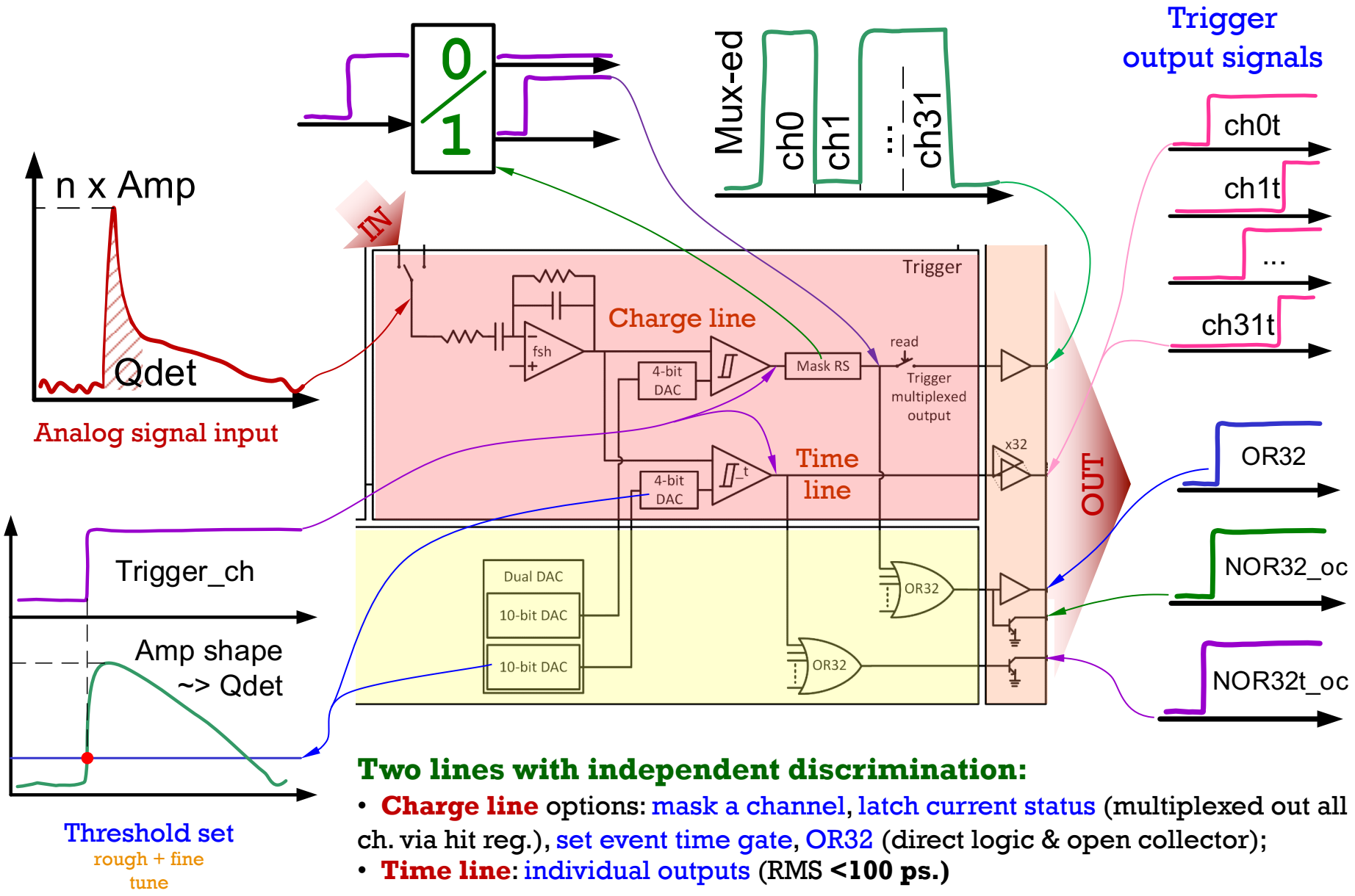
Signal processing & outputs of trigger branch



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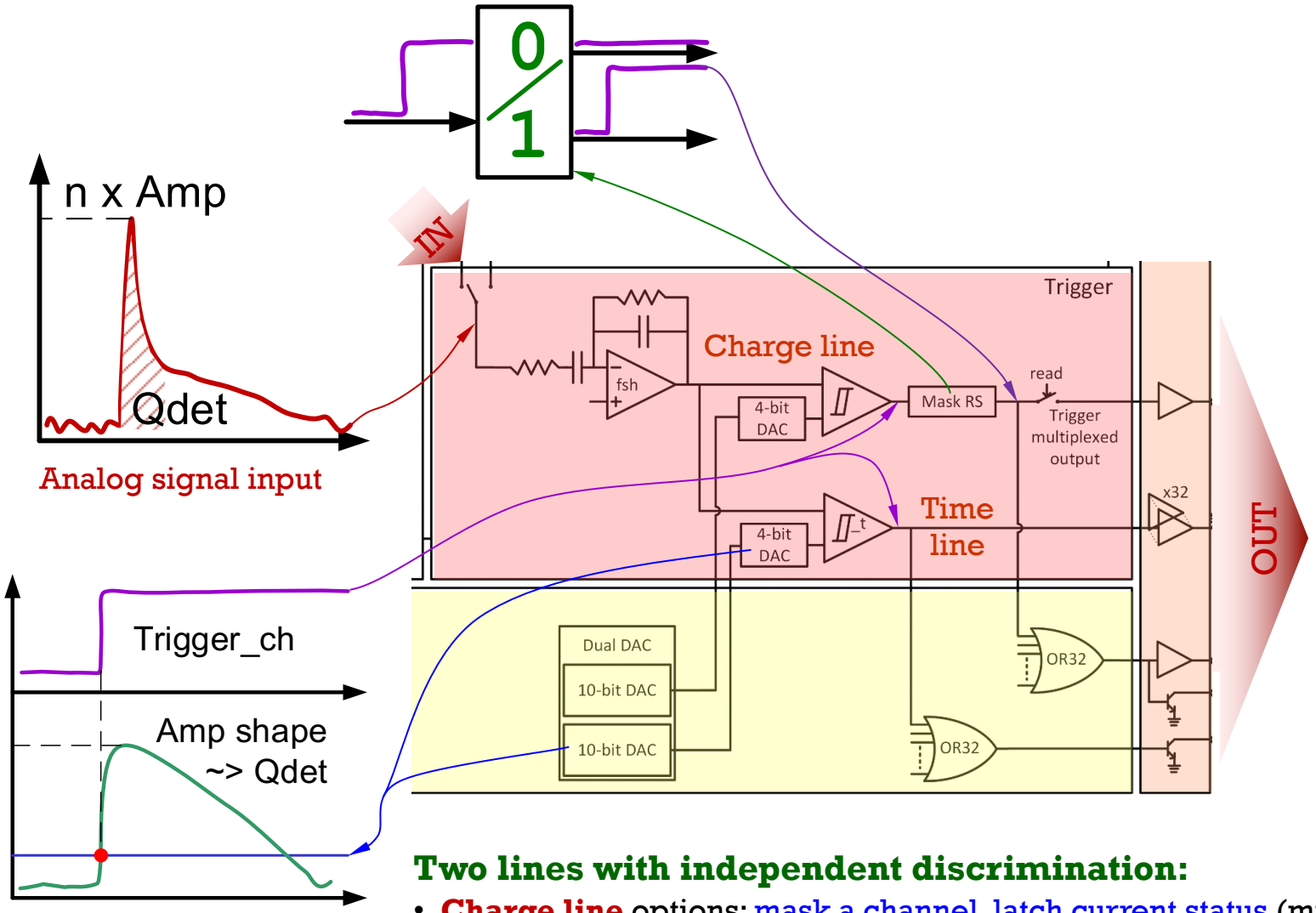
Signal processing & outputs of trigger branch



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