# Update on μ-RWELL R&D

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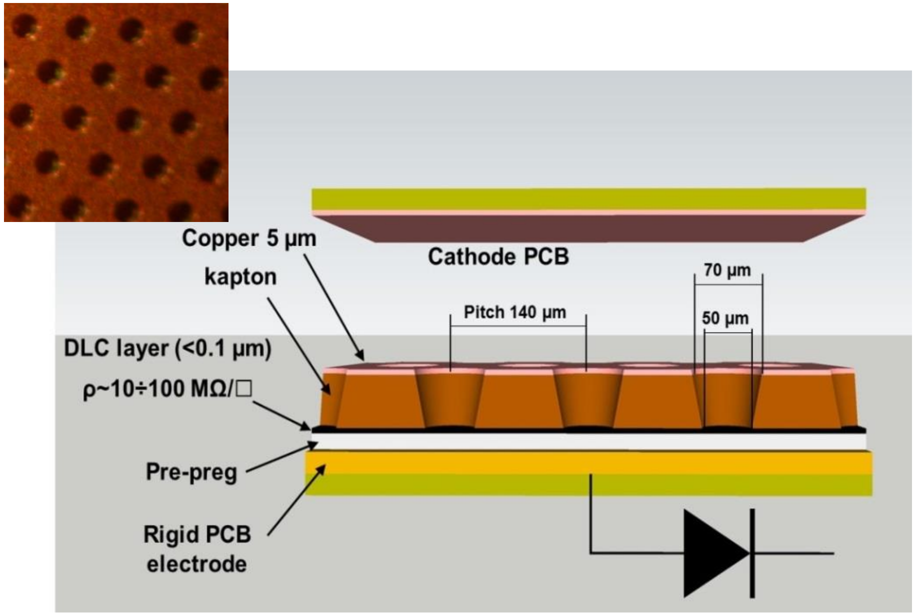
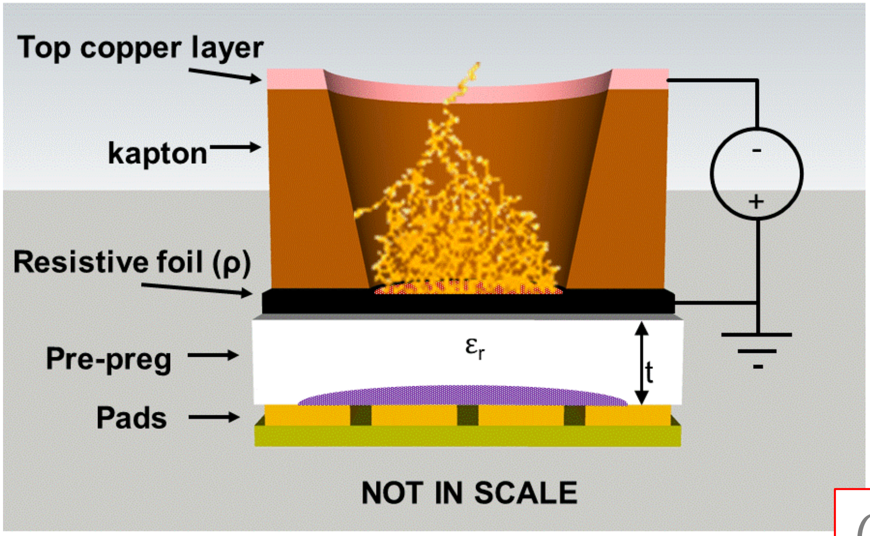
# The µ-RWELL architecture

The µ-RWELL is composed of only two elements:
- µ-RWELL_PCB
- drift/cathode PCB defining the gas gap

µ-RWELL_PCB = amplification-stage ⊕ resistive stage ⊕ readout PCB



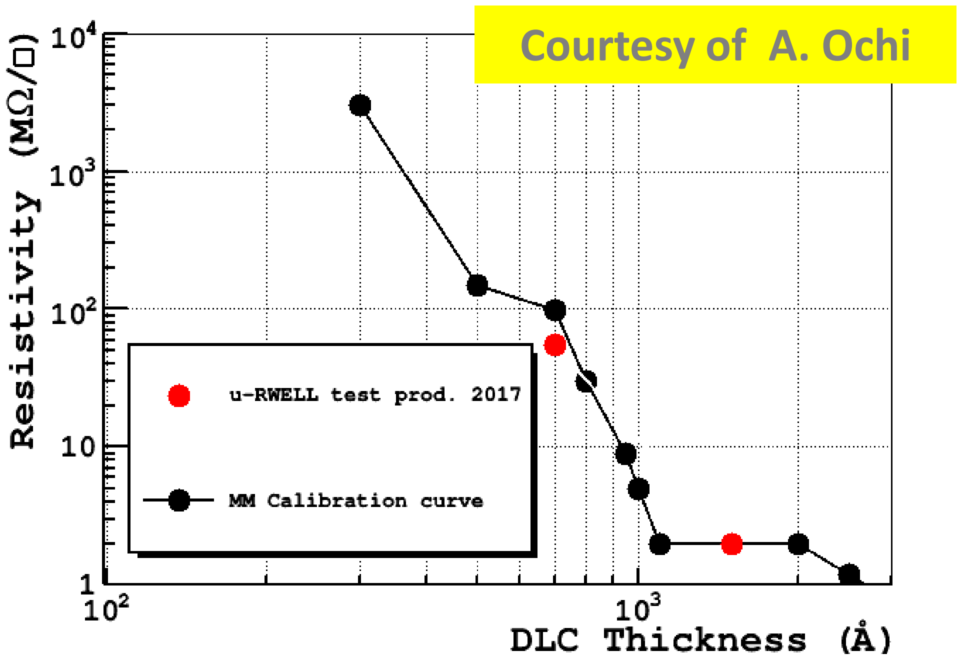




- The "WELL" acts as a multiplication channel for the ionization produced in the gas of the drift gap
- The charge induced on the resistive layer is spread with a time constant, τ ~ ρ×C

$C = \varepsilon_0 \times \varepsilon_r \times \frac{S}{t} \cong 50\ pF/m$ (pitch/width 0,4 mm)

# The resistive layer: DLC sputtering

The **Diamond Like Carbon (DLC) is sputtered** on one side of a **50 µm thick Apical® foil** using a pure graphite target, on **the other side** of the **foil the usual 5 µm thick Cu layer**, as for the base material used for GEM foil, is deposited.



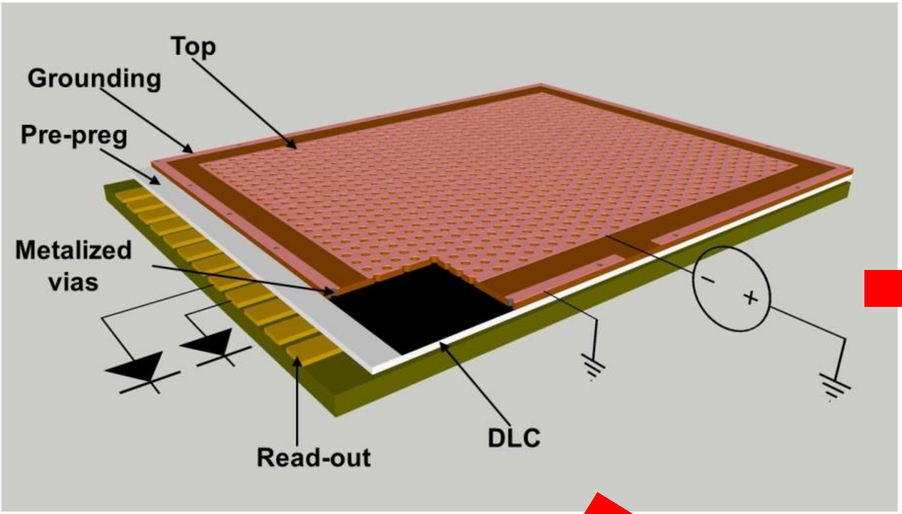

NEW

Recent developments, at **USTC – Hefei (Zhou Yi)**, brought to the manufacturing **of DLC+Cu sputtered Apical® foils**, where an **additional layer of few microns of Cu above the DLC** coating has been deposited.

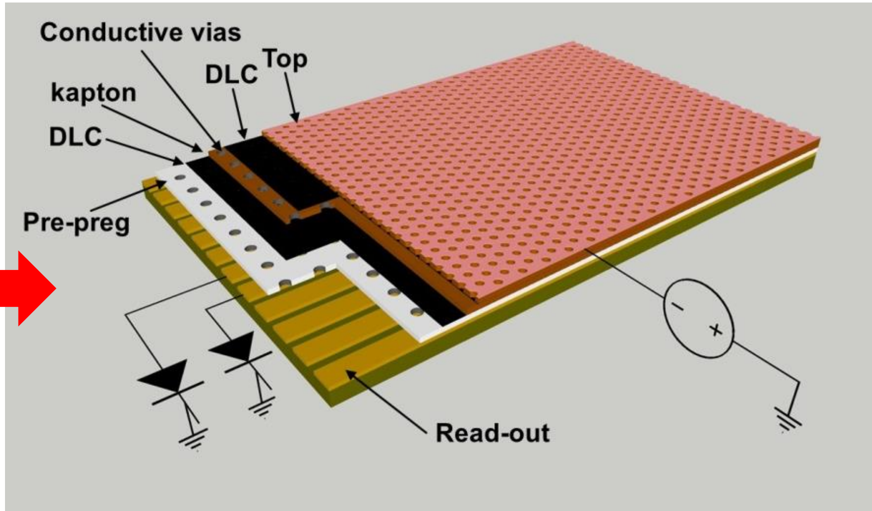
This new coating open the way towards **improved high rate µ-RWELL layouts** .

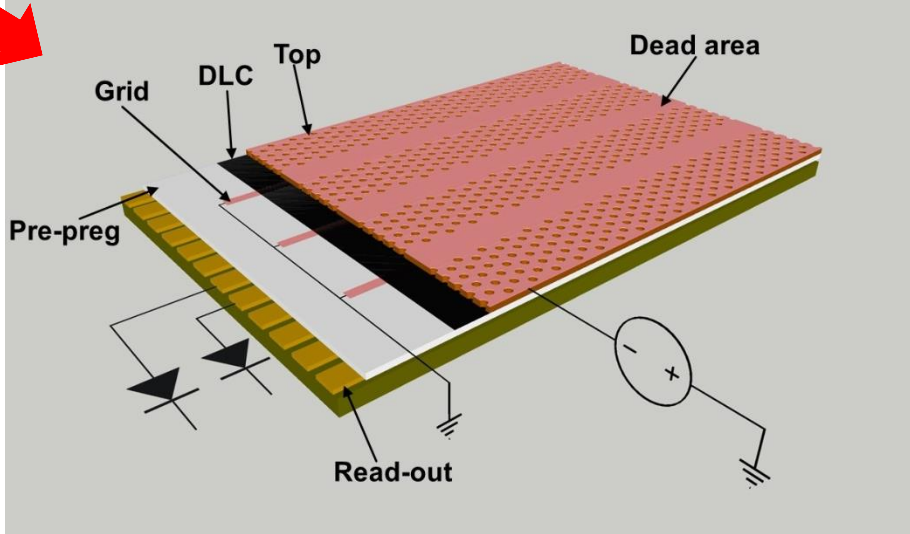
# Detector Layouts

Single resistive layer




Double resistive layer



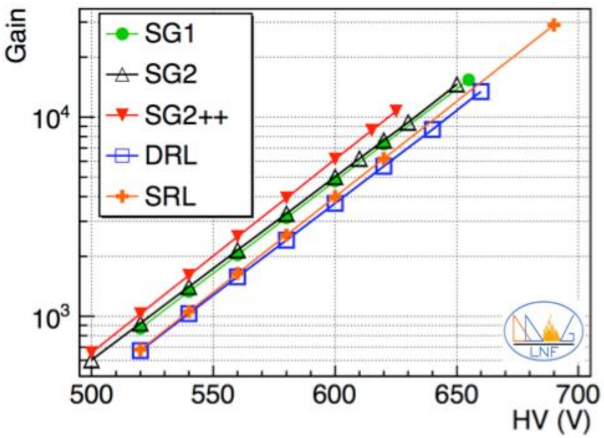



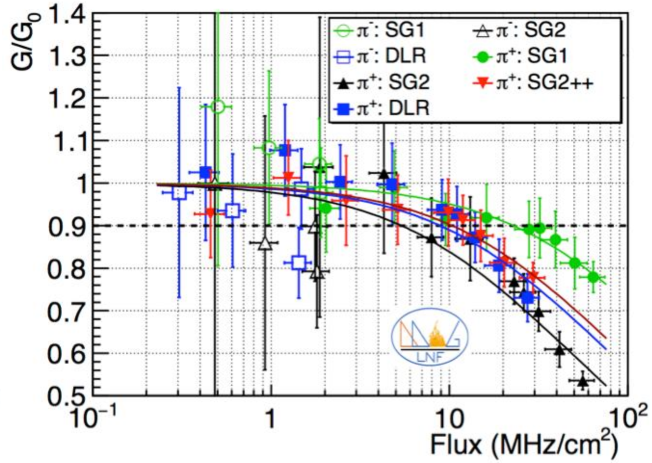

Single resistive layer with dense grid grounding

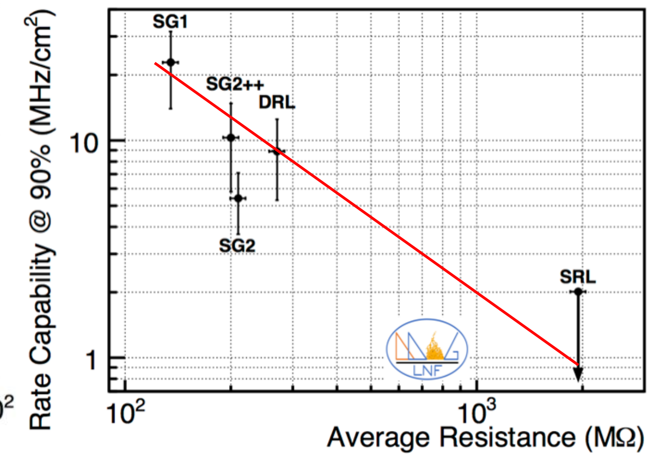
# Detector performance

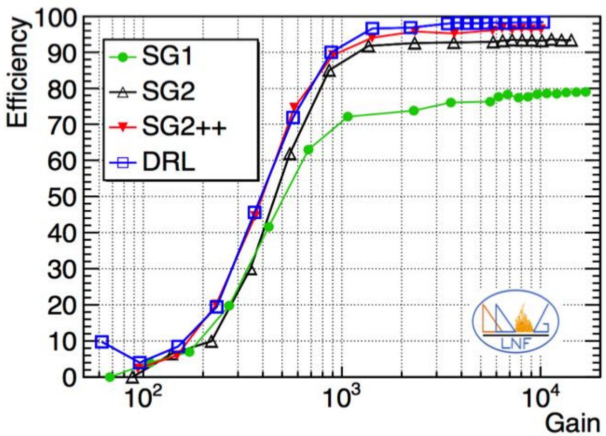
$G \sim 10^4$

Rate capability $\sim 10\ MHz/cm^2$

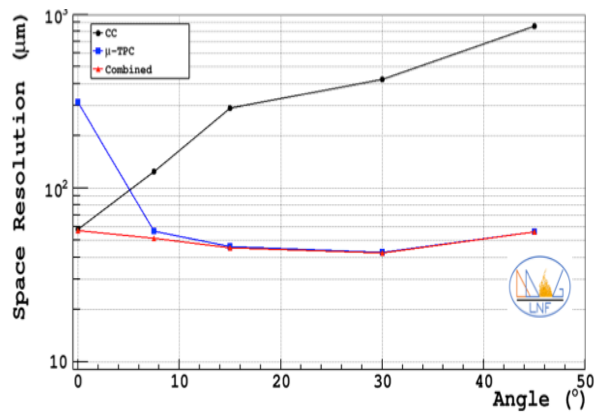


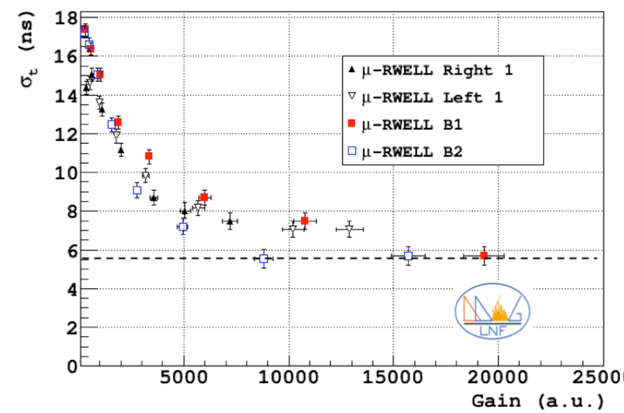




Efficiency $\sim 98\%$



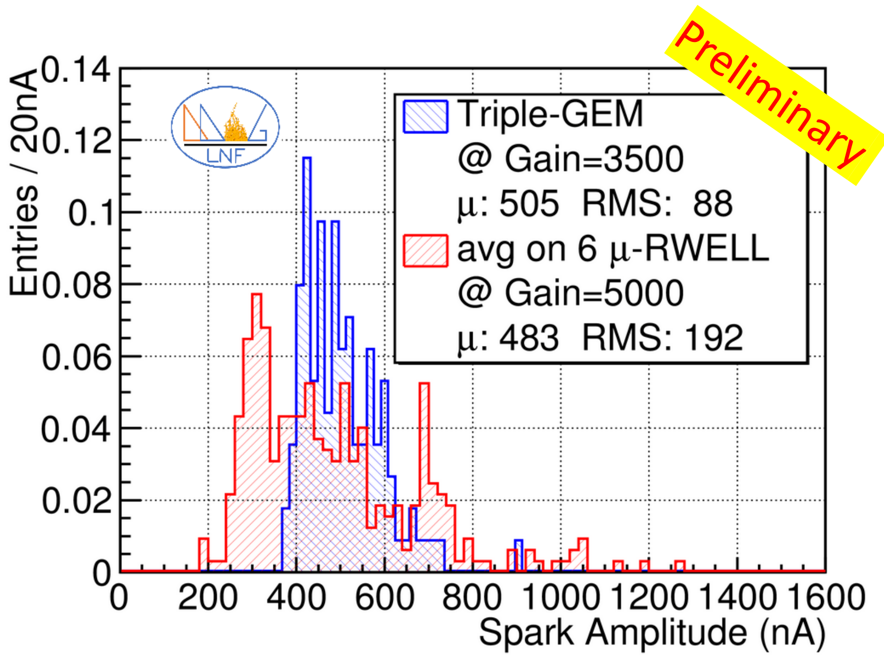

$\sigma_x \sim 40 - 60\ \mu m$

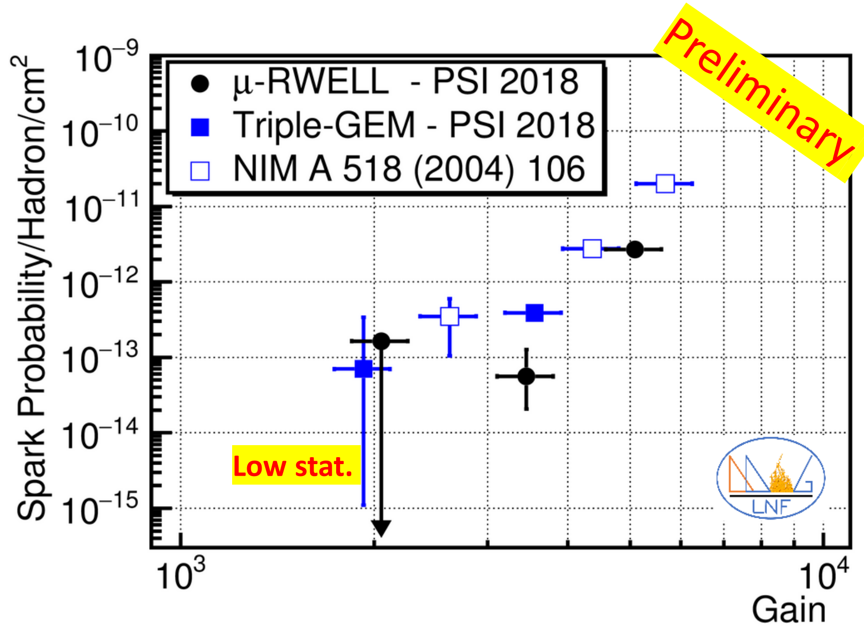



$\sigma_t \sim 5\text{- } 6\ ns$

# Discharge studies @ PSI

A “discharge” has been defined as the **current spike** exceeding the steady current level correlated to the particle flux (~90 MHz on a ~5 $cm^2$ beam spot size).




**The discharge probability for μ-RWELL comes out to be slightly lower than the one measured for GEM.**

**While its discharge amplitude seems to be lower than the one measured for GEM.**

**More extensive test will be done at PSI next autumn**

# What next: the DLC side

Concerning the **DLC** (*Common Project RD51 – USTC, Kobe Univ, CERN, LNF-INFN*):

- **large area simple DLC** foil sputtering at **Be-sputter in Japan**
- **R&D on improved DLC (Zhou Yi, USTC – Hefei - PRC)** → **DLC+Cu**, thick vs thin DLC (small samples, 30x30 $cm^2$ , 120x30 $cm^2$ in 1 year)

- **large area DLC+Cu sputtering** → **mass production required**
- **validation test of DLC** → aging studies, surface discharge

# Validation test of the DLC

Taking as a reference the following requirements:

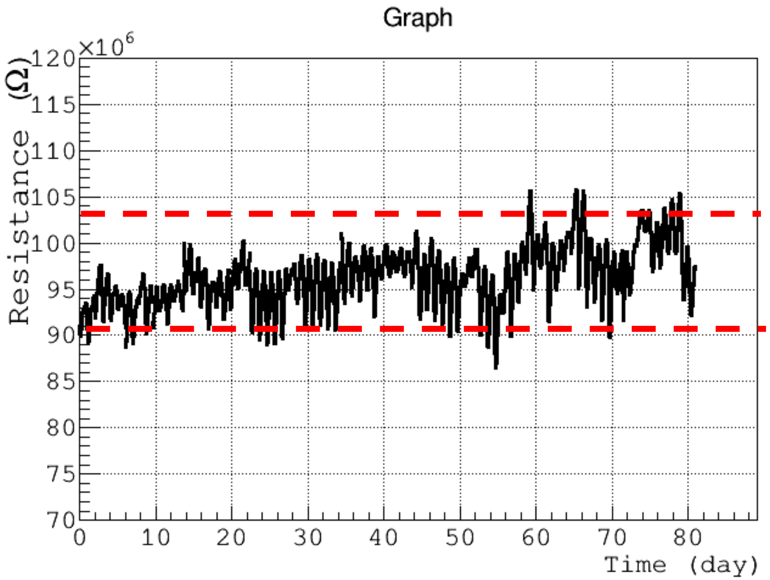
- **rate** up to **1 $MHz/cm^2$ on detector**
- **detector and DLC stability verified** up to **2 $C/cm^2$ (**integrated charge in **10 y** of operation … )

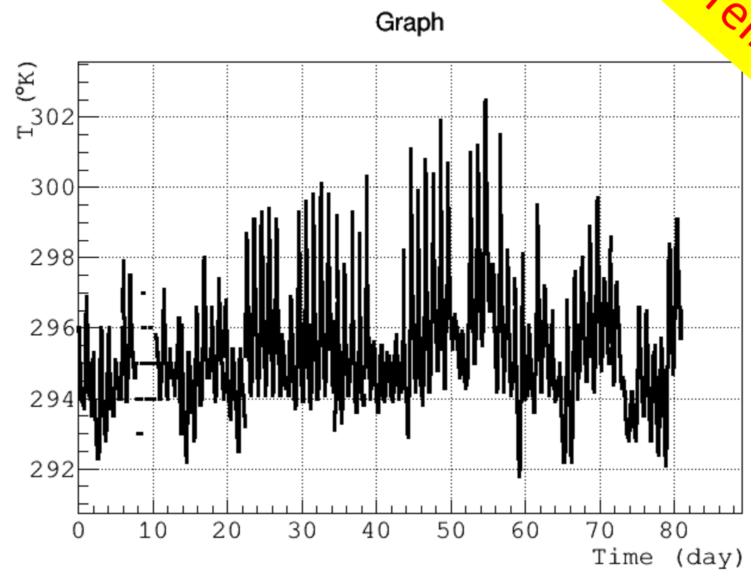
Ongoing tests:

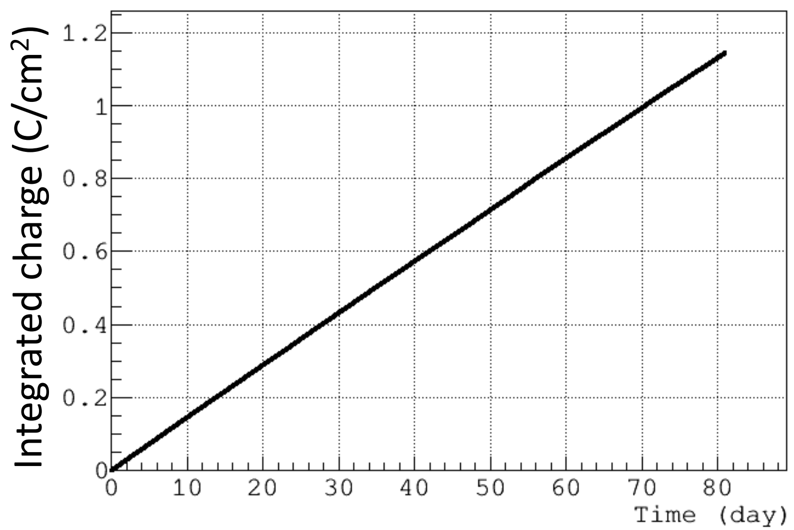
- **long term test of DLC foils** (thin vs thick) **under high current**
- **aging test of detectors** with different radiation (X-ray, gammas, hip)

# DLC studies (III)

preliminary



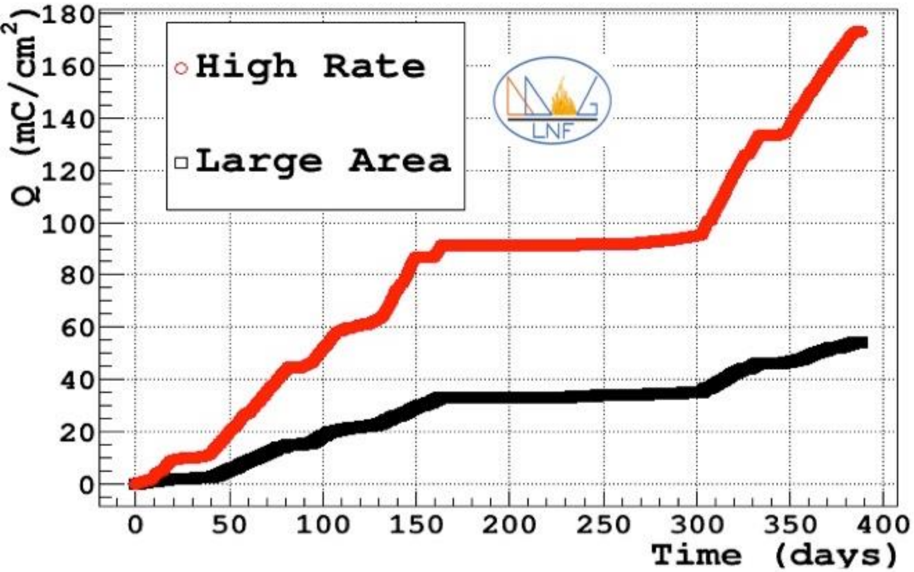



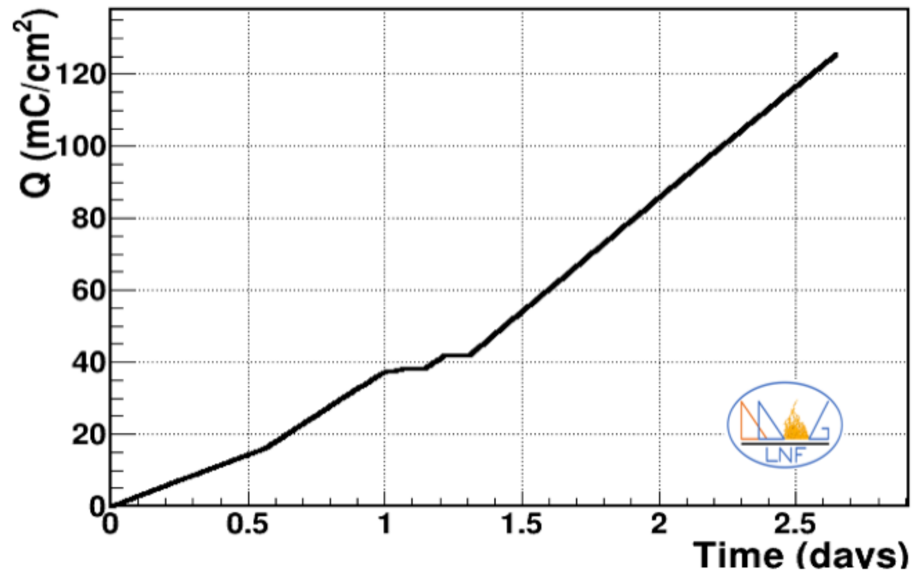

**Goal 2 C/cm2**

# Ageing studies

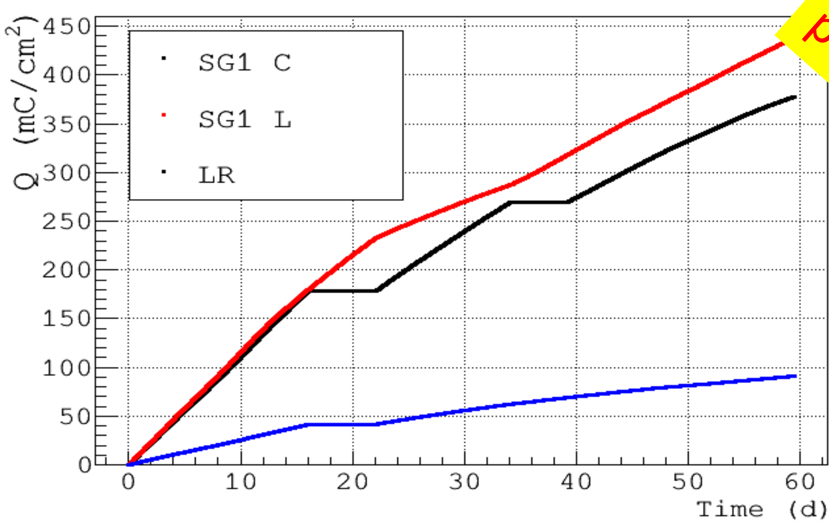
GIF++ - Full area & flux ~ 200 kHz/cm²




TB PSI – beam spot 9 cm² – flux ~ 10 MHz/cm²




X-Ray gun- spot 50 cm² flux ~ 5 MHz/cm²




preliminary

**GOAL:**
**Integrate a charge up to 1-2 C/cm²**

**Slice test of u-RWELLs during RUN3 in the LHCb Muon APPARATUS under discussion**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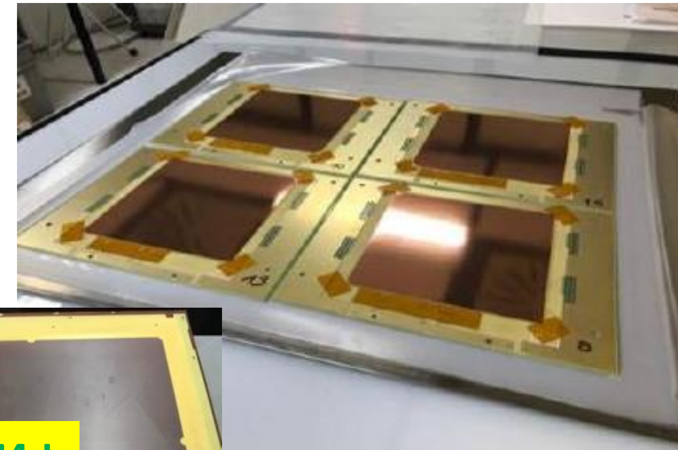
# What next: Technology Transfer

**Production tests @ ELTOS of the low rate version :**

- 10x10 cm$^2$ PCB – (PAD r/o)
- 10x10 cm$^2$ PCB – (strip r/o)




**1.2x0.5m$^2$ μ-RWELL**

**1.9x1.2m$^2$ μ-RWELL**

Prototypes proposed for CMS phase-2 muon upgrade

**Production Tests @ ELTOS, large area detectors (w/CMS):**

- 1.2x0.5m$^2$ with strip r/o
- 1.9x1.2m$^2$ with strip r/o - (**w/PCB splicing**)

kapton etching done @ CERN

# Future plans @ ELTOS for the 2019-2020

Production tests of **HR – layouts** (SG2++ type):

- n. **2-3 batches** of **100x100 $mm^2$ active area** (w/pad readout)
- n. **1-2 batches** of medium-large **size 300x250 ÷ 600x250 $mm^2$** (w/pad readout) → for the slice test of **LHCb-muon**
- **…**

The ELTOS is also involved in the ATTRACT project (see Gigi presentation)

# SUMMARY

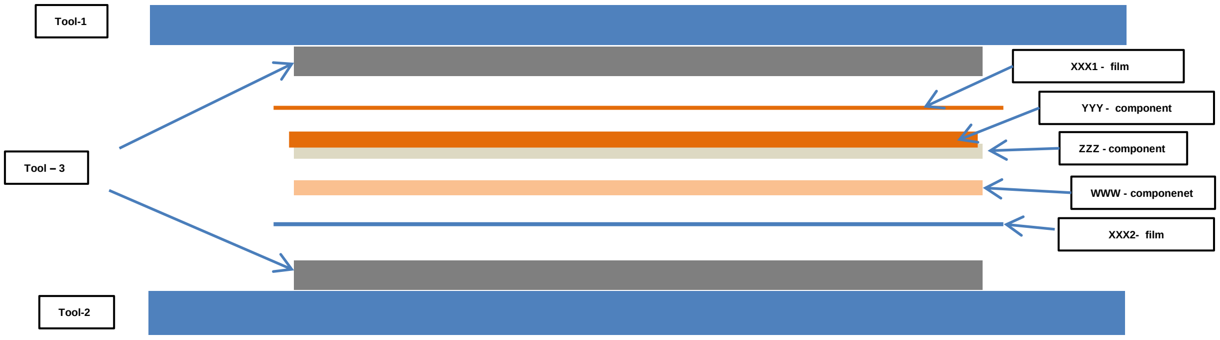
- The R&D phase on μ-RWELL is almost completed
- Discharges & long term stability studies under heavy irradiation:
  - PSI TB in sept/oct 2019
  - slice test > 2020 with detectors installed on the LHCb Muon apparatus (under discussion)
- Technology Transfer to ELTOS (+ …) is on-going
- Long-term stability studies of DLC started in the framework of CP-RD51
- Large area DLC+Cu sputtering (Hefei Collaboration) crucial for the high rate version

# Spares Slides

# The micro-RWELL manufacturing at ELTOS

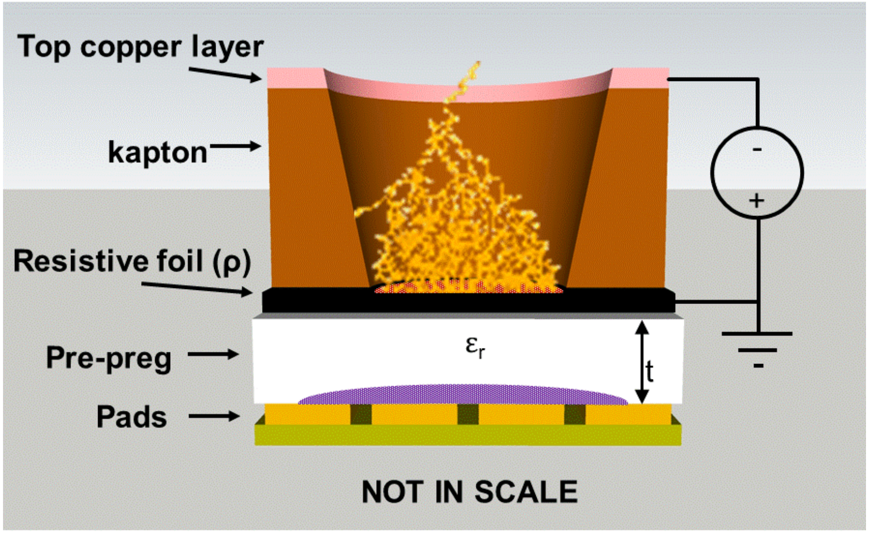
At ELTOS they do the **coupling of the DLC-foil with the readout PCB** (produced by them).

The **max size of the μ-RWELL-PCB** that the press could allocate is about **600x700 mm$^2$. Up to 4 of such PCBs** can be manufactured at the same time or **equivalently 16 small size (100x100 mm$^2$ active area**).




# Principle of operation

Applying a suitable voltage between the top Cu-layer and the DLC the "WELL" acts as a multiplication channel for the ionization produced in the drift gas gap.



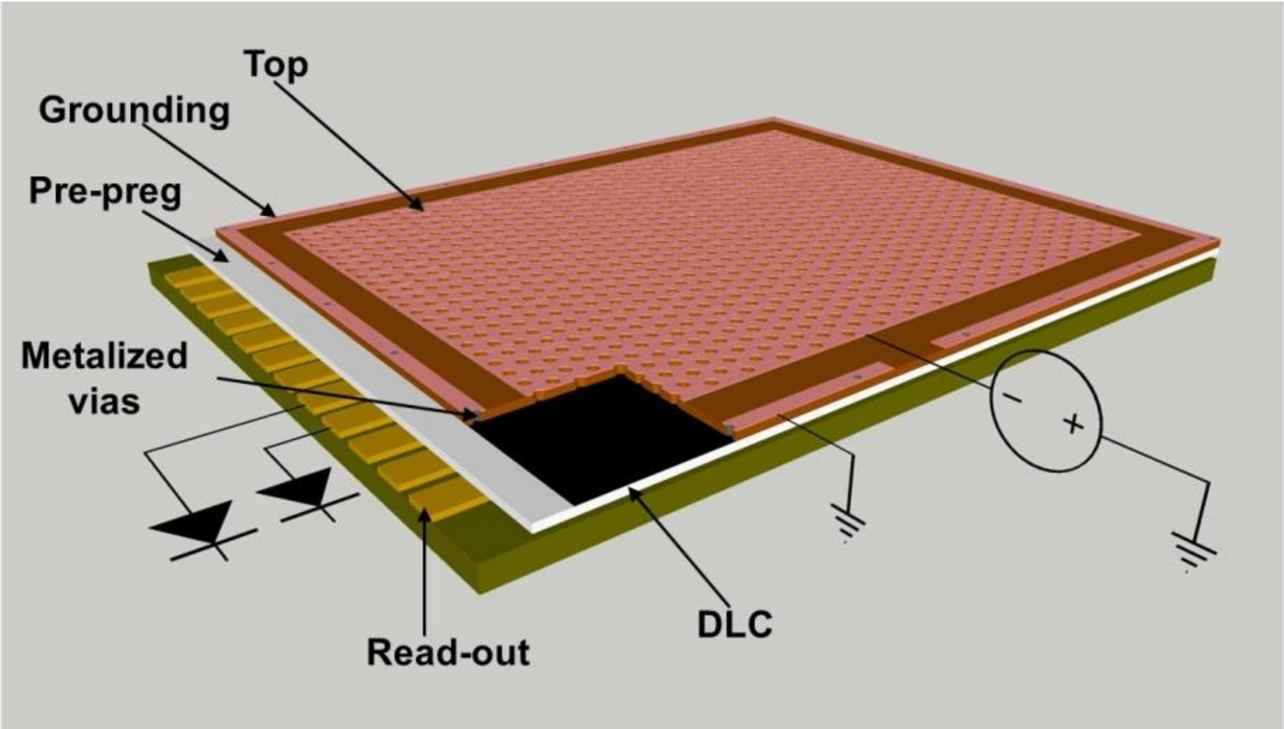

The charge induced on the resistive layer is spread with a *time constant*, $\tau \sim \rho \times C$ [*M.S. Dixit et al., NIMA 566 (2006) 281*]:

- the DLC surface resistivity → ρ
- the capacitance per unit area, which depends on the distance between the resistive foil and the pad/strip readout plane → t
- the dielectric constant of the insulating medium → $\varepsilon_r$

$$C = \varepsilon_0 \times \varepsilon_r \times \frac{S}{t}$$

- The main effect of the introduction of the resistive stage is the suppression of the transition from streamer to spark, with a consequent reduction of the spark-amplitude
- As a drawback, the capability to stand high particle fluxes is reduced, but appropriate grounding schemes of the resistive layer solves this problem (*see High Rate layouts*)

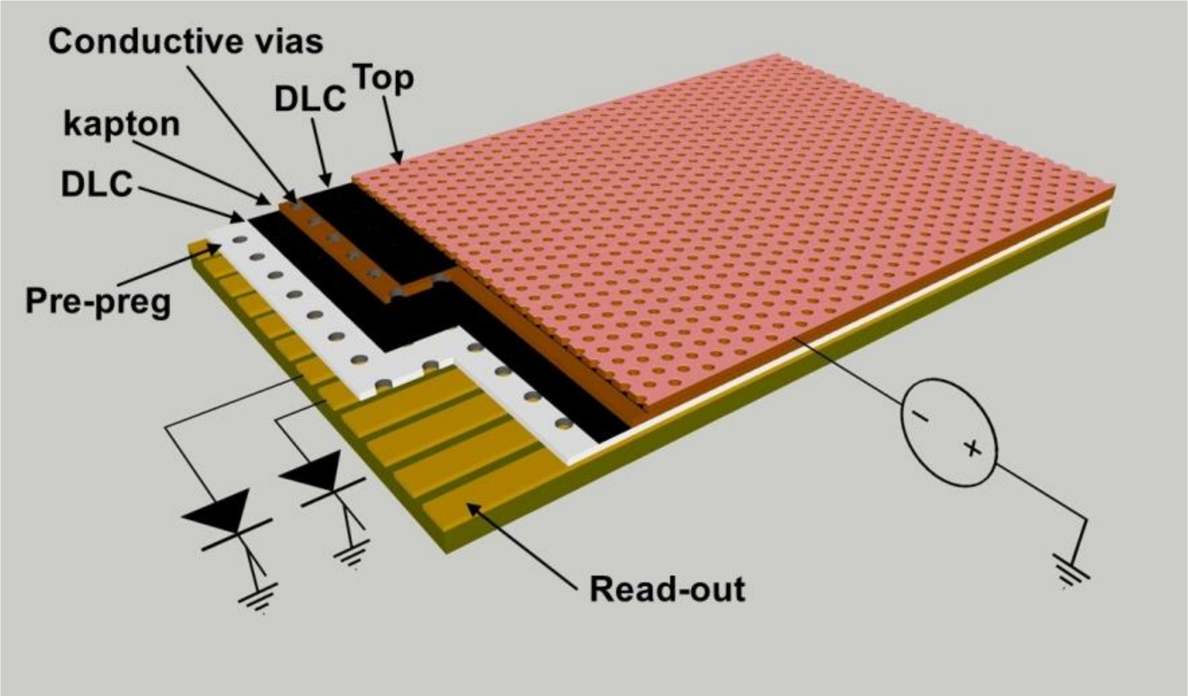
# The Low Rate Layout




**Single Resistive Layer (SRL):** a simple **2-D current evacuation** scheme based on a **single resistive layer** with a conductive **grounding all around the perimeter** of the active area.

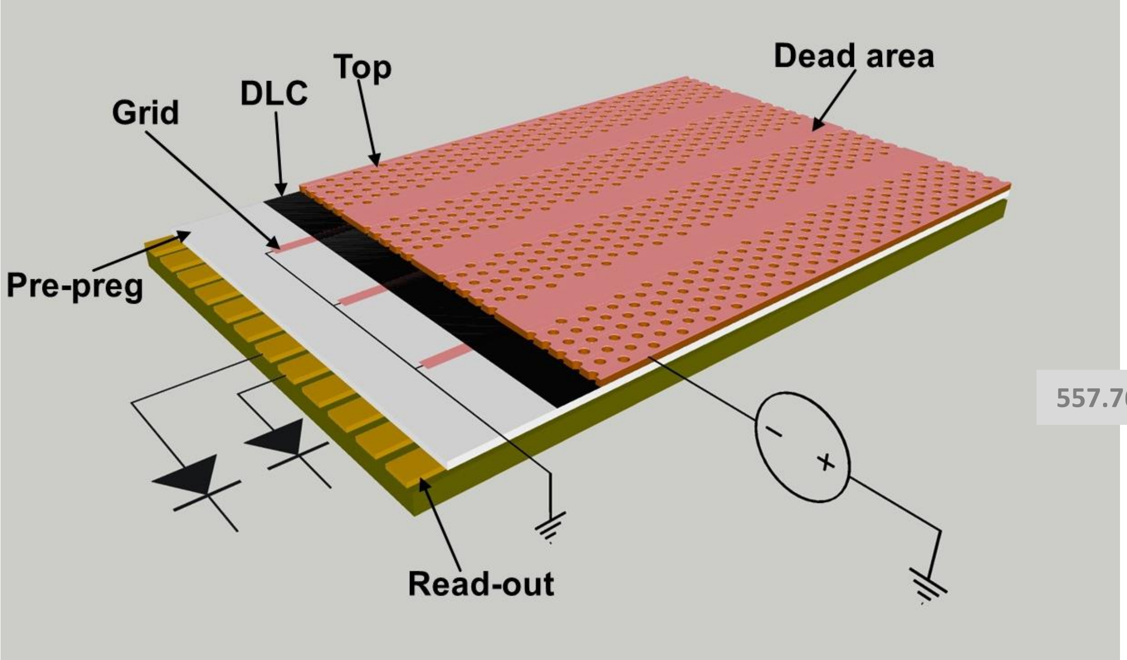
For **large area detectors** the **path of the current towards the ground connection** could be large and strongly dependent on the particle incidence point, giving rise to **detector response inhomogeneity → limited rate capability.**

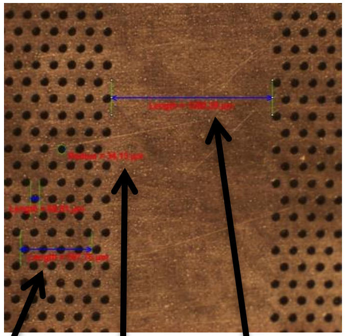
# HR layouts: the double-resistive laye




**Double Resistive Layer (DRL): 3-D current evacuation scheme** based on **two stacked resistive layers** connected through a **matrix of conductive vias** and **grounded through a further matrix of vias to the underlying readout** electrodes. The **pitch of the vias** can be done with a density **less than 1/cm$^2$**.

# HR layouts: the Silver grid




The **SG** is a **simplified HR scheme** based on a **Single Resistive layer** with a **2-D grounding** by means a **conductive strip lines grid** realized on the DLC layer.
The **conductive grid lines** can be screen-printed or **etched** by photo-lithography (*using the DLC+Cu deposition technology developed at USTC – Hefei*).

The **conductive grid** can **induce instabilities due to discharges over the DLC surface**, thus requiring for the **introduction of a small dead zone** on the amplification stage.