GRASS Padova 2019

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Electronic hardware and software development for EPR squeezer

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on behalf of the EPR squeezing group

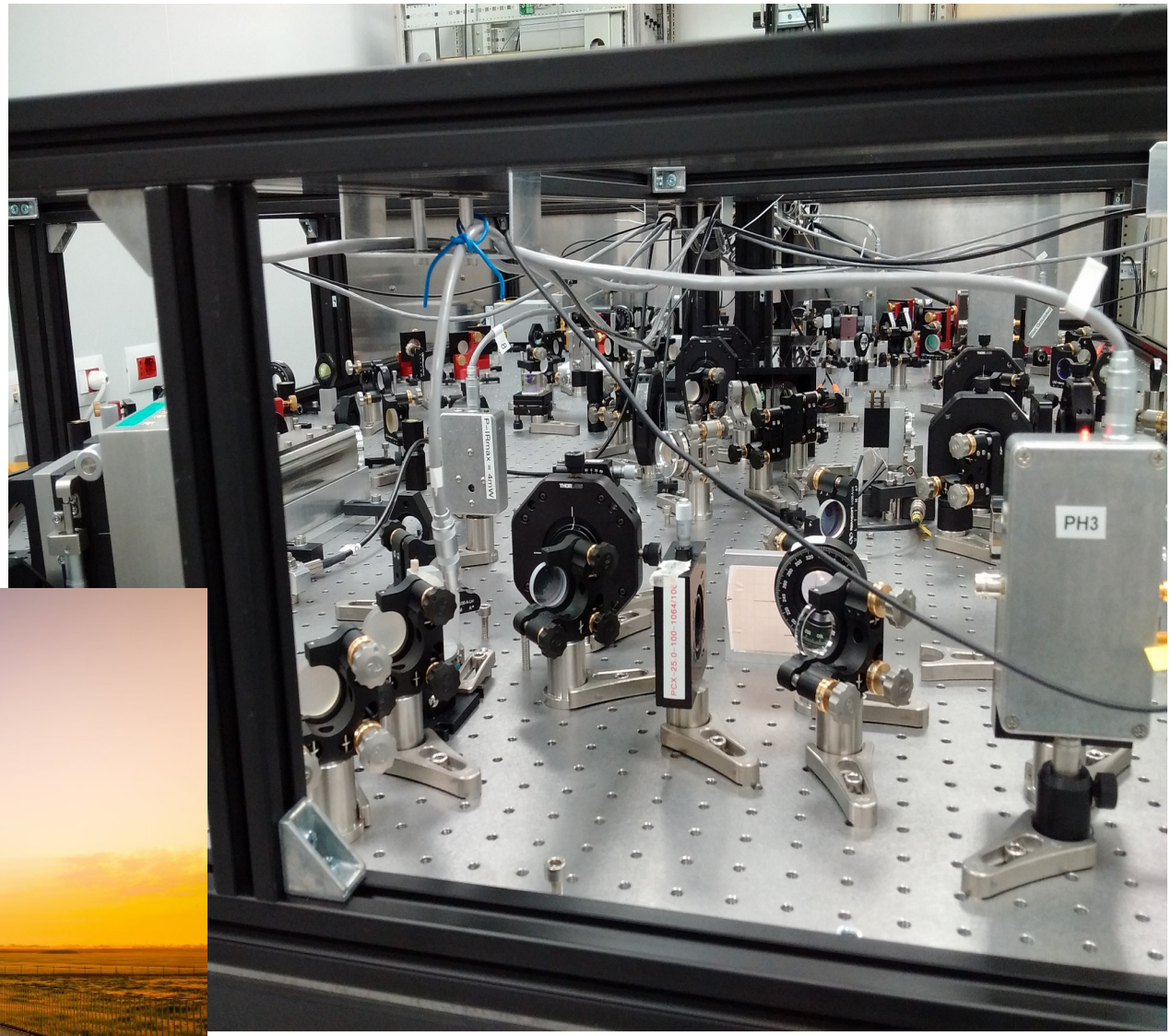
VIRGO

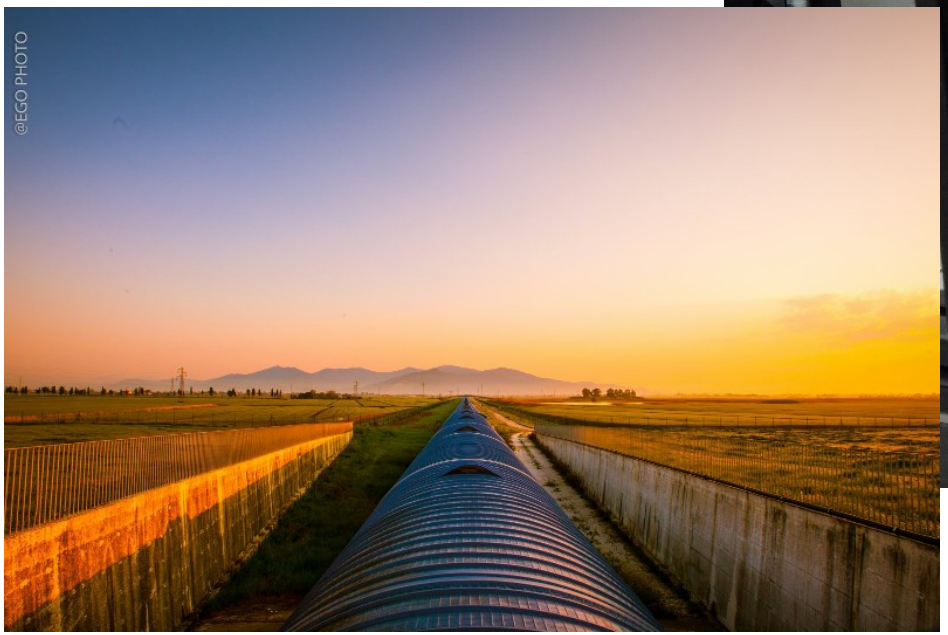
INFN Sez. di Perugia

Squeezing group

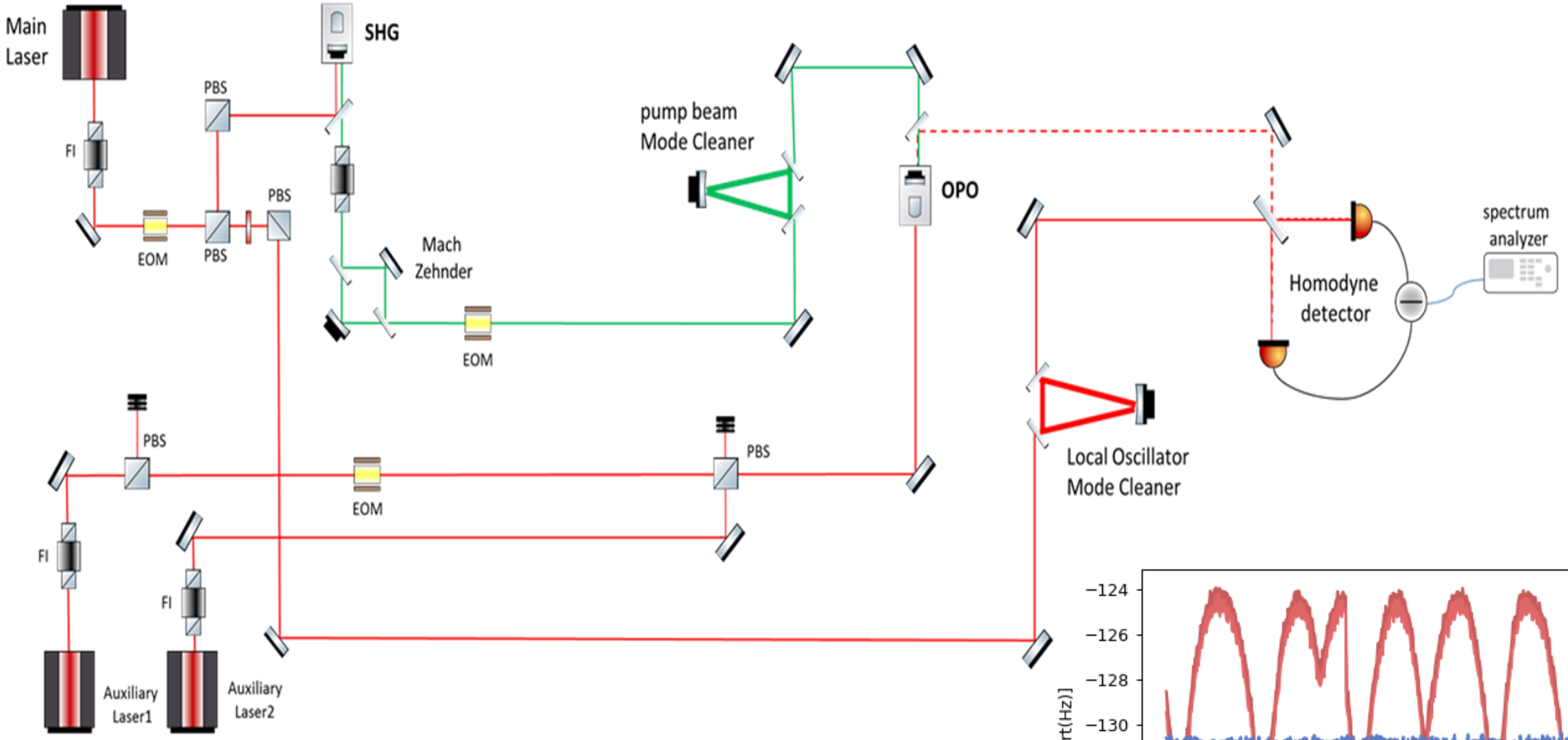
INFN
- Genova
- Napoli
- Padova/LNL
- Perugia
- Roma 1
- Roma 2

APC/CNRS Paris





Starting point



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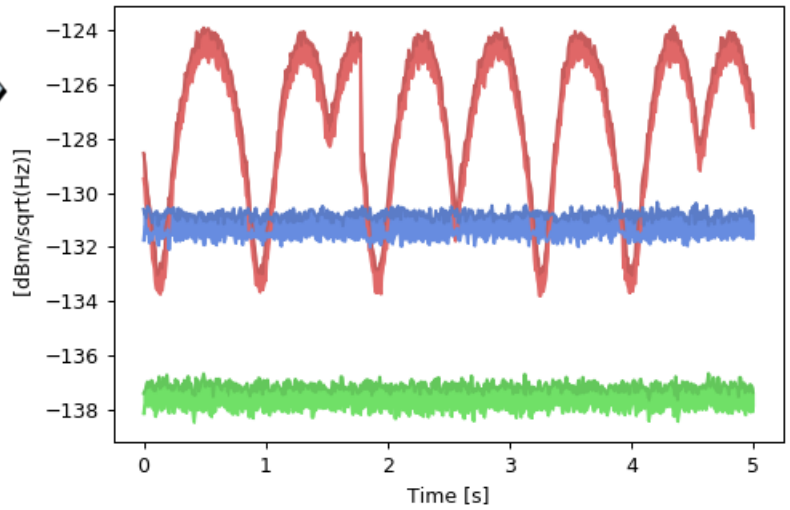
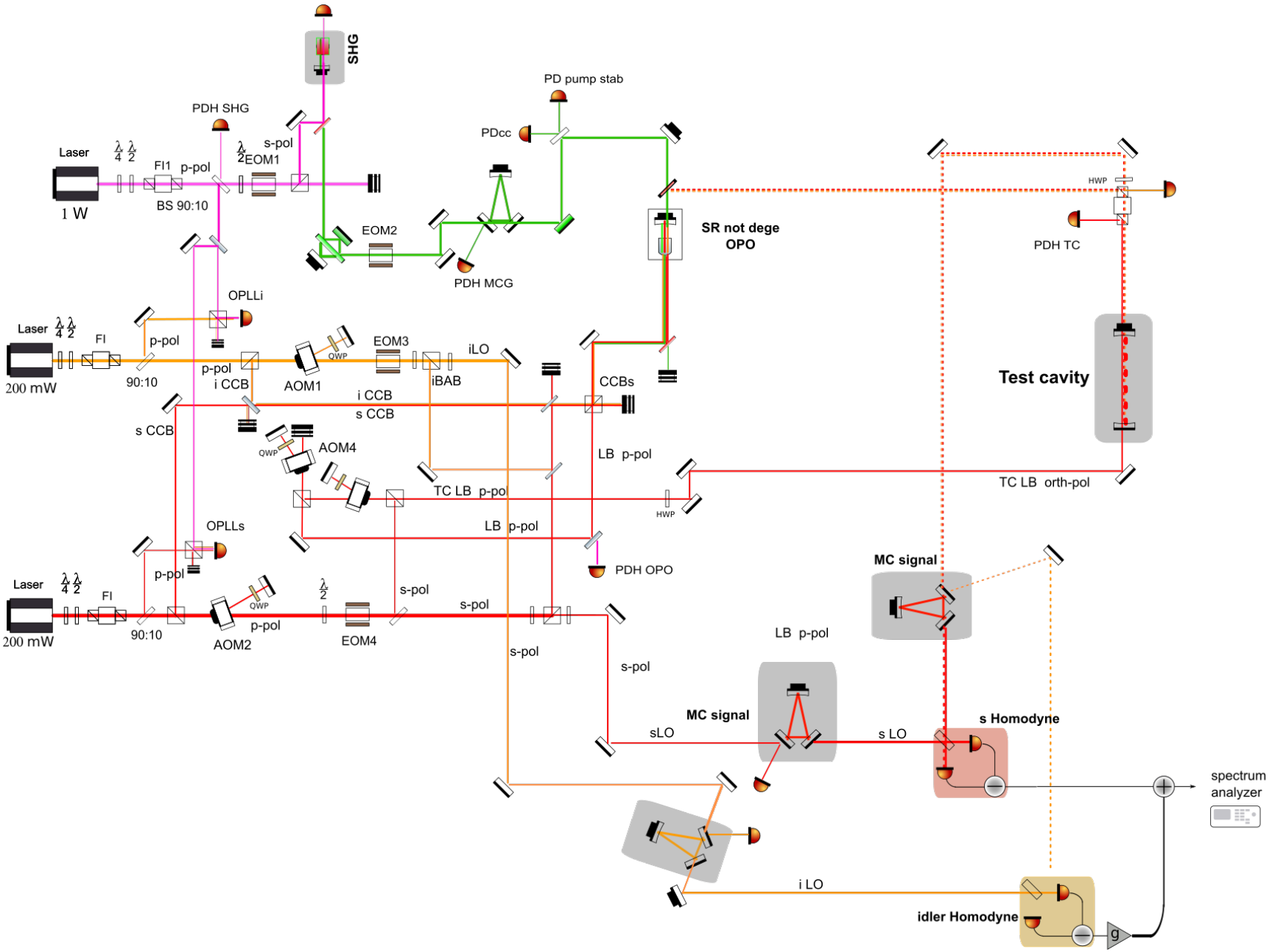


Squeezing

Goals

- Lower the noise
- Maximize Quality of Service of the subsystem
- Shorten time of complex operation on the controls (tuning)
- Minimize necessary human interaction with the subsystem
- Keep it compatible with Virgo

EPR conceptual design

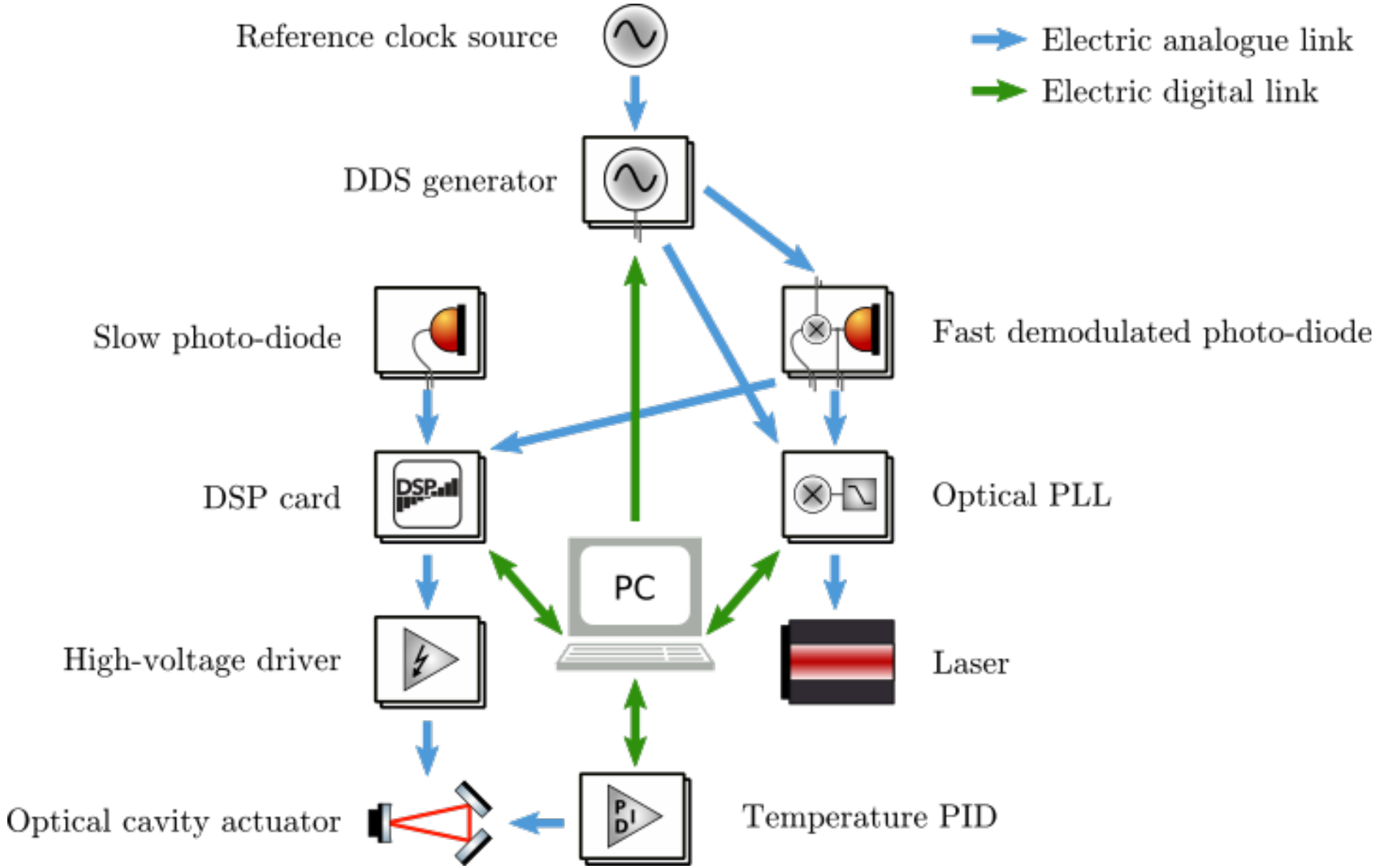


Design requirements

Feedback loops

- 2x PLL
- 2x non-linear crystal cavity longitudinal lock
- 1x Mach-Zender interferometer
- 4x optical cavity longitudinal lock
- 1x coherent control
- 14x DDS channels
- 2x temperature control

Hardware system architecture



Improvements in electronic equipment

- Reliable reference clock source
- High voltage drivers for piezoelectric stacks
- Fast photo-detectors
- Homodyne detector
- Lock acquisition stability improvement and automation

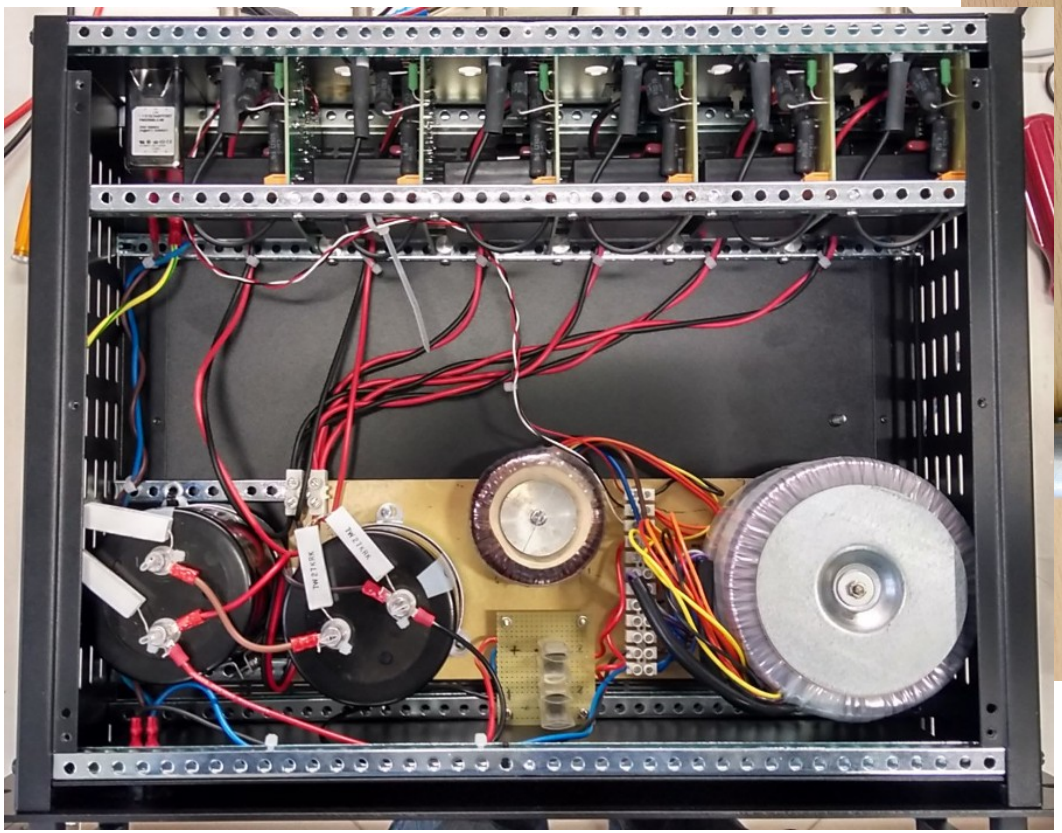
500MHz reference clock source

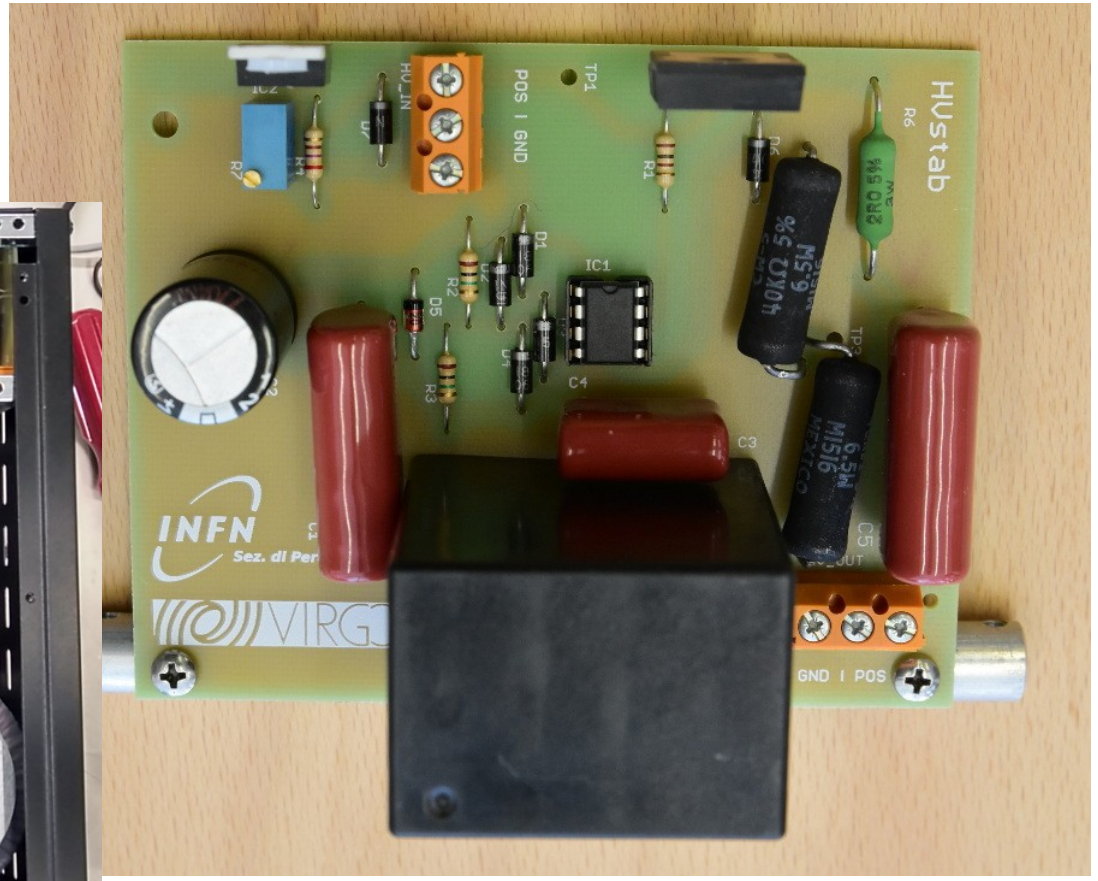
- VCO based, PLL stabilized clock source
- Parameters managed by a micro-controller
- PLL-lock status is monitored by the micro-controller to react in case of failure thus increase reliability

High voltage drivers

Purpose of modifications

- Lowering piezo driver output noise by power supply modification
- Eliminating 50Hz power line oscillation
- Decrease filtering capacity

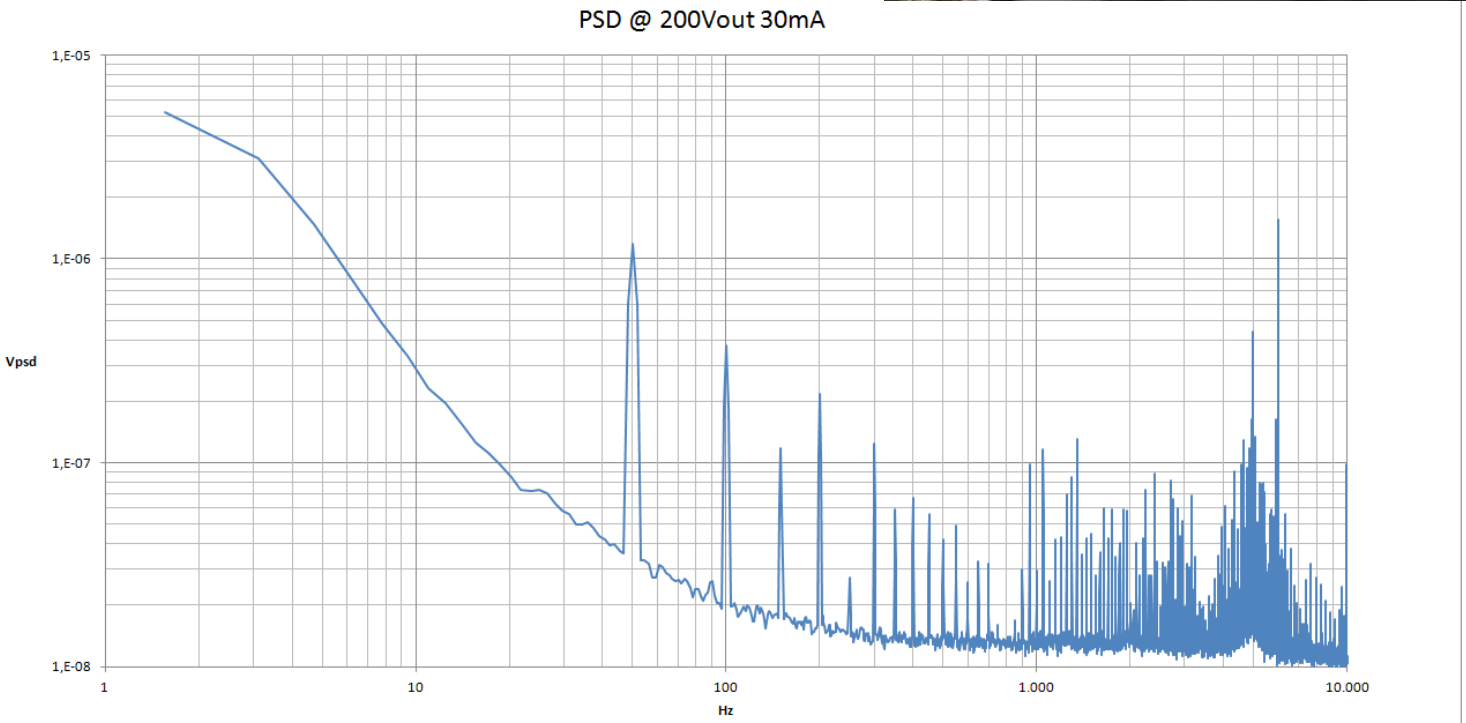




High voltage drivers

E_{out} = 3uV/sqrt(Hz)
@ 200Hz corner

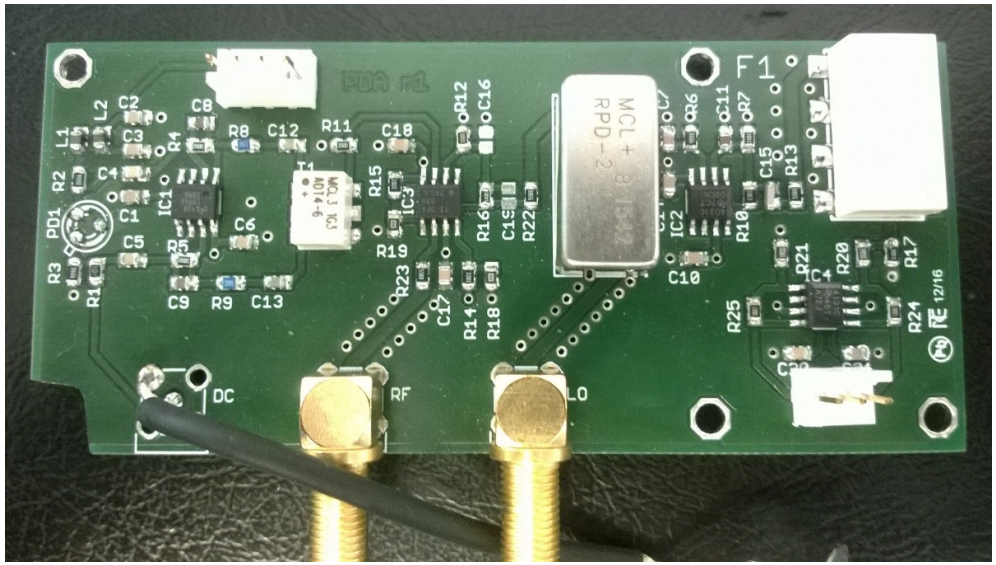
Power supply noise

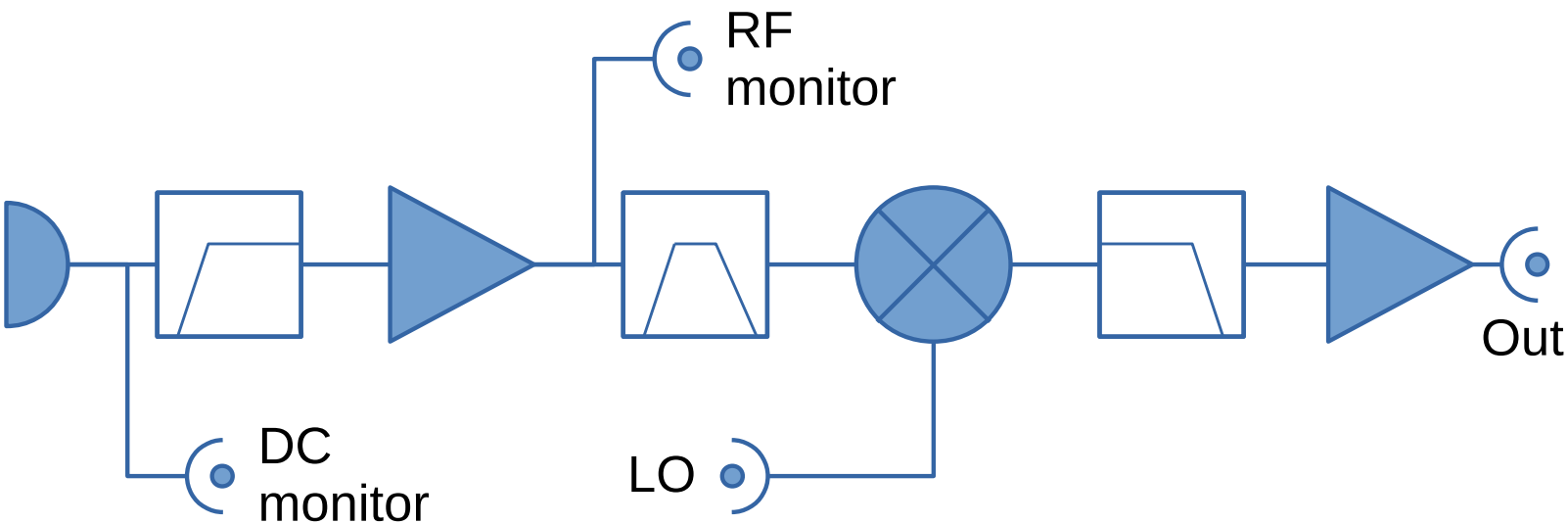


V_{RMS} = 4,85uV

Fast photo-detectors

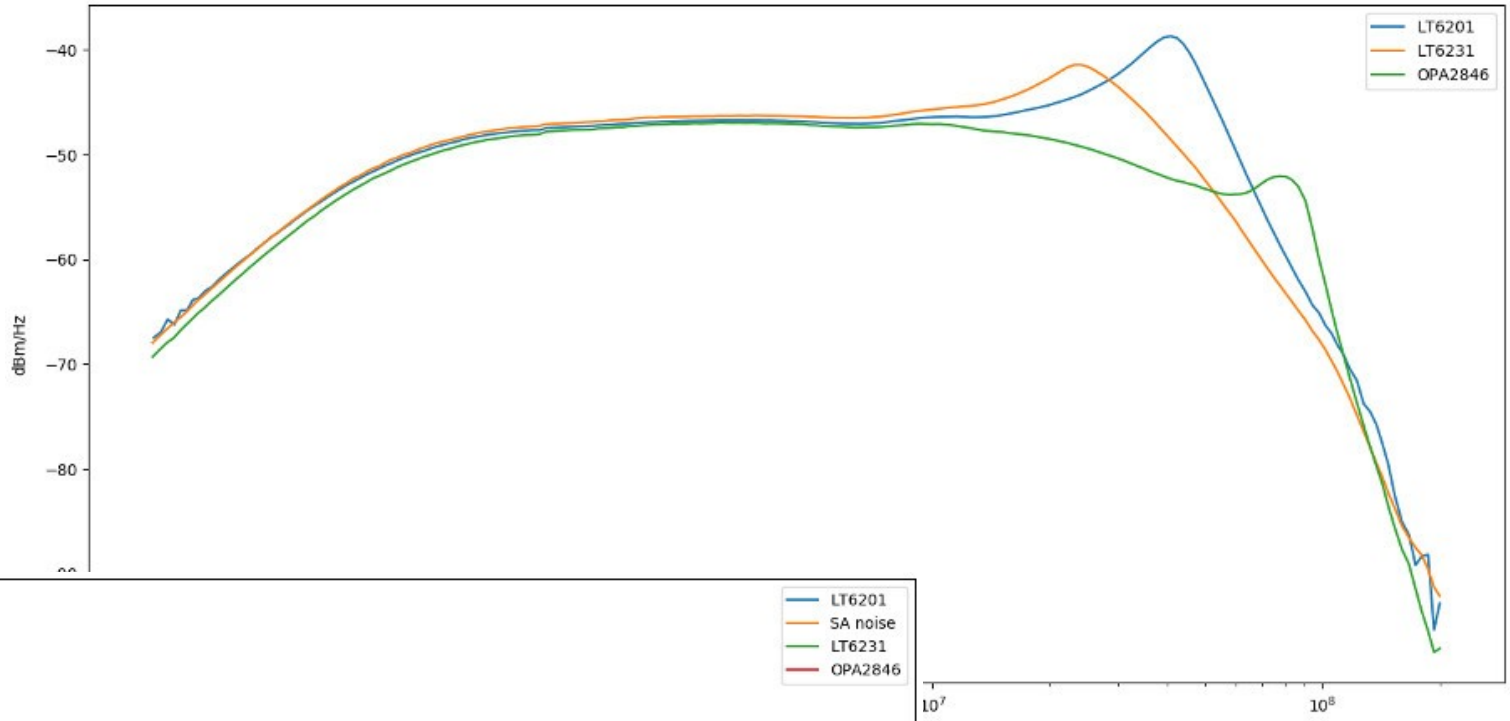
- On-board demodulation
- Differential outputs in stead of unipolar
- Bandwidth:
  80MHz for d=0,5mm
  120MHz for d=0,3mm



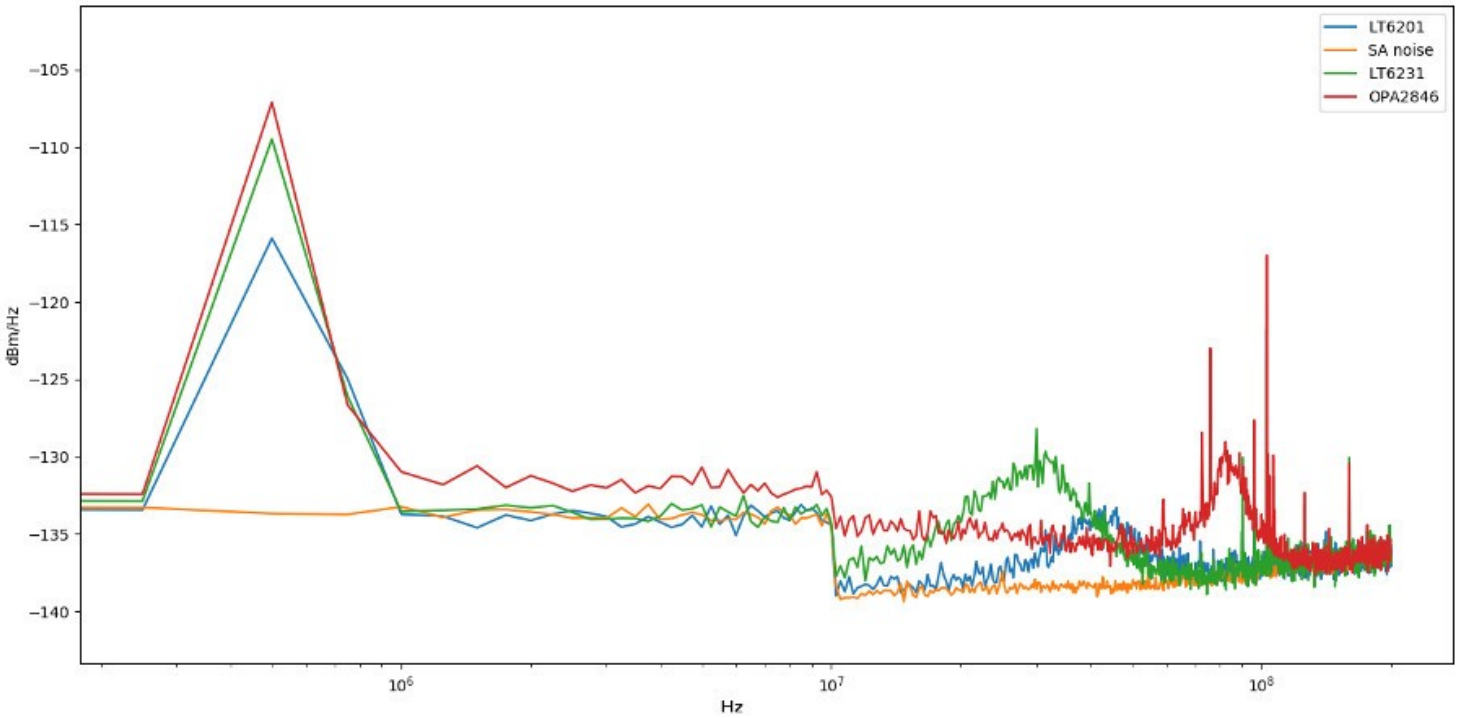


Fast photo-detectors

RF bandwidth



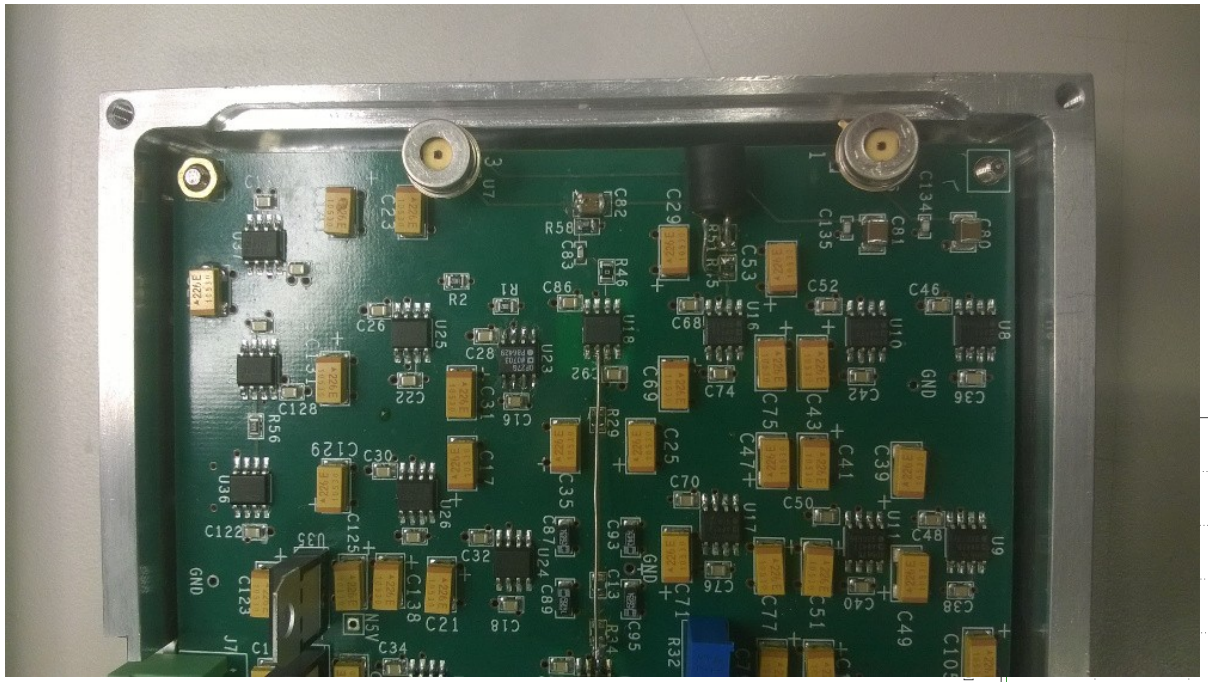
RF monitor output noise



Measurements with:
Hamamatsu G8376-05
d=0,5mm

Homodyne detector

- Improvements in the electric circuit design
- Improved mechanical stability
- Improved noise characteristics
- Measured 82dB of CMRR (at 270Hz)



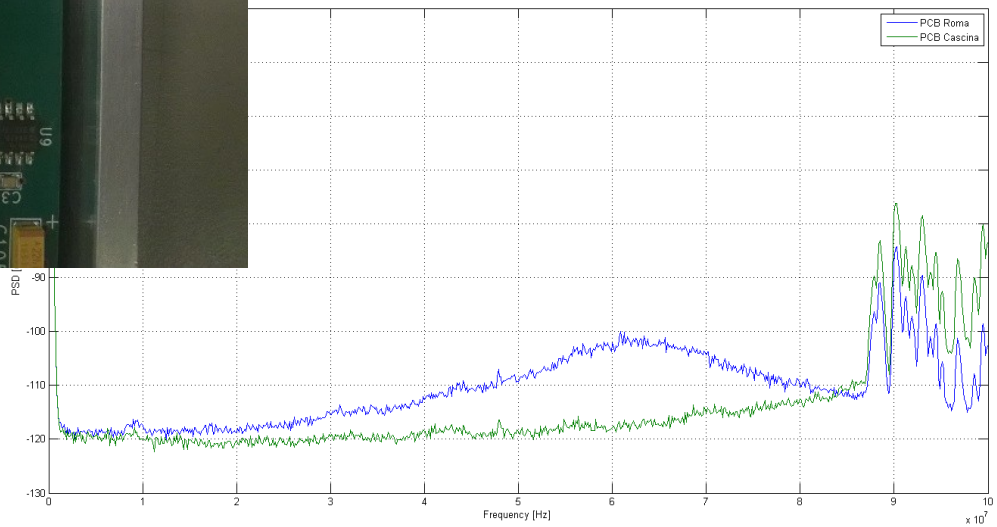
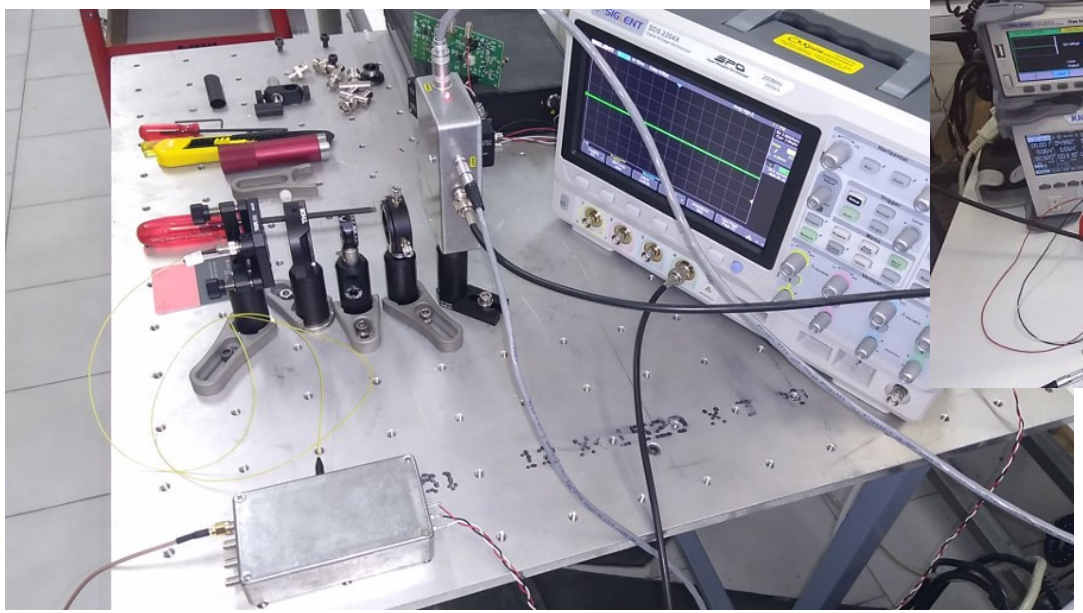
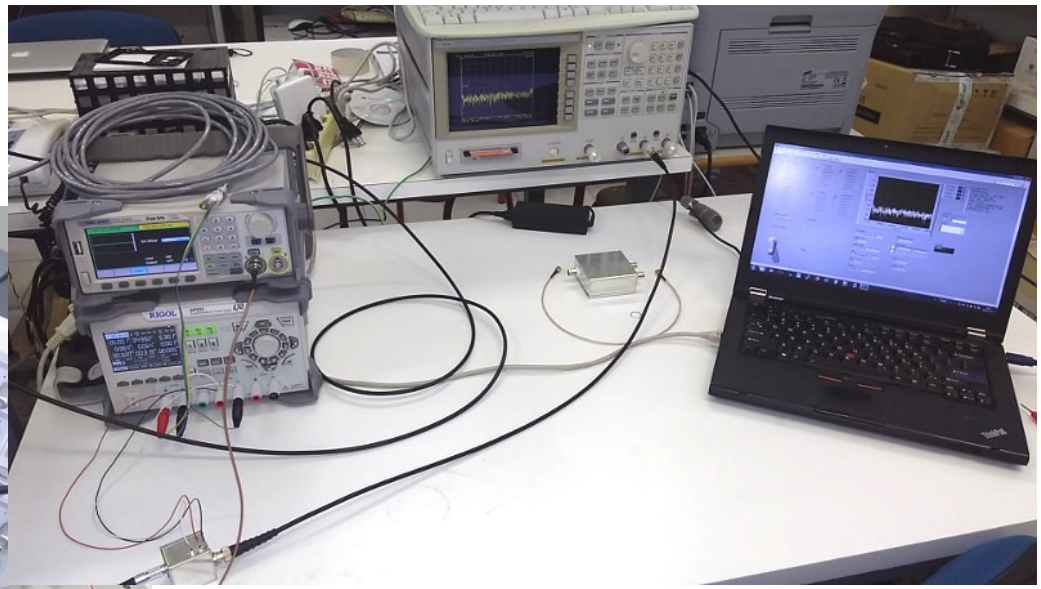


Photo detector testbench

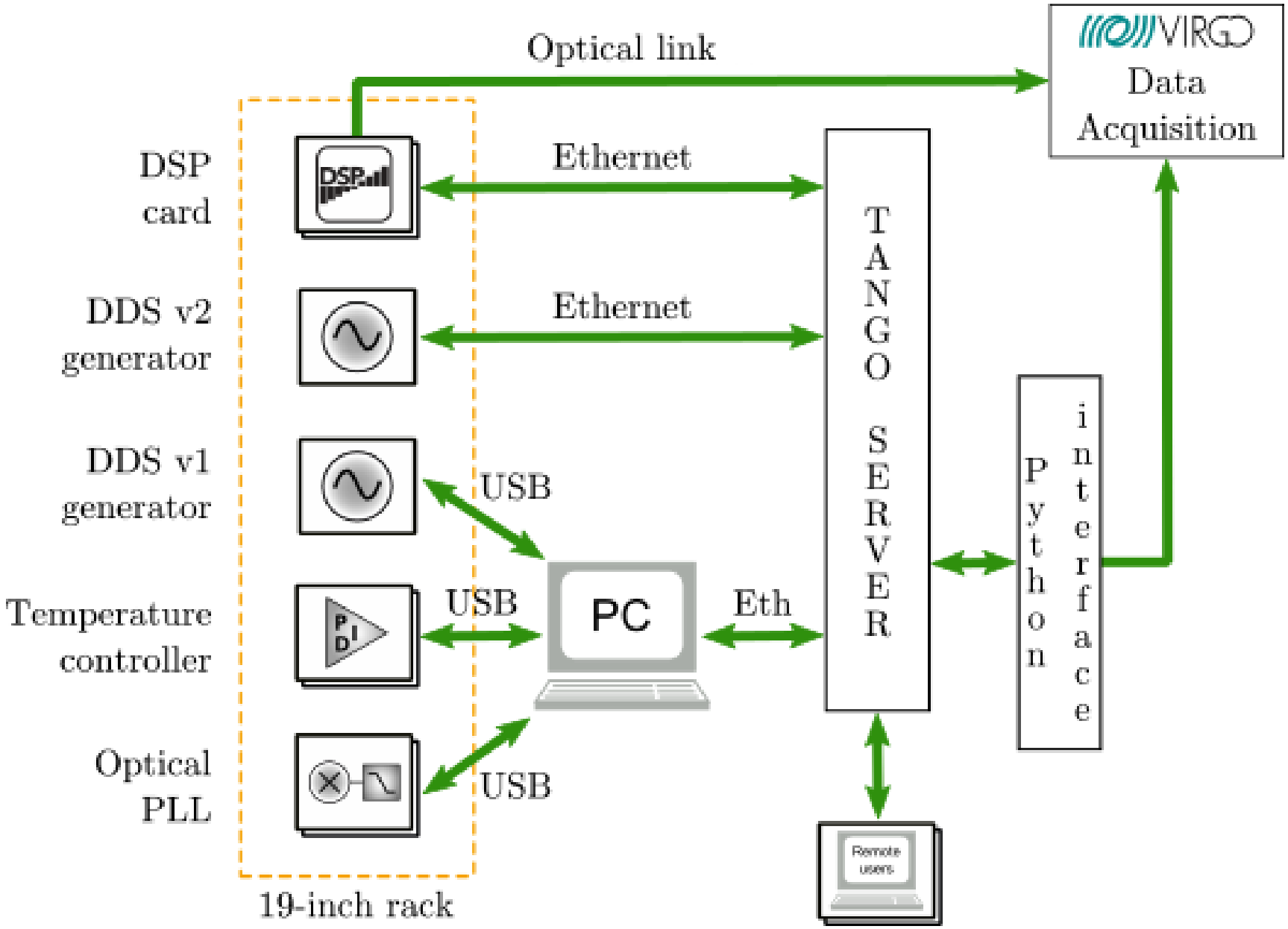
Components:

- Amplitude modulated laser up to 300MHz
- Optical bench + optical components
- Spectrum/Network analyzer
- Dedicated piece of software for quick spectra visualization and comparison





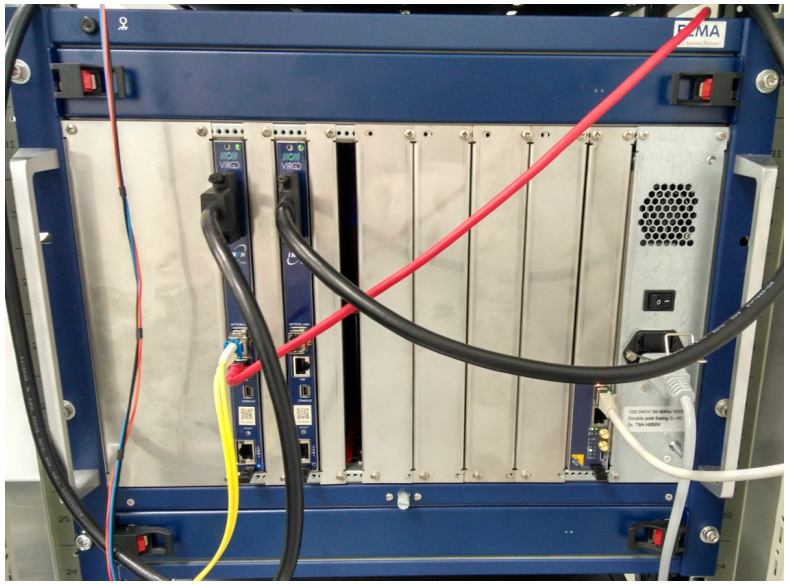
Software system architecture



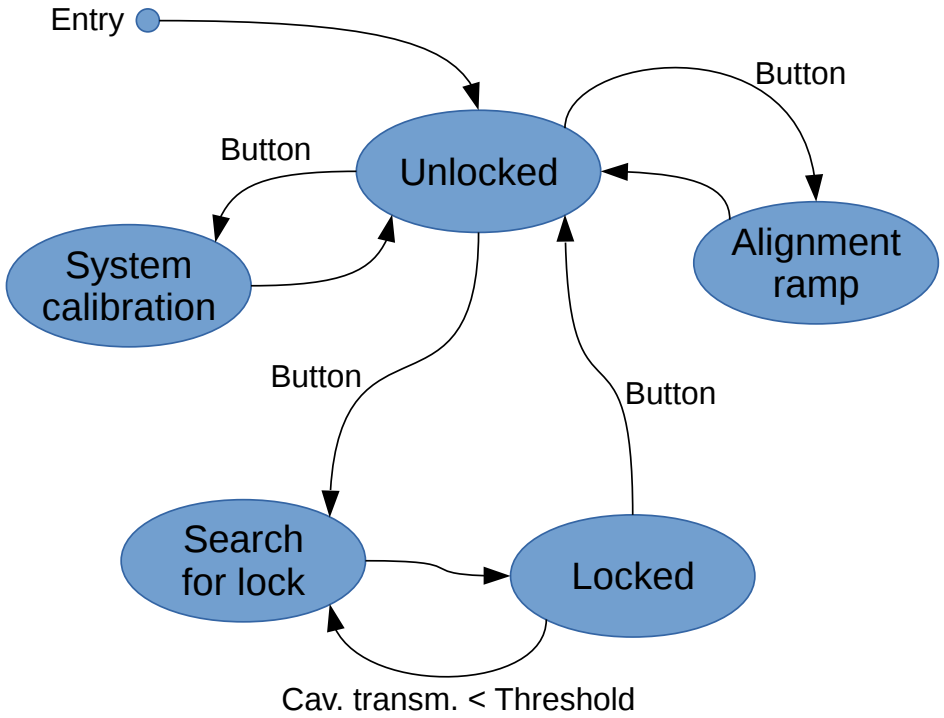
Automation

Development platform features:

- DSP accelerated DAQ system
- supporting Finite State Machines (FSM) implementation



Single cavity lock logic scheme

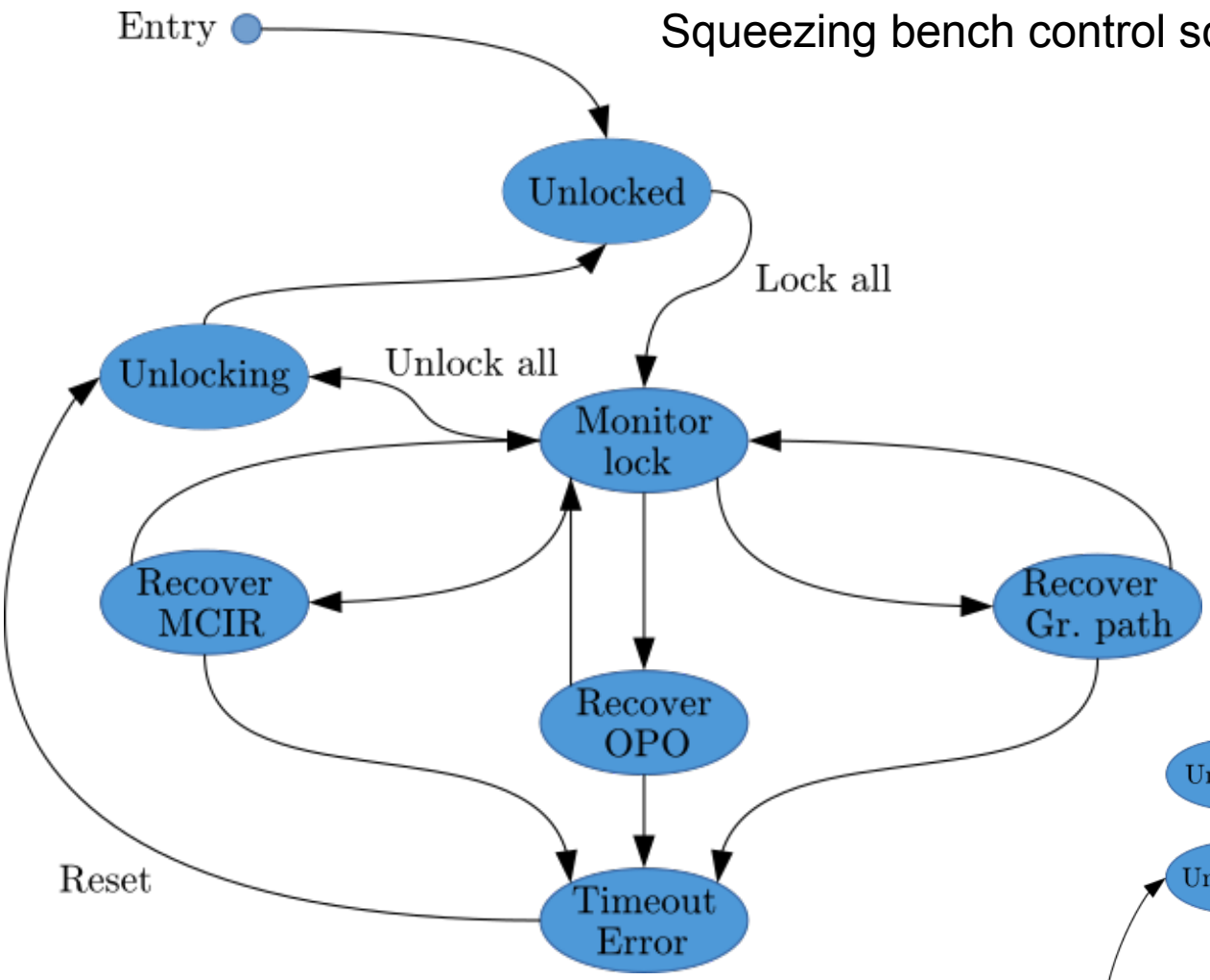


Requirements

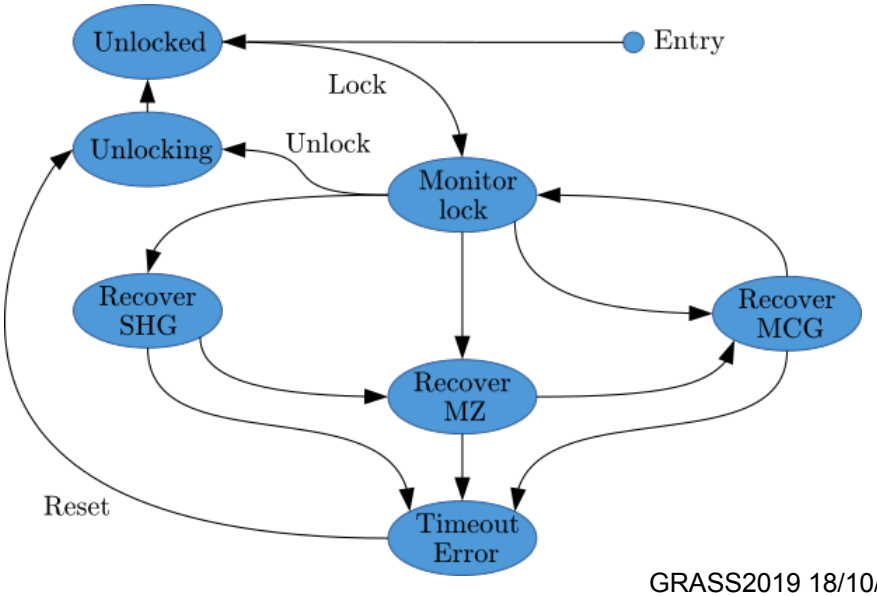
- High lock stability
- User friendly and autonomous operation

Automation

Squeezing bench control scheme

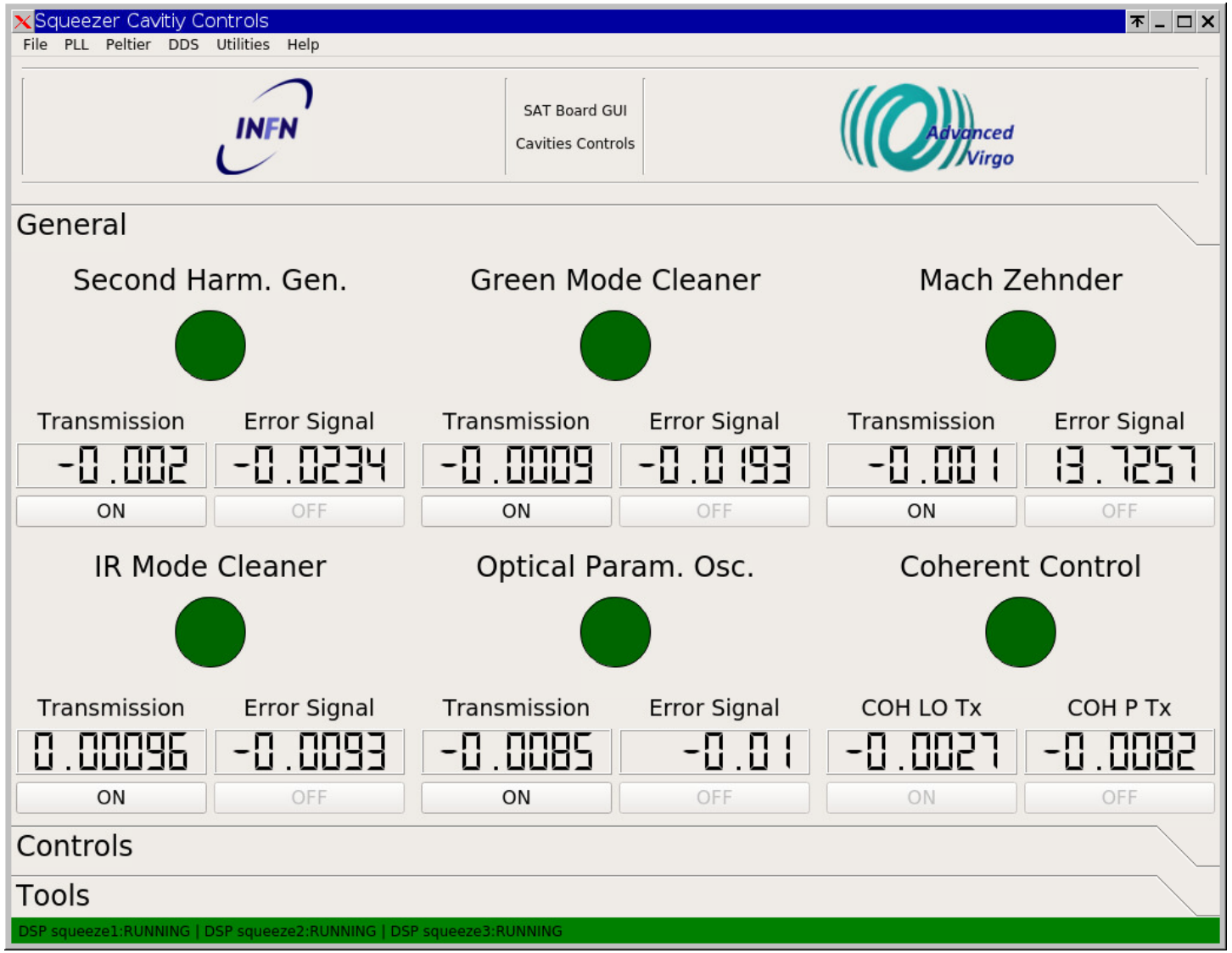


Green patch control scheme



Slow logic and GUI

Bench automation is implemented in python together with GUI.



Main FSM loop execution time is compatible with Virgo automation tool =1s

Summary

- We introduced monitored reference clock oscillator
- We implemented hardware modifications in the high-voltage section of the control system
- We built the test-bench where we upgraded of our photo-detectors
- We improved the homodyne detector
- We developed new code implementing the logic of the automated system of bench control

Next steps:

- Multiply our devices to satisfy the requirements of the EPR optical project
- Extend the FSM logic on the additional hardware
- Commissioning of the software
- Measurement of the QoS

*Bawaj M.[1], De Laurentis M.[2], Di Pace S.[3,4], Gennai A.[5], Khan I.[6], Majorana E.[3,4], Naticchioni L.[3,4], Nguyen C.[7], Passuello D.[5], Sequino V.[8], Sorrentino F.[8], Vardaro M.[9,10], Zendri J.P.[9,10]

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