

# SPARC activities at Roma2

INFN-Roma2  
(L.Catani)

# Status of Emittance-Meter system

Meeting on SPARC Emittance-Meter - 11 March 2004

Participants: L.Catani, G. Di Pirro, V.Fusco, E.Chiadroni, A.Cianchi, M.Castellano, D.Filippetto, S.Tazzari, A.Clozza, M. Ferrario

## Status Report from A.Clozza:

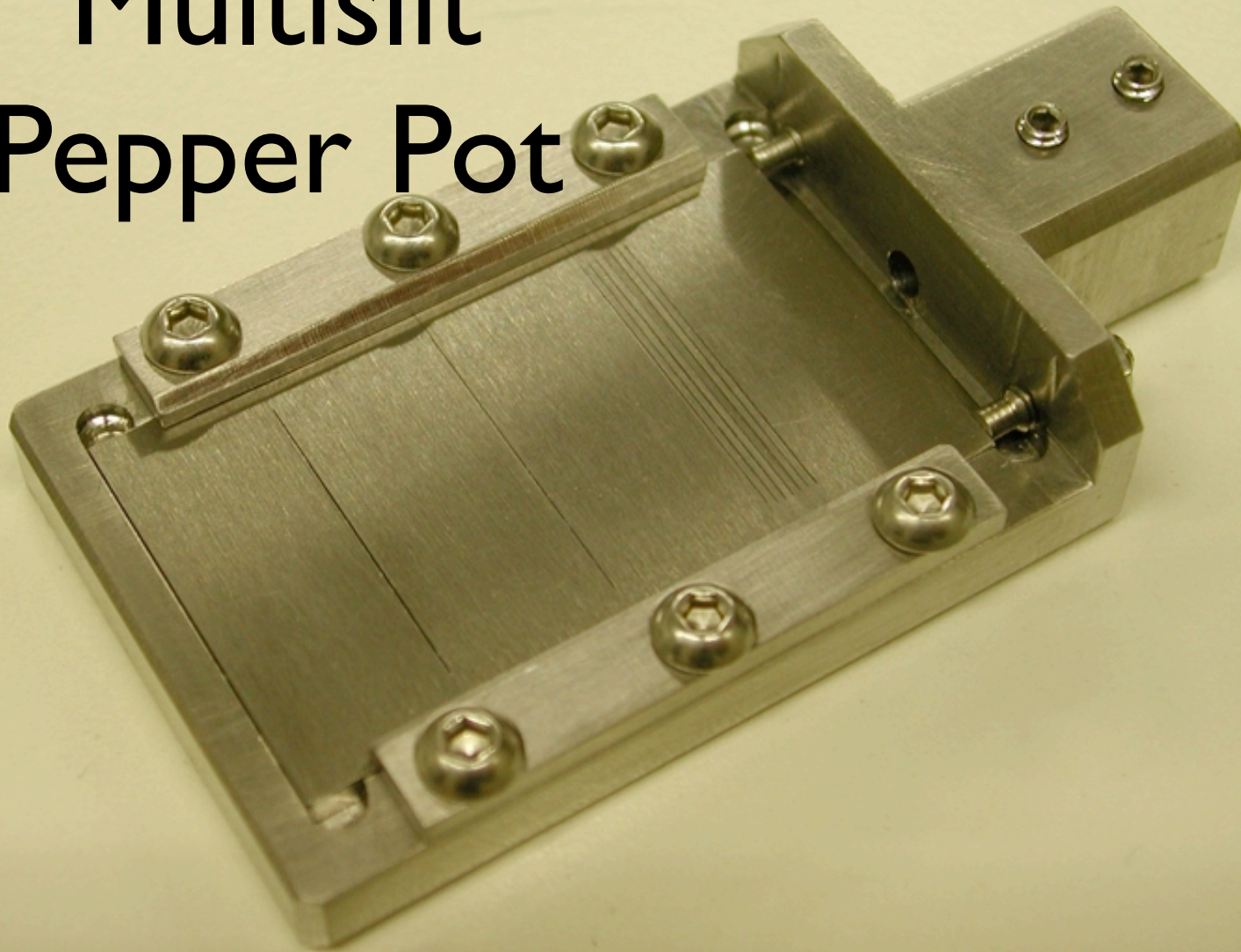
Pepper-pot machined and delivered to LNF It still needs to be cleaned
Order for bellows signed (~25 kEUR): <ul style="list-style-type: none"> <li>2 x long bellows</li> <li>1 x short</li> <li>3 months delivery times</li> </ul>
Minimum distance from cathode to pepper will be ~83cm
Design of the overall system in under way and should be completed in few weeks.

## Discussion

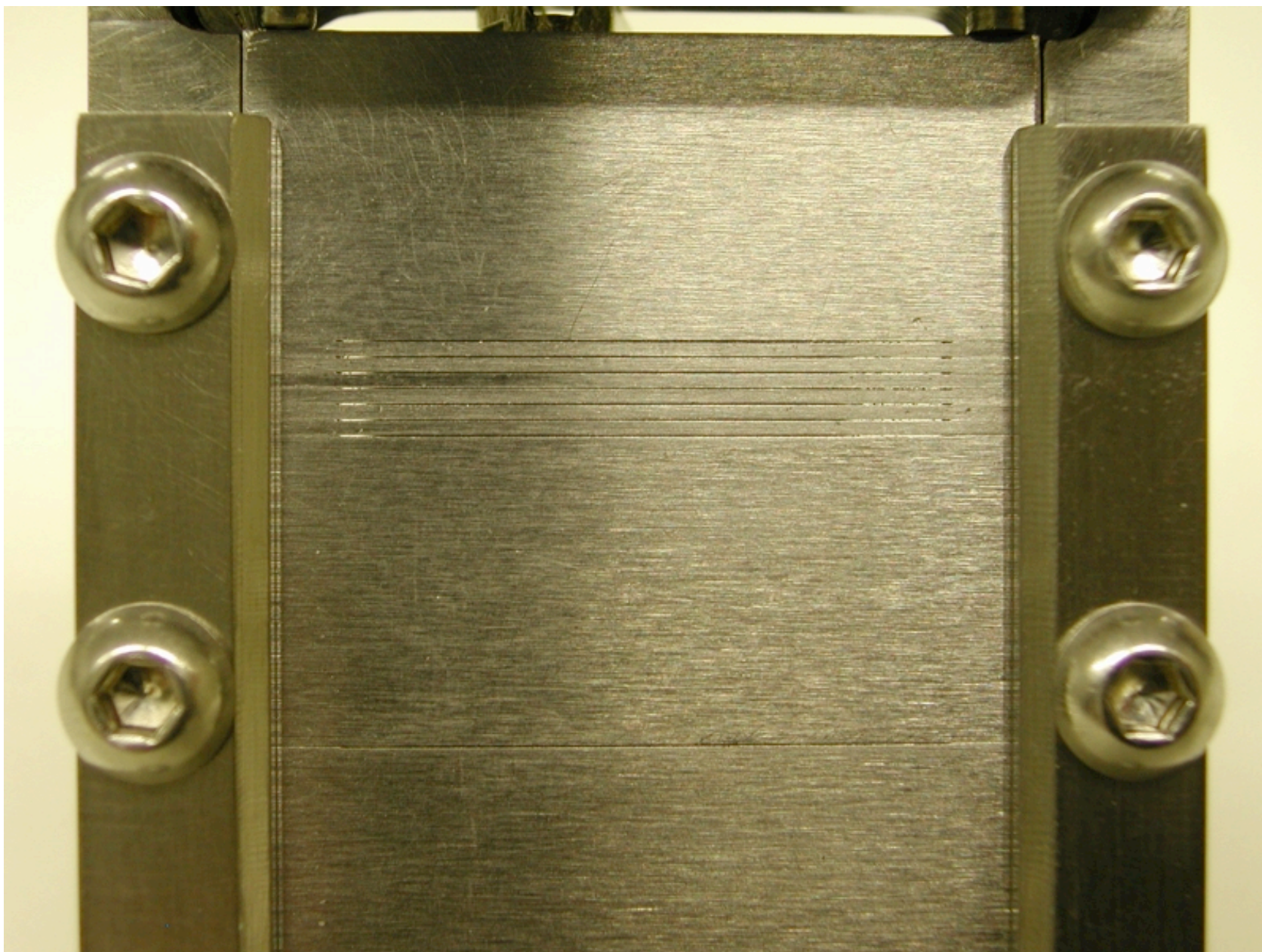
	the possibility of tilting the pepper-pot holder is considered as not critical. The angular acceptance is large enough (25 mrad) to avoid any disturbance to the measurement if the pepper-pot will be properly aligned.	
requirement	Simulations including tilted pepper-pot should be carried out (A.Cianchi) to confirm this analysis providing more detailed information	
	Steerings are desirable to correct beam misalignment in the long e-meter structure	
requirement	Vertical resolution of the pepper-pot position must be better than 25 $\mu\text{m}$ provided the accuracy of the movement is <2 $\mu\text{m}$	
	Speed of vertical movement is not an issue	
requirement	4-phase stepper motor 200 steps/turn	
requirement	Absolute Optical Encoder: accuracy must be	

	better than 10 $\mu\text{m}$ (in principle it should be compatible with the required resolution being 2 $\mu\text{m}$ )	
	For the fluorescent/YAG screen a three positions movement (out, in, calibration) will be sufficient. Precision of the movement is not an issue though the same mechanical components as for the pepper-pot could be used for compatibility. Some calibration system (either a calibration target or some calibration marks on the screen frame) will be needed and it must be discussed.	
	YAG screen with back-observation is so far preferred to ceramic screen	
	Performances and limitations of YAG screen have been discussed taking into account results available in the literature. Calibration of YAG radiator should be performed to evaluate the possible dependency of the beam size with the beam charge density. We should consider to buy a set of crystals to be measured at BTF.	
requirement	Decision on the screen solution should be taken in a separate discussion	

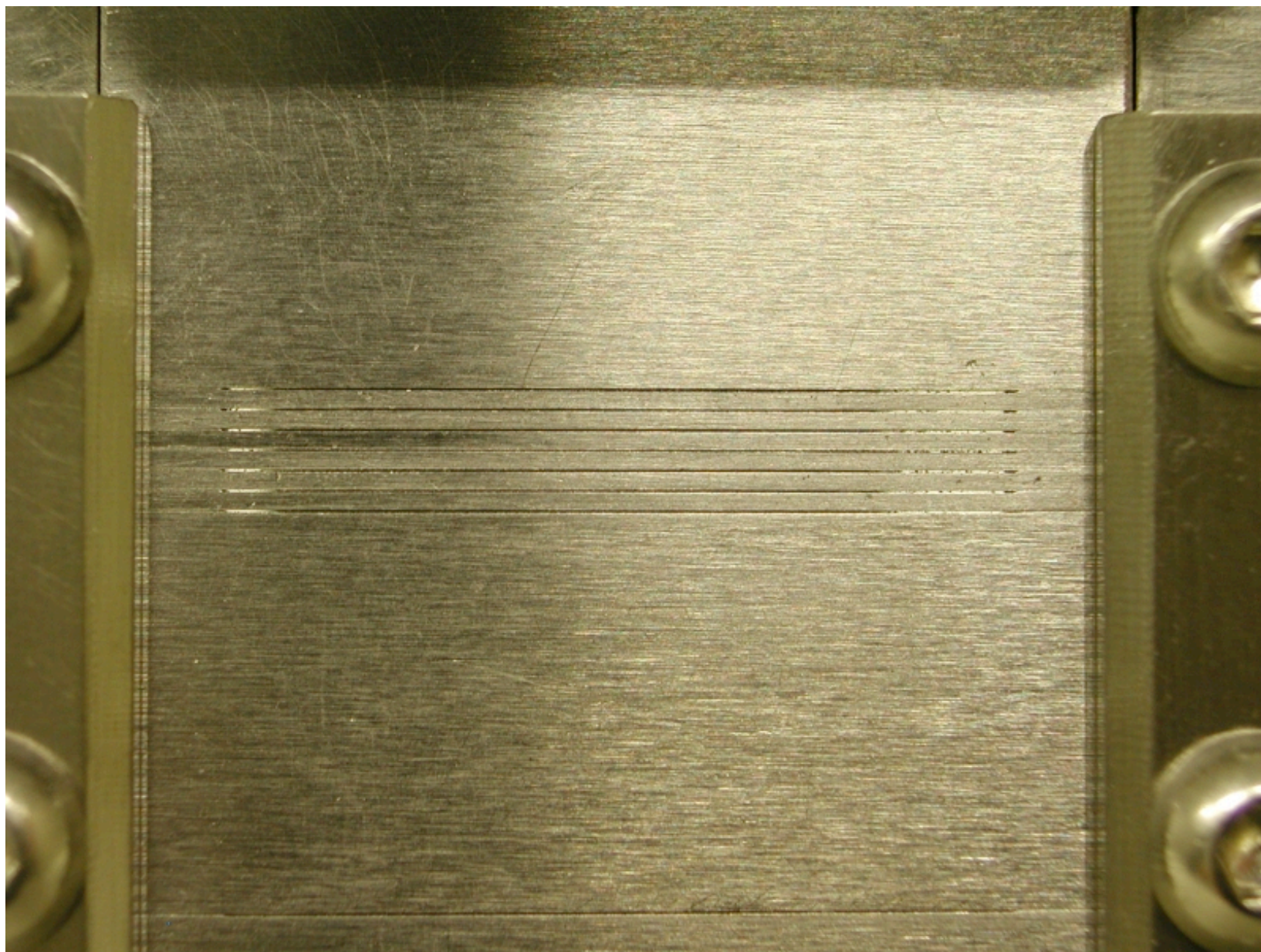
# Multislit Pepper Pot





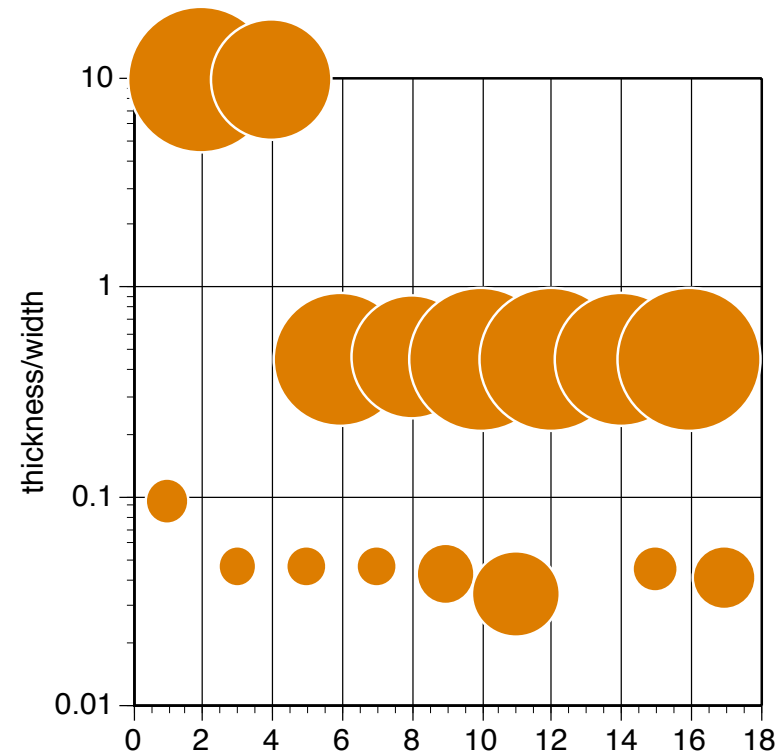






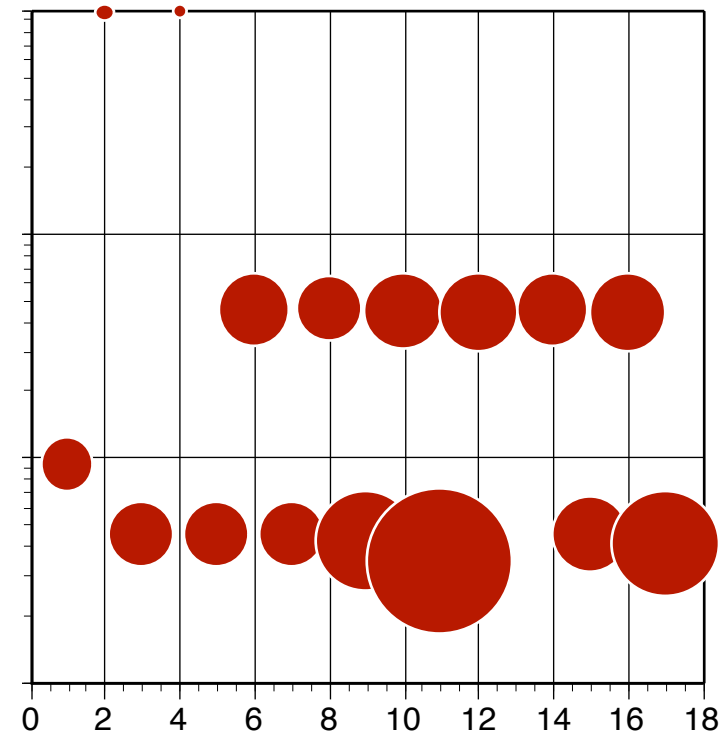
# Multislit Pepper-Pot machining accuracy

	slit#	size (mm)	exp. (mm)	err (mm)
100 $\mu\text{m}$	1	0.0960	0.1000	0.0040
	spacer	9.9600	10.0000	0.0430
50 $\mu\text{m}$	2	0.0470	0.0500	0.0030
	spacer	9.9700	10.0000	0.0290
array of 50 $\mu\text{m}$ slits	3	0.0470	0.0500	0.0030
	spacer	0.4640	0.5000	0.0360
	4	0.0470	0.0500	0.0030
	spacer	0.4700	0.5000	0.0300
	5	0.0430	0.0500	0.0070
	spacer	0.4590	0.5000	0.0410
	6	0.0350	0.0500	0.0150
	spacer	0.4580	0.5000	0.0420
	7	0.0500	0.0500	0.0000
	spacer	0.4640	0.5000	0.0360
	8	0.0460	0.0500	0.0040
	spacer	0.4580	0.5000	0.0420
	9	0.0420	0.0500	0.0080



# Multislit Pepper-Pot (relative errors)

	slit#	size (mm)	exp. (mm)	err (mm)
100 $\mu\text{m}$	1	0.0960	0.1000	0.0400
	spacer	9.9600	10.0000	0.0043
50 $\mu\text{m}$	2	0.0470	0.0500	0.0600
	spacer	9.9700	10.0000	0.0029
array of 50 $\mu\text{m}$ slits	3	0.0470	0.0500	0.0600
	spacer	0.4640	0.5000	0.0720
	4	0.0470	0.0500	0.0600
	spacer	0.4700	0.5000	0.0600
	5	0.0430	0.0500	0.1400
	spacer	0.4590	0.5000	0.0820
	6	0.0350	0.0500	0.3000
	spacer	0.4580	0.5000	0.0840
	7	0.0500	0.0500	0.0000
	spacer	0.4640	0.5000	0.0720
	8	0.0460	0.0500	0.0800
	spacer	0.4580	0.5000	0.0840
	9	0.0420	0.0500	0.1600



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# Status of PCI-PCI Link development

Meeting on PCI-PCI link for the SPARC DAQ/Control System - 11 March 2004  
 Participants: L.Catani, G. Di Pirro, M.Castellano, A.Salamon, E.Gabrielli, M.Sabene, G.Salina, A.Stecchi

## Status Report from A.Salamon:

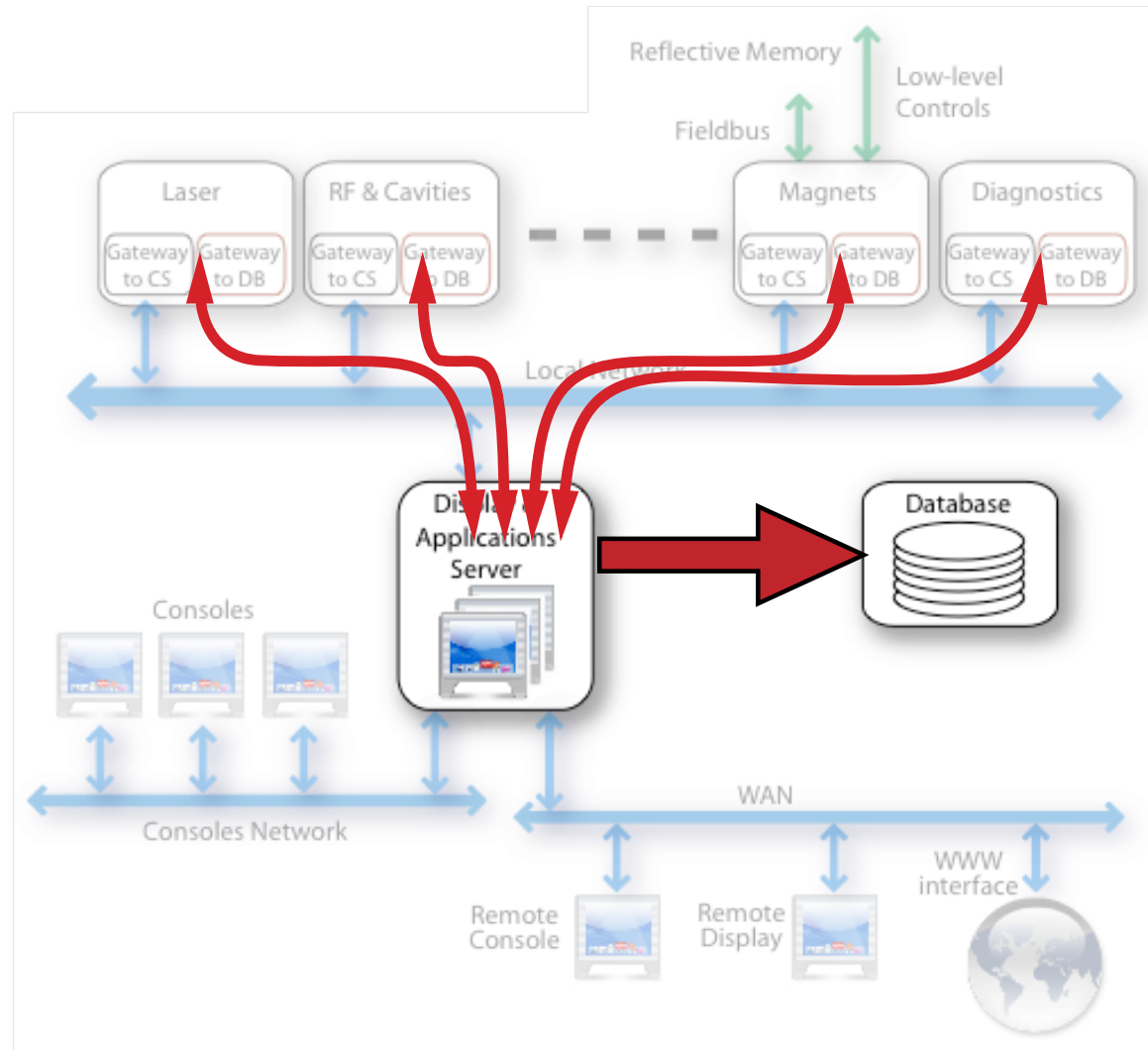
Board developed for 64 bit/66Mhz PCI
Compatible (in principle) with PCI-X (64bit/133Mhz)
On-board memory: single-chip SRAM are available with either 1 Mbyte dual-port or 8 Mbytes single-port. Performances of the PCI-PCI link depends on the choice of the SRAM memory type
2 Mbits bi-directional fiber-optic link has been chosen

## Discussion

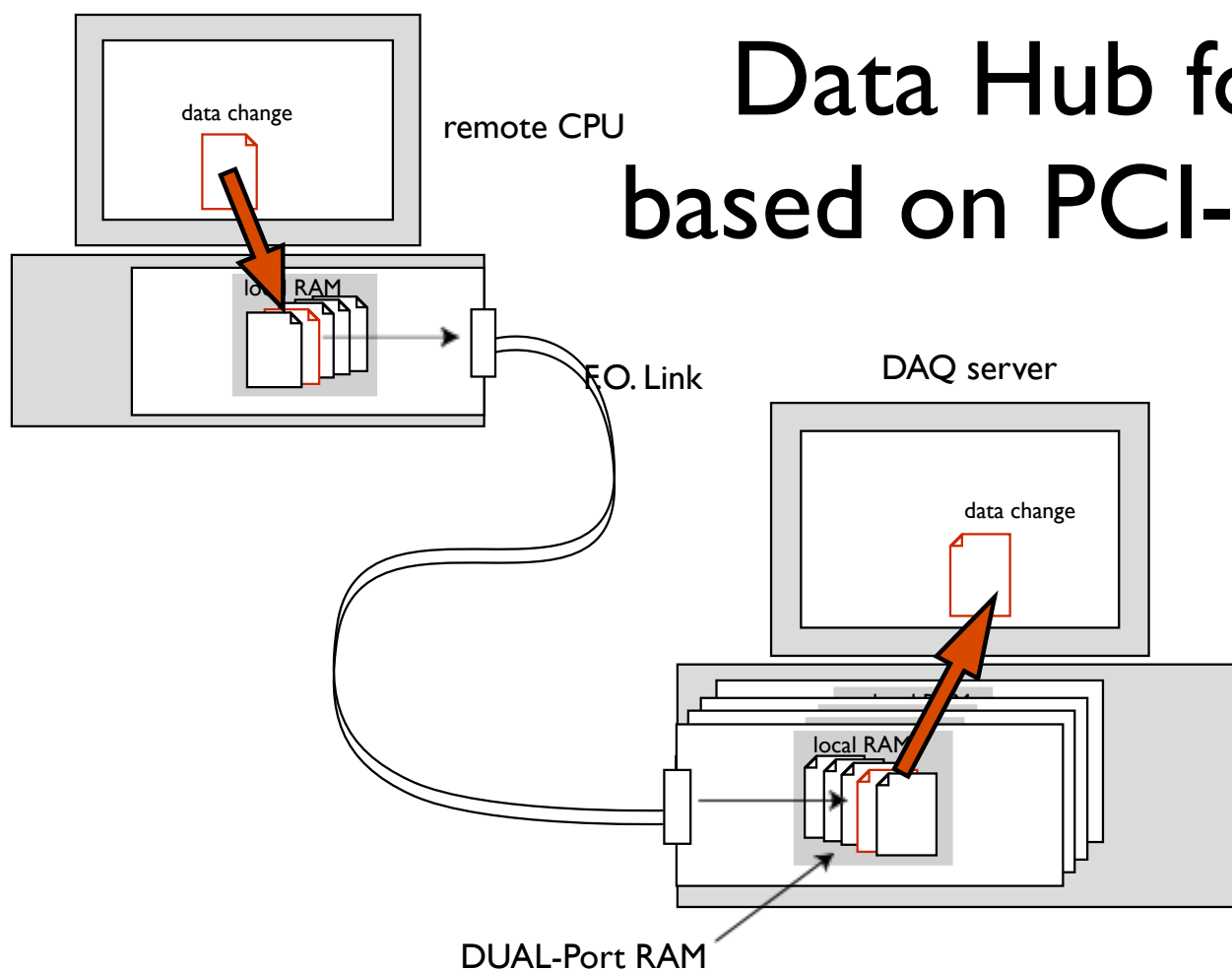
	Single-port SRAM is cheaper than dual-ported counterpart. One 8 Mbyte s-p SRAM cost approx. the same as on 1 Mbyte d-p SRAM (~200 EUR)	
	d-p SRAM allows simultaneous read (from PCI) and write (from f.o. link) maximizing the overall data throughput. In this case some control on the memory access must be foreseen to avoid conflicts when R/Writing the same memory location. This functionality should be provided by the on-board FPGA	
	s-p SRAM doesn't support simultaneous R/W; as consequence the above conflict cannot take place. The main disadvantage is the reduced PCI-PCI data throughput. It is in principle halved but this figure can be slightly improved reading data as longwords (they are written 16 bits)	
	A second level of handshaking is needed to assure data consistency when R/Writing the same block of memory locations (e.g. when a local application is reading a data block being currently updated with data received from the f.o. channel)	
	Any conflict due to simultaneous access to the same	

	memory location/block must be solved giving priority to the writing process, i.e. (new) data coming from the f.o. channel	
decision	An on-board memory of 1 Mbyte has been considered as appropriated for most of the applications foreseen in the SPARC DAQ and control system. Larger memory size might be needed only for large data structure as 16-bit 640x480 image maps. Standard 8-bit 640x480 images will fit into a 1 Mbyte mirrored-memory This solution will provide the maximum achievable data throughput.	
decision	Next step of the development will focus on: <ul style="list-style-type: none"> <li>Designing a PCI-PCI 1 Mbyte mirrored-memory</li> <li>Evaluate the compatibility of the above design with extended on-board memory up to 4 Mbytes</li> <li>2 Mbits f.o. link</li> </ul>	
	Cost of a set of PCI-PCI link should cost ~2.5 kEUR to be compared with ~5 kEUR of the commercial competitor.	
decision	So far only unidirectional data transfer has been taken into account. This feature is sufficient for DAQ application of the PCI-PCI link The possibility to have bidirectional memory-mirroring must be discussed	
decision	A set of boards (at least two) will be ready to be tested with DAQ and Control System applications in 6 months	
	Next meeting will be scheduled when new results from the Roma2 group will be available	

# DAQ



# Data Hub for DAQ based on PCI-PCI link





# e-LogBook

- e-LogBook for SPARC (based on TTF e-LogBook) has been developed and is operational on a temporary server (<http://elog.roma2.infn.it/MYelog/index.jsp>)

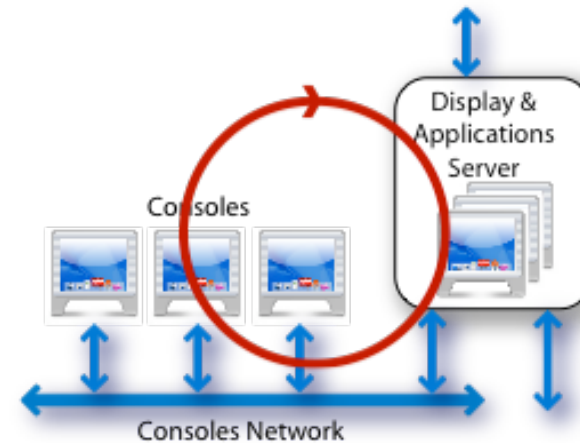
# possible configurations to investigate

thin-clients (Dafne)

workstations (TTF)

hybrid (Linux Terminal Sever)

other..(distributed resources- ex. openmosix.org)



< preliminary  
< results

# WBS for the Emittance-meter

					2004												2005												2006												
topics	sub-topic	milestones		who	g f m a m g l a s o n d												g f m a m g l a s o n d												g f m a m g l a s o n d												
					31-12-2004																																				
meccanica e vuoto		31-12-2004																																							
	progettazione	15-02-2004		LNF	RM2																																				
	offerte	15-05-2004		LNF	RM2																																				
	ordini	30-06-2004		LNF	RM2																																				
	realizzazione	31-10-2004		LNF																																					
test fenditure		31-10-2004		LNF	RM2																																				
movimenti longitudinali e discendenti targhette (motori stepper, elettronica)		31-10-2004																																							
	progettazione	30-06-2004		LNF	RM2																																				
	offerte	15-07-2004		LNF	RM2																																				
	ordini	31-07-2004		LNF																																					
	realizzazione	31-10-2004		LNF	RM2																																				
telecamera e sistema ottico		31-10-2004																																							
	ordini hardware per sviluppo e prog.	1-01-2004			RM2																																				
	progettazione	30-06-2004			RM2																																				
	offerte	15-07-2004			RM2																																				
	ordini	31-07-2004		LNF																																					
	realizzazione	31-10-2004		LNF	RM2																																				
sistema di controllo e acquisizione		31-11-2004																																							
	progettazione	30-06-2004		LNF	RM2																																				
	offerte	15-07-2004		LNF	RM2																																				
	ordini	31-07-2004		LNF																																					
	realizzazione	31-11-2004		LNF	RM2																																				
software di analisi	realizzazione	30-10-2004		RM2																																					



# OTR diagnostics

					2004	2005	2006
31-12-2005					g f m a m g l a s o n d	g f m a m g l a s o n d	g f m a m g l a s o n d
telecamera alta sensibilità		31-12-2005					
	ordine telecamera per tests	31-10-2004		RM2		*	
	test telecamera	30-06-2005	LNF	RM2			
	ordine telecamera scelta	15-07-2005	LNF				
	collaudo e installazione	31-12-2005	LNF	RM2			
obbiettivo MACRO		30-07-2005					
	ordini obb.macro per sviluppo	1-01-2004		RM2	*		
	studio e test	31-12-2004		RM2			
	offerte	15-01-2005		RM2			
	ordini	31-01-2005	LNF				
	realizzazione	30-07-2005	LNF	RM2			
remotizzazione obbiettivo MACRO		31-07-2005					
	progettazione	31-12-2004*	* dipende dalla disponibilit	RM2		*	
	offerte	15-01-2005		RM2			
	ordini	31-01-2005	LNF				
	realizzazione	30-07-2005	LNF	RM2			
sistemi ottici		31-07-2005					
	ordine sistema di sviluppo (componenti ottiche)	1-06-2004		RM2	*		
	progettazione	31-03-2005		RM2			
	offerte	15-04-2005		RM2			
	ordini	31-04-2005	LNF				
	realizzazione	31-07-2005	LNF	RM2			

# Controls

					2004	2005	2006
31-03-2006					g f m a m g l a s o n d	g f m a m g l a s o n d	g f m a m g l a s o n d
Console system		31-05-2004					
	ordini hardware per sviluppo	1-01-2004		RM2	*		
	test e progettazione	31-05-2004		RM2			
e-Logbook		31-10-2004					
	sviluppo e test	30-06-2004		RM2			
	installazione e attivazione	31-10-2004		RM2			
DAQ		31-03-2006					
	test prototipo	31-10-2005	LNF	RM2			
	progettazione	31-12-2005	LNF	RM2			
	offerte	15-01-2006	LNF	RM2			
	ordini	1-02-2006	LNF	RM2			
	realizzazione	31-03-2006	LNF	RM2			

PREVENTIVO LOCALE DI SPESA PER L'ANNO 2004

In KEuro

VOCI DI SPESA		DESCRIZIONE DELLA SPESA					IMPORTI				A cura della Comm.ne Scientifica Nazionale
							Parziali		Totale Compet.		
							SJ		SJ		
Viaggi e missioni	Interno	meeting collaborazione, sviluppo e collaudo a LNF di componenti					3.0		3.0	0.0	
	Estero	conferenze (EPAC, PCaPAC) collaborazione con DESY/Zeuthen e incontri scientifici					5.0 7.0		12.0	0.0	
Materiale Consumo		licenze software (Windows XP Embebbed, LabVIEW) modulistica CAN e kit di sviluppo sistemi ottici e movimentazioni					3.0 5.0		8.0	0.0	
Trasp. e facch.									0.0	0.0	
Spese Calcolo	Consorzio	Ore CPU	Spazio Disco	Cassette	Altro			0.0	0.0		
Affitti e manutenz. apparecchiati.									0.0	0.0	
Materiale inventariabile		telecamera digitale Alta Risoluzione e software di controllo PC104 + kit di sviluppo server rack-mounting scheda IEEE1394 per il controllo della telecamera cavi IEEE1394 alta qualità e ripetitore ottico IEEE1394					4.5 2.5 3.0 3.0		13.0	0.0	
Costruzione Apparat.									0.0	0.0	
Totale									36.0	0.0	

Sono previsti interventi e/o impiantistica che ricadono sotto la disciplina della legge Merloni ? ☐

Breve descrizione dell'intervento:

Mod EC/EN. 2

(a cura del responsabile locale)

+2.0 k€ DAQ, e-Logbook collaboration

- components for the optical resolution test-stand
- camera objective remote control

+1.5 k€ Switch Gigabit Ethernet

+2.0 k€ RAID system

41.5 k€ (total)