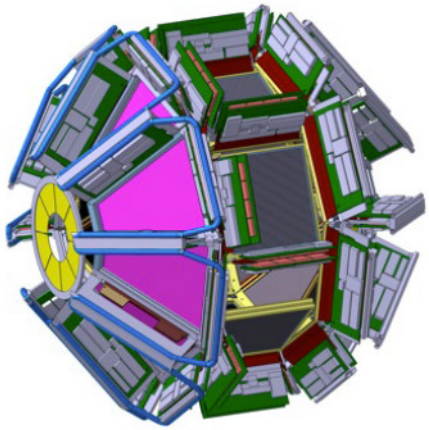
Introduction and Status of the PLAS ASIC developments

Andres Gadea (IFIC-CSIC, Spain)

- **Introduction to Triggered Sampling FEE**
- **Introduction and Status of the GRIT PLAS FEE.**
- **Outlook**



GRIT Workshop, Firenze, Italy, October 9th-11th , 2019

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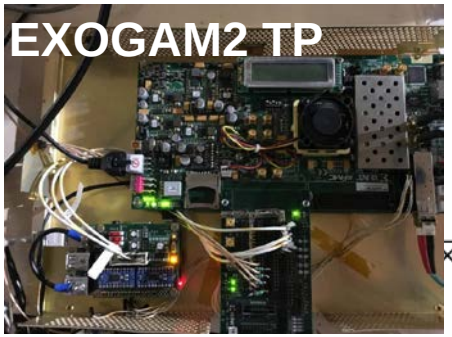
lpc caen laboratoire de physique corpusculaire

GTS Trigger & Synchronization Structure

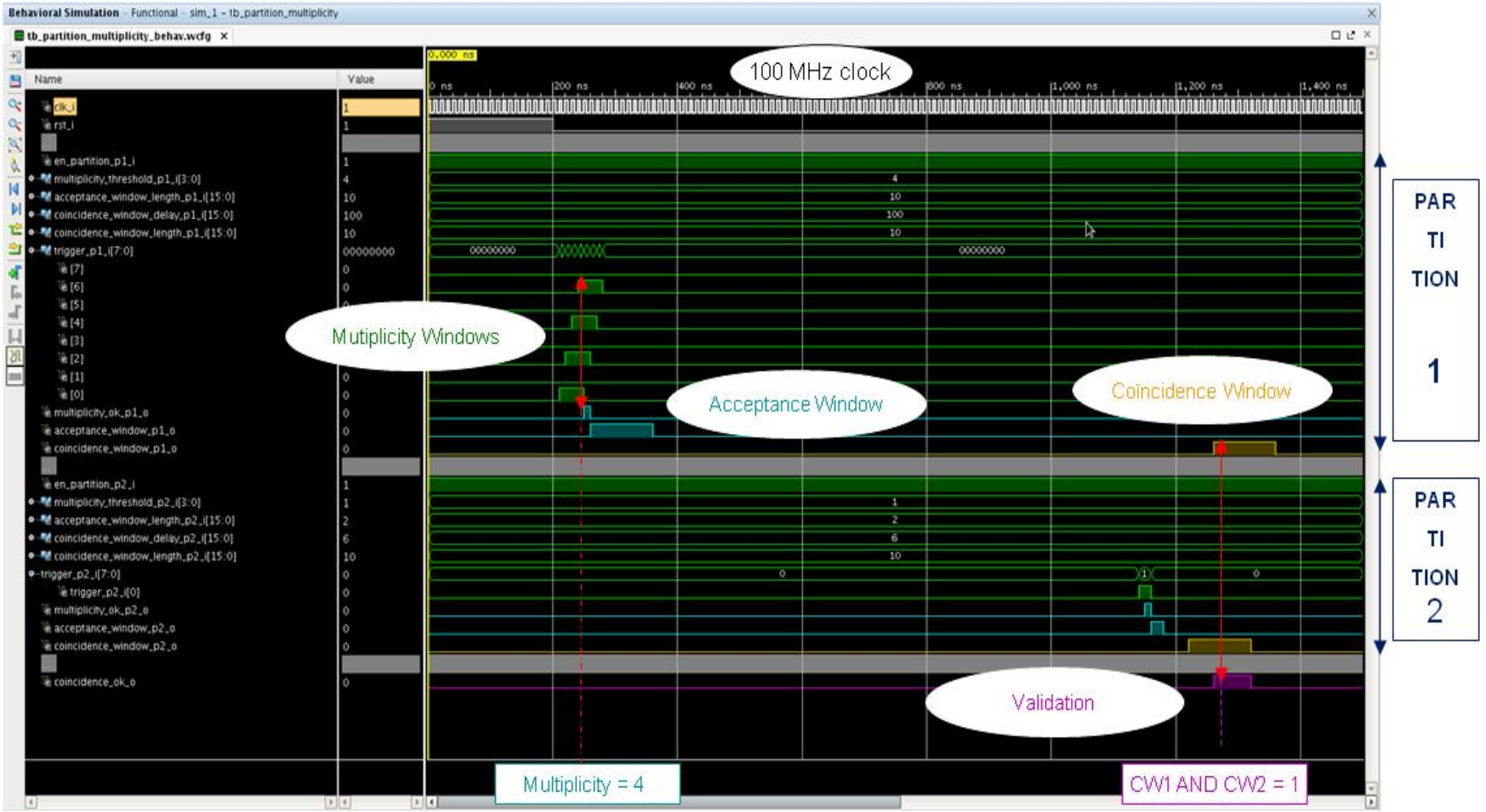


Early AGATA GTS Trigger Processor limited to 40 TR (channels).
The EXOGAM2 GTS Trigger Processor, (GANIL), used for 2018 campaign,
Control by IPbus done at IPHC
New version under production.

GTS Trigger decisions based on topological & time information

INFN-Padova, GANIL-Caen, IPHC-Strasbourg

NUMEXO2 / GANIL GTS Trigger Processor

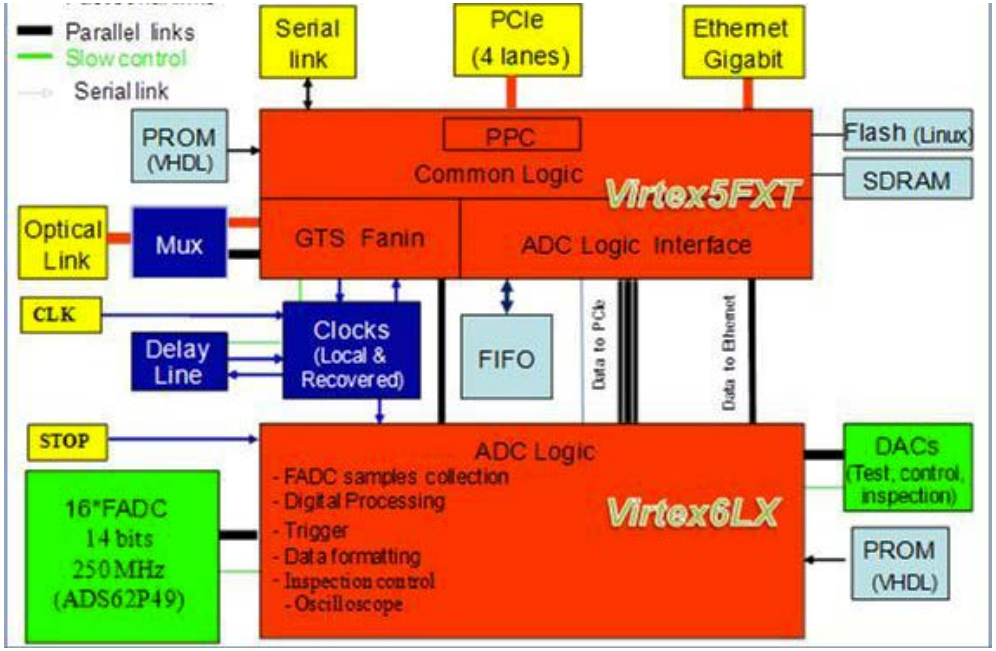


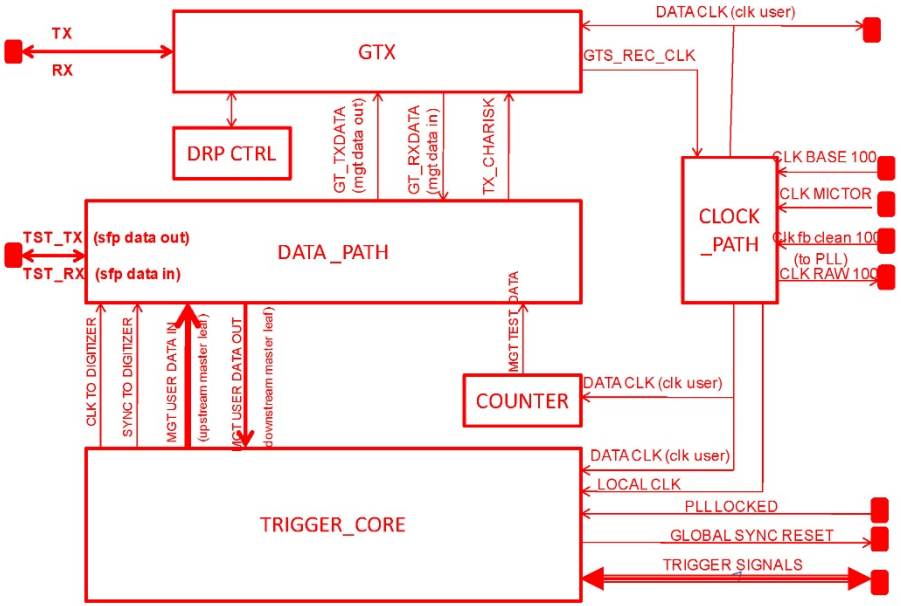
Looking forward to have a Hardware and a Software Trigger Levels

Courtesy of M.Tripon and the GANIL collaborators

GANIL-Caen, IPHC-Strasbourg, CSNSM

e.g. designed FEE for NEDA





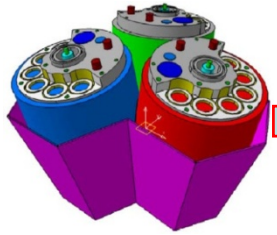
Design by GANIL

FADC Mezzanine

Design and Build by ETSE (UVEG) & IFIC in Collaboration with GANIL

Structure of Electronics and DAQ

Digital preamplifier concept



Fast 1st Level Trigger

Other Detectors

Diff. Fast-reset-TOT
INFN-MI/GANIL/KÖLN

75.5db SNR
IPHC/Liverpool/
STFC

12.2 ENOB

200MB/s/
segment

GL Trigger

Clock
100 MHz
T-Stamp

Other
detectors

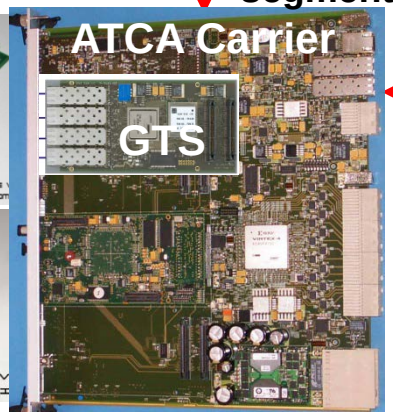
GTS
INFN-Pd

Detector
Level

PSA
FARM

Core +
36 seg.

100MB/s/
detector



HIGH THROUGHTPUT
PRE-PROCESSING
CARRIER / MEZZANINES
IPNO/CSNSM/INFN-Pd

Global Level

EVENT
BUILDER

TRACKING

Control,
Storage…

Other
detectors

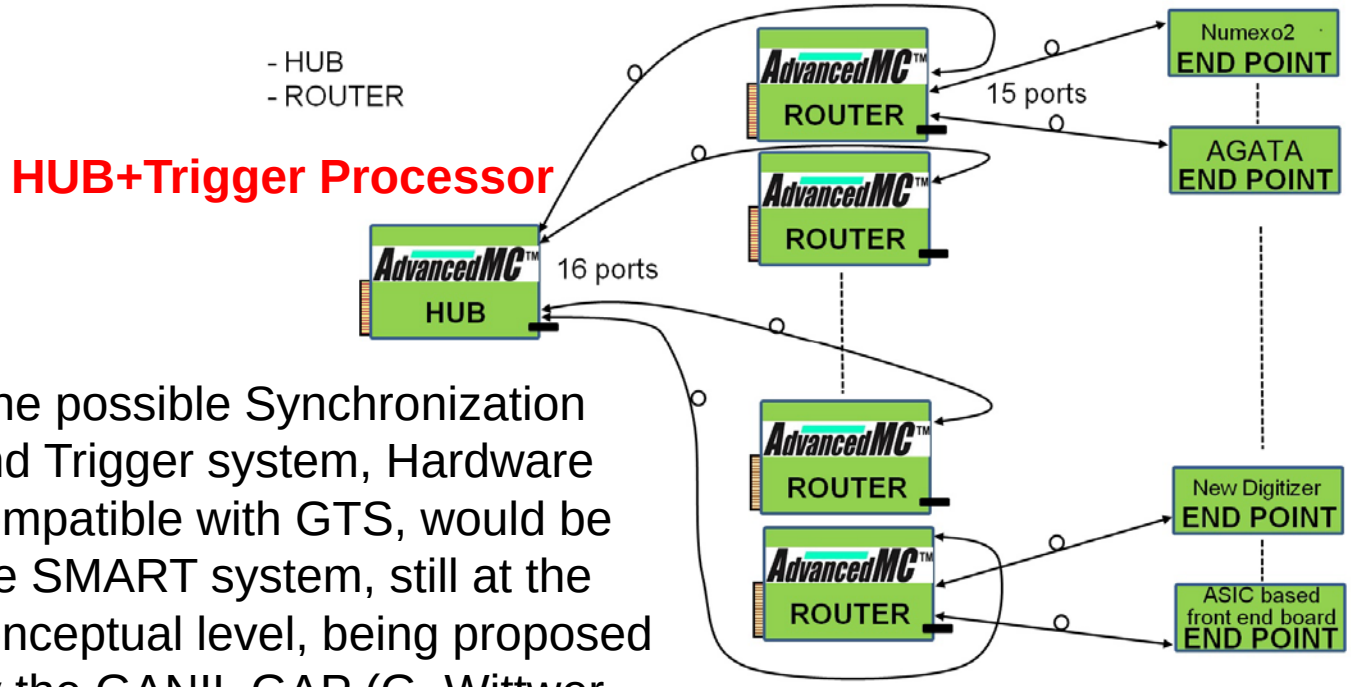
DAQ-NARVAL
RUN- & SLOW-Control

IPNO/CSNSM/
LNL/GANIL/IFJ-PAN

interface to GTS, merge time-stamped data into event builder, prompt local trigger from digitisers

GTS → SMART

UPGRADE OR NEW SYNCHRONIZATION/TRIGGER SYSTEM



One possible Synchronization and Trigger system, Hardware compatible with GTS, would be the SMART system, still at the conceptual level, being proposed by the GANIL GAP (G. Wittwer et al.).

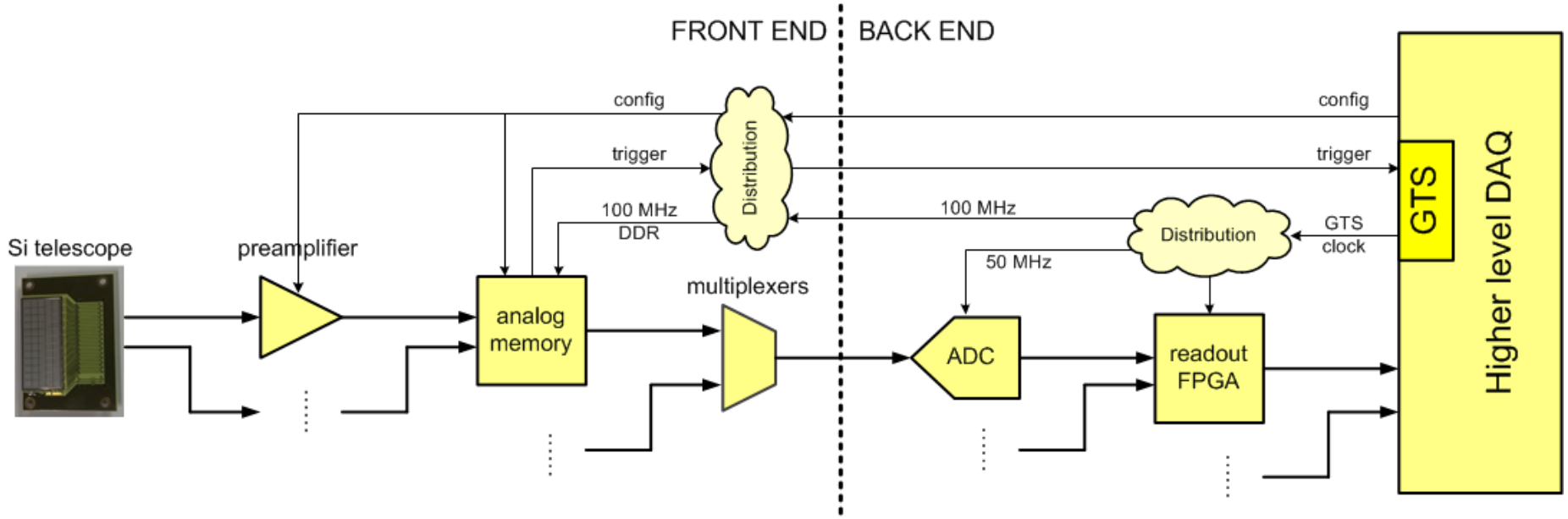
Expected to start in 2021 with the present GTS system but we would need to migrate towards a new system (SMART) system during the early years of the Phase 2.

Note that the pre-processing embedded GTS hardware is compatible with the SMART hardware. In SMART the HUB hosts the Trigger Processor.

GRIT
Front-end Electronics requirements.

- High integration to limit cost and reduce complexity in a large number of channels (>10000). Readout by few lines.
- Digital FEE with a sampling frequency ≥ 200 MHz (required for Pulse Shape Discrimination and timing)
- Large dynamical range (Possibly fast reset PA)
- Capability to contribute to the GTS trigger
- Capability to synchronize with AGATA, EXOGAM2 and GALILEO.
- Samples read-out to perform off-line advanced PSA

GRIT
readout chain concept (I)



- Multiple detectors analogically sampled and buffered
- All detectors synchronized and participating to the trigger
- Readout, through a single line, including all identification of the channel and all ingredients for calibration

Not feasible to link GTS to each detector Strip/PAD

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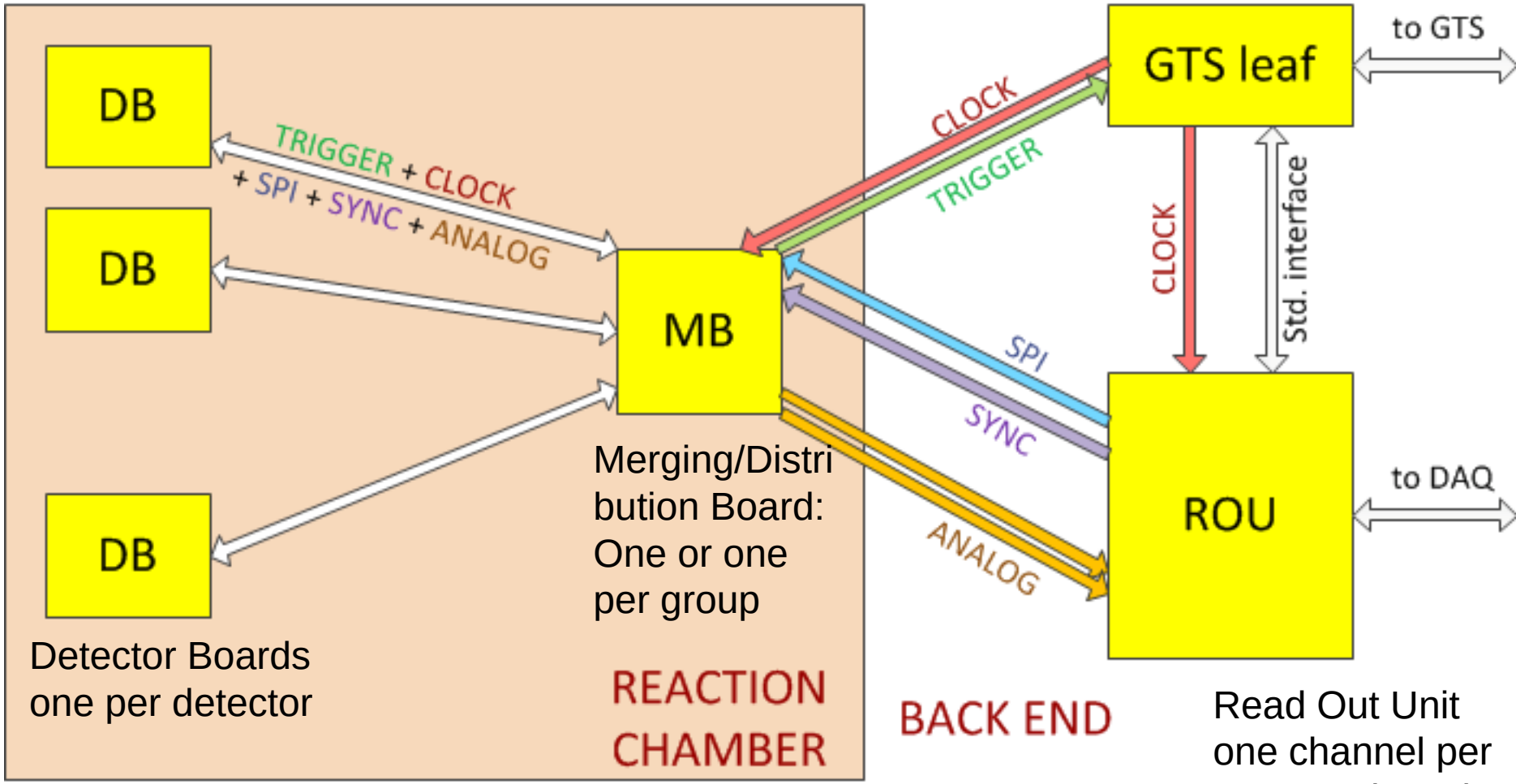
GRIT
readout chain concept (II)



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GRIT
Electronics Ingredients:

- Highly integrated pre-amplifier on ASIC
  - ToT ASIC (INFN-Milano): with Fast Reset and ToT capability **(Stefano Capra Talk)**
  - iPACI ASIC (IPNO Orsay): with Current and Charge signals **(Emmanuel RaulyTalk)**
- Shaper to take into account the baseline (to be understood where to place it)
- Analogue buffer PLAS (sampling at 200 MHz, clock, synchronization, trigger detector Pad/Strip identification etc…
- Merging/Distribution board:
  - Clock Distribution
  - Trigger Merger
  - Control Distribution
  - Synchronization Distribution
- READOUT system Sampling at 50 MHz, One channel per Detector/PLAS, GTS leaf capability. Possibility to use FASTER.
- To be discussed how to include ToF measurements

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GRIT
Electronics Ingredients:

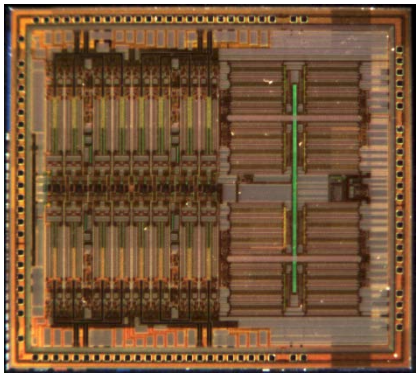
The READOUT system should be able to:

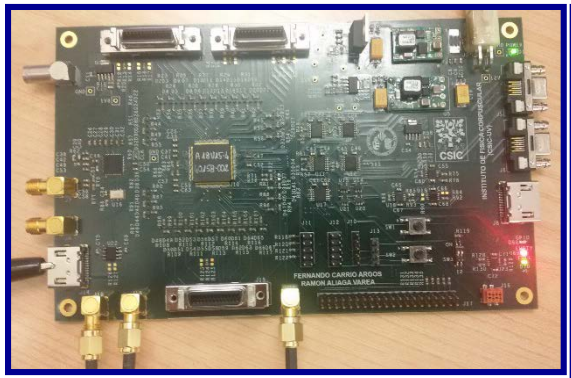
- Receive an external trigger request from the PLAS ASIC
- Capability to link to GTS and provide a time stamp at the time of the trigger request.
- Should be able to produce a synchronize order for the PLAS ASIC and assign the PLAS counters for all detectors the corresponding GTS timestamp offset.
- To input the data sequence to be sample at least at 50 MHz.
- On receiving real data, to decode the synchronization counter from the data sequence and reconstruct the corresponding GTS time stamp.
- Decode detector identifier and Digitize the analogue samples amplitude from the waveform, as well as the sample information stored in the data flow.
- Receiving the Validation or rejection answer from the GTS TP, with transfer the data or clean/flush them respectively.

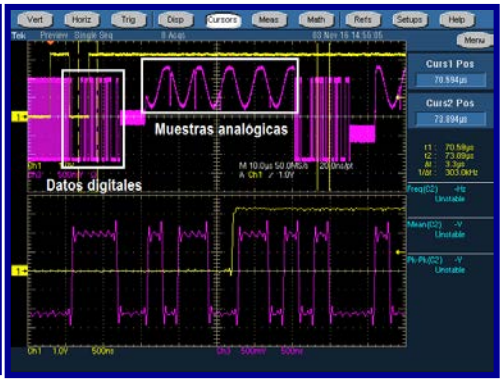
The AGATA Group at IFIC: Contribution and Status

Grant PROMETEO II/2014/019 2014-17

•Microelectronics R&D for the readout of the GHT light charged particle DSSSD/Si-PAD telescope detector array as tagging detector for AGATA. Development of an ASIC with synchronized analogue buffers: signal sampling for particle identification: IFIC (R.Aliaga et al.) Electronics serv., UPV-I3M, UVEG-ETSE.







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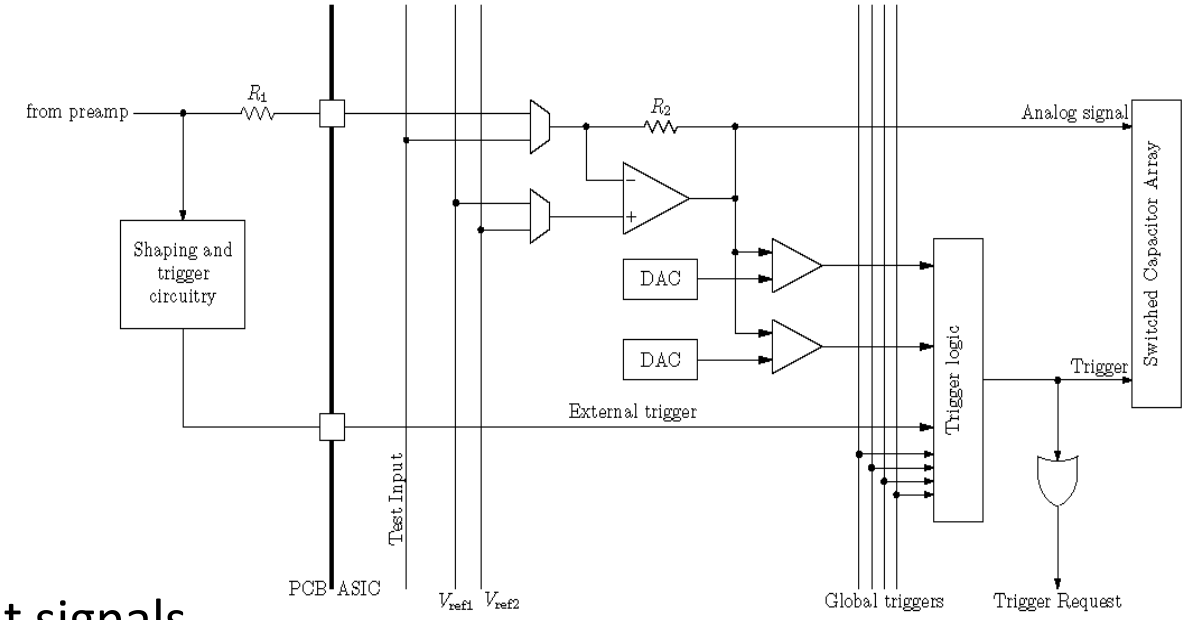
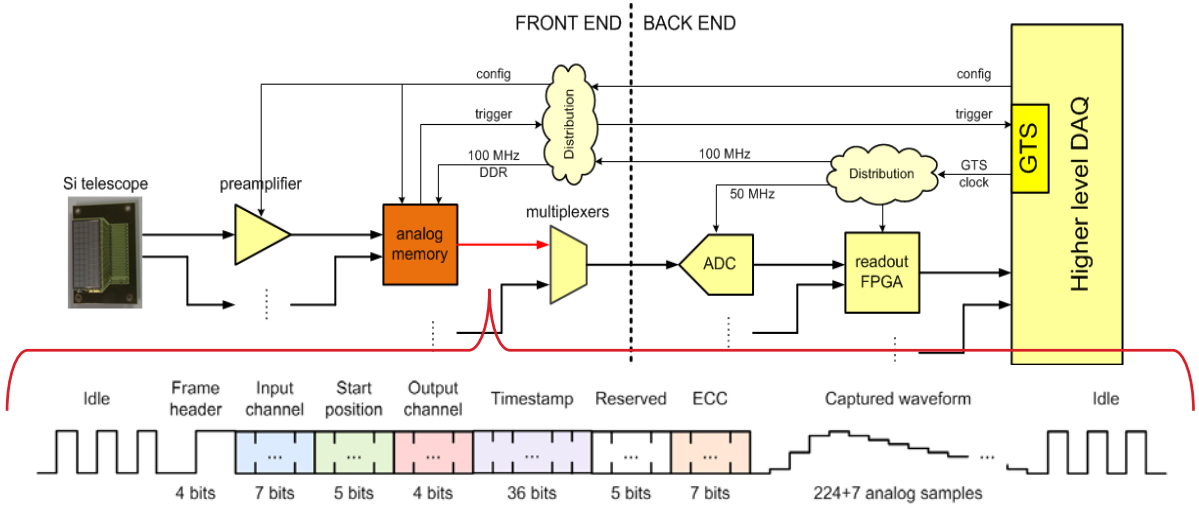
PLAS V1

The Input Stage



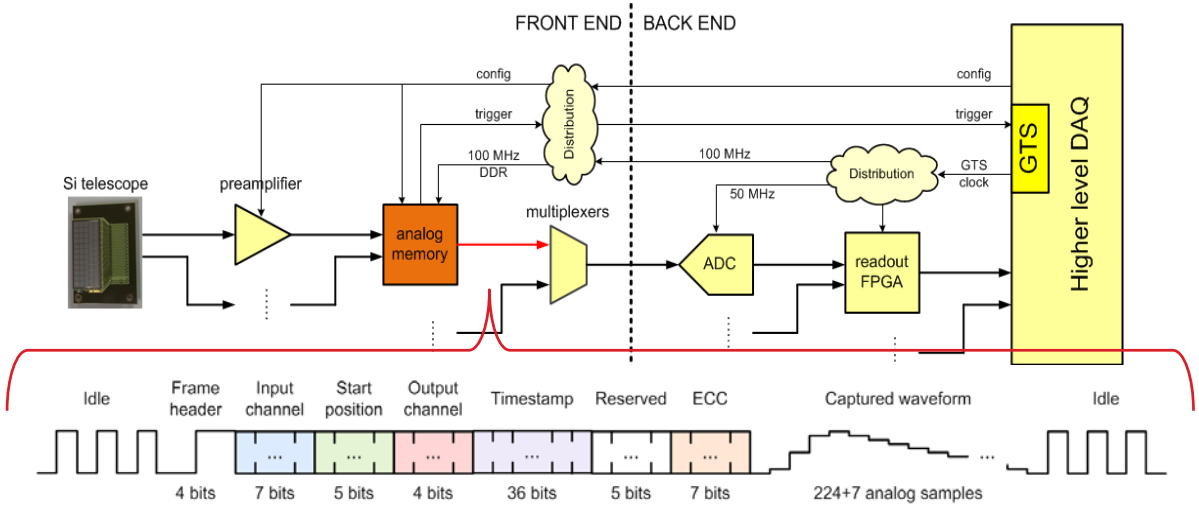
- Input signals
  - Configurable input range and polarity for each channel
  - External resistor R_1
  - Programmable V_{ref} (2 per block of 8 channels)
- Channel trigger
  - Leading edge, programmable threshold (2 per channel)
  - Programmable mode (edge polarity, global trigger, hysteresis…)

PLAS
The Output Format



- All data serialized into one differential link at 50 MBaud
- Output frames contain analog and digital data for single pulses
- Frame contents:
  - Training pattern when idle (010101…)
  - Frame header
  - ID of triggering channel
  - Circular buffer position on trigger
  - Tracking info through PLAS
  - Trigger timestamp (Grey encoded)
  - Error correcting code (SECDED)
  - 32(+1) pre-trigger samples
  - 192(+6) post-trigger samples
- Total duration: **6.0 µs** (up to 166 kEvent/s)

PLAS
The Output Format Testing

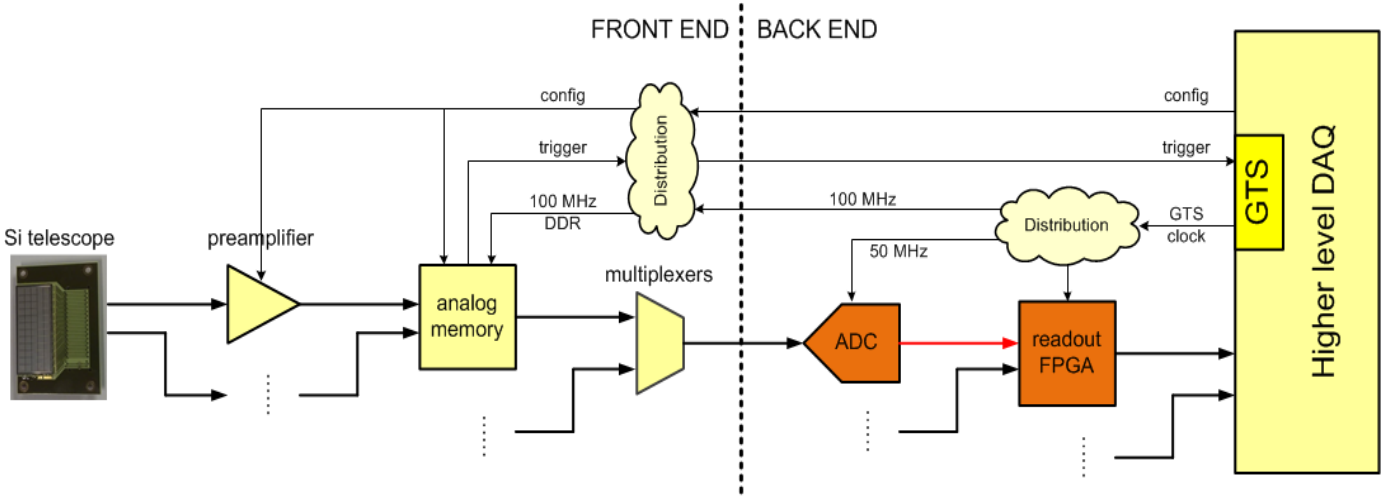


- All data serialized into one differential link at 40 MBaud
- Output frames contain analog and digital data for single pulses
- Frame contents:
  - Training pattern when idle (010101…)
  - Frame header
  - ID of triggering channel
  - Circular buffer position on trigger
  - Tracking info through PLAS
  - Trigger timestamp (Grey encoded)
  - Error correcting code (SECDED)
  - 32(+1) pre-trigger samples
  - 192(+6) post-trigger samples
- Total duration: **7.5 µs** (up to 133 kEvent/s)

Ramon Aliaga, IFIC and UPV

PLAS

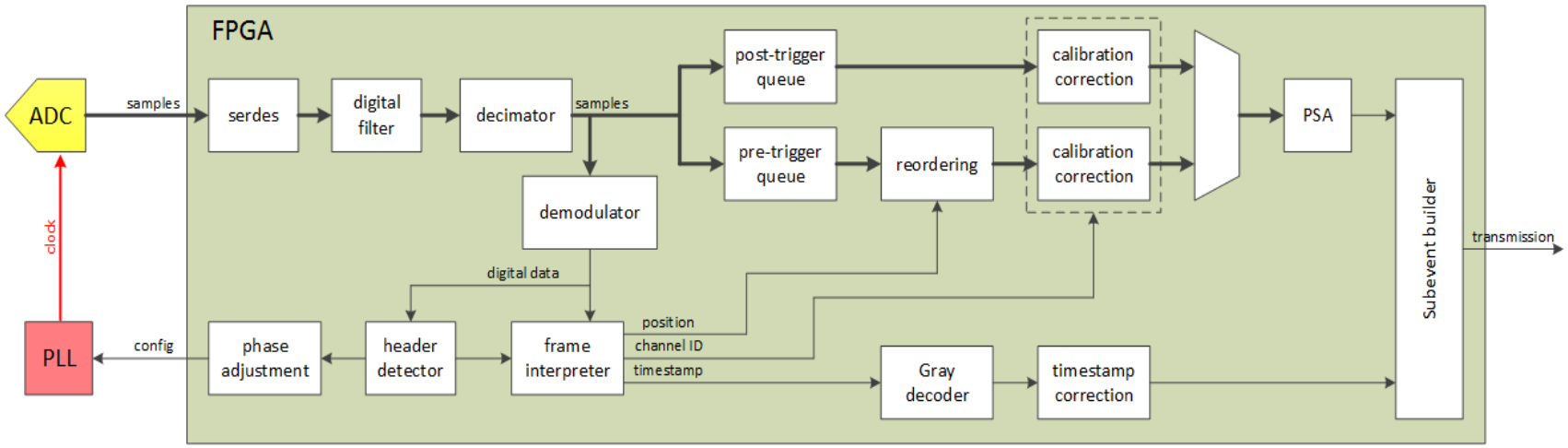
The Readout



- Frames are digitized by free running ADC
  - Digital: “0”= –1.8V, “1” = +1.8V
- FPGA mandatory for decoding ADC output
  - Detect start of frame
  - Decode frame contents
  - Reorder samples
  - Digital filtering
  - Control sampling phase

PLAS

The Readout



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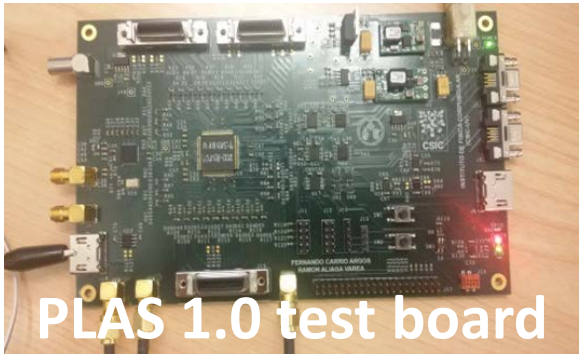

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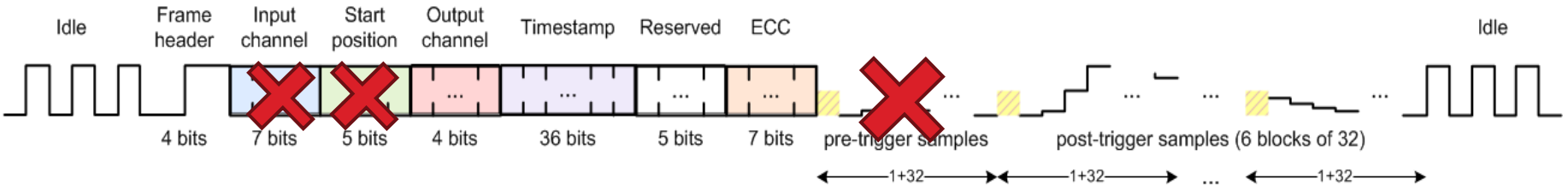
PLAS
Fuctional Test Summary

- Summary: **PLAS 1.0 works partially**, **redesign mandatory**
- Some event data is lost
  - Pre-trigger samples
  - Triggering channel ID
  - Circular buffer position
- Max frequency below 100 MHz
  - Using 80 MHz for tests
- Configuration interface fully operational
- Trigger request and control signals working



PLAS
Calibrated Performance

Performance	
Bandwidth	45 MHz
Input range*	around 3 $V_{pp\ in}$
Noise floor*	7.9 mV_{in} rms (overall) 6.1 mV_{in} rms (good channels)
SNR	52.8 dBFS 8.5 ENOB
INL	0.1%
Crosstalk	0.1% (adjacent channels)
Power consumption	12 mW/channel

* related to input voltage, with gain G=1/2.6

- Simulated values were
  - BW > 150 MHz
  - SNR > 11.5 ENOB
- We need to analyze what went wrong

PLAS

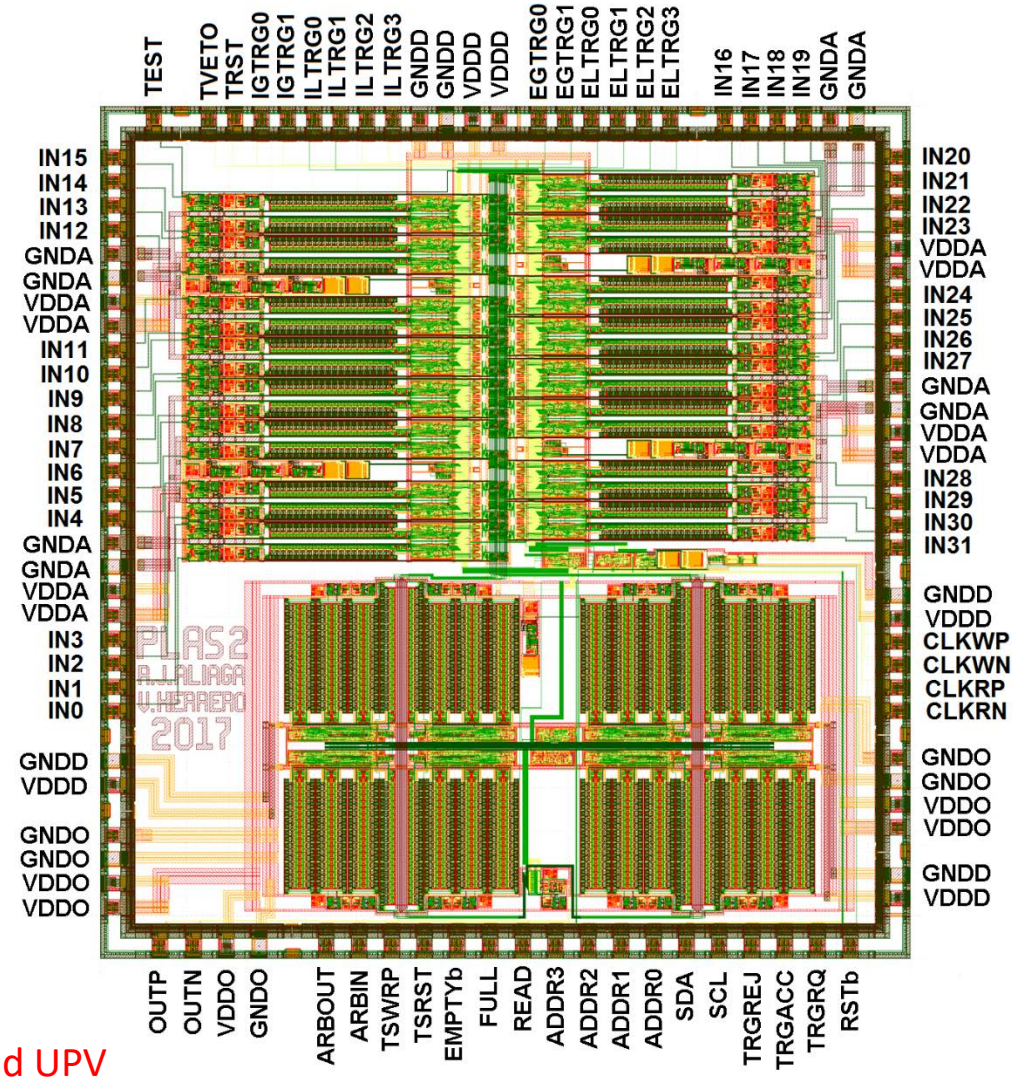
Status

- PLAS 1.0
  - FPGA-based readout
    - Custom DAQ: Complete (some upgrades pending)
    - NUMEXO2: TBD
  - Characterization and calibration
    - @ 20 MHz: Complete
    - @ 160 MHz: TBD, results expected soon

- PLAS 2.0
  - Fix/redesign trigger logic
  - Fix digital operating frequency
  - Tune analog performance based on final characterization
  - Implement additional functionality
  - Foundry deadline: **?**

PLAS V2

layout



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PLAS V2

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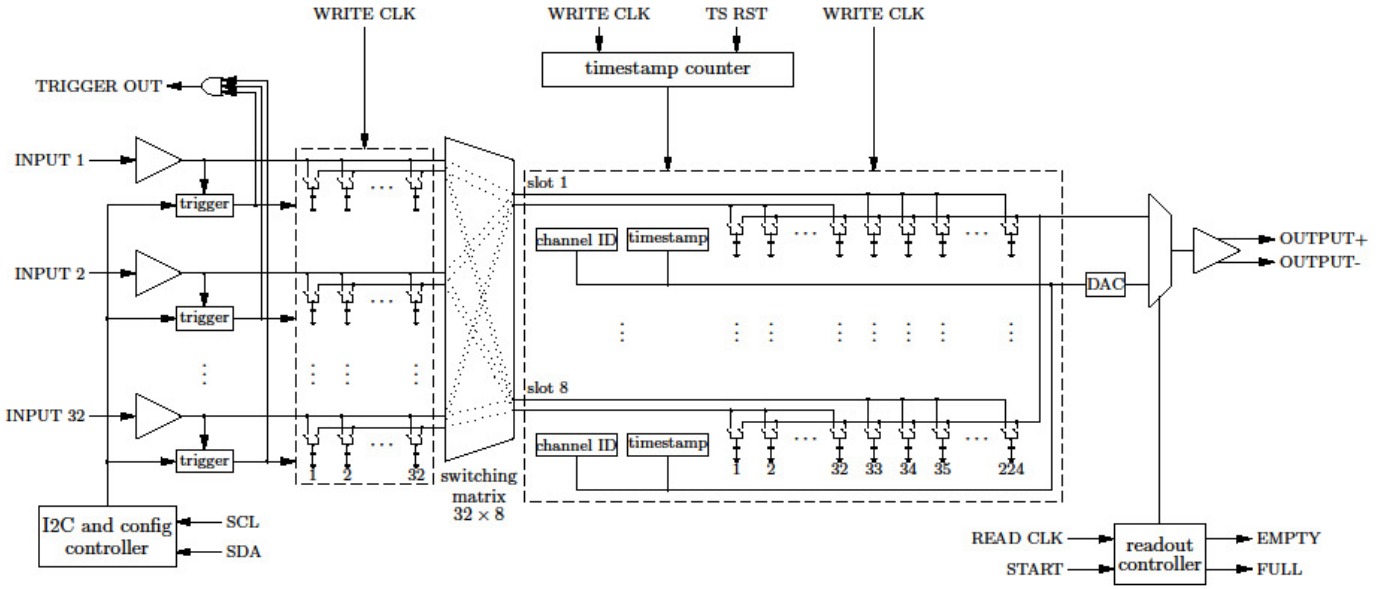

Figure 1. PLAS functional block diagram.

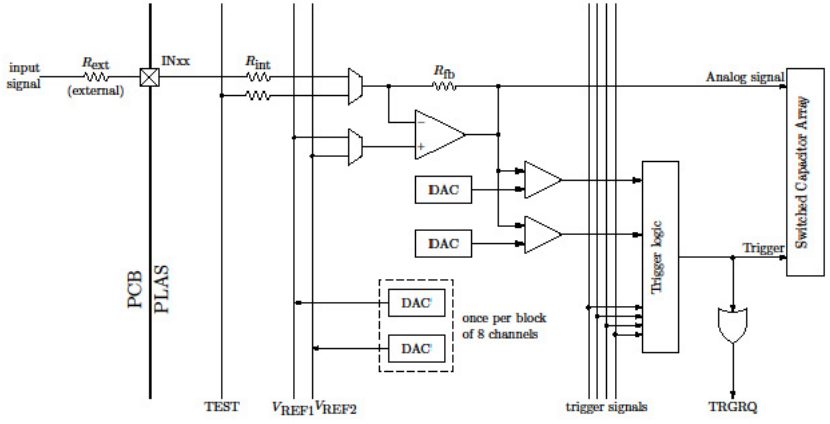

Figure 4. PLAS2 input channel schematic.

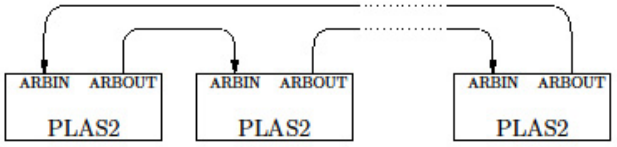

Figure 6. Connection of multiple PLAS2 devices.

PLAS V2

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Bug corrections

- Corrected a bug that limited the input bandwidth to around 40 MHz
- Corrected a bug that caused the pre-trigger samples and input channel ID not to be transmitted

New features

- Reworked trigger system, including trigger vetoes and channels triggering other channels
- Independent clocks for write and read operations
- Internal tuning of write clock duty cycle
- Storage of old samples for baseline estimation
- Support for multichip arbitration and multiplexing

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PLAS V2
Status and Outlook

LPC-Caen, IFIC-Valencia

- IFIC-Valencia has no more available the Original designer of PLAS (R.Aliaga), Moreover PLAS V2 was not ready for production due to issues with the foundry (change of 0.18µm technology).
- LPC-Caen Colleagues: Laurent Leterrier, Sebastien Drouet, et al., took over the original design, corrected it with the help of R.Aliaga
- They also found the TSI company which offers the 0.18um process with a MPW Shuttle Service, based on the IBM 0.18µm process used by AMS at the time of the PLAS V1 and V2 design.
- Exchange of information is continuing over these months.
- LPC-Caen confident on the possibility to submit the PLAS V2 design to the foundry by the end of the year.
- PLAS readout electronics supporting GTS/SMART to be decided: FASTER ?

Thank You!

EXCELENCIA SEVERO OCHOA

UNIÓN EUROPEA
Cofinanciado por el Fondo Europeo de Desarrollo Regional
Una manera de hacer Europa

GVA Grant PROMETEU 2019/05
Science Ministry, Spain n. FPA2017-84756-C4

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