A proposal for the SPARC Timing System

Alessandro Drago

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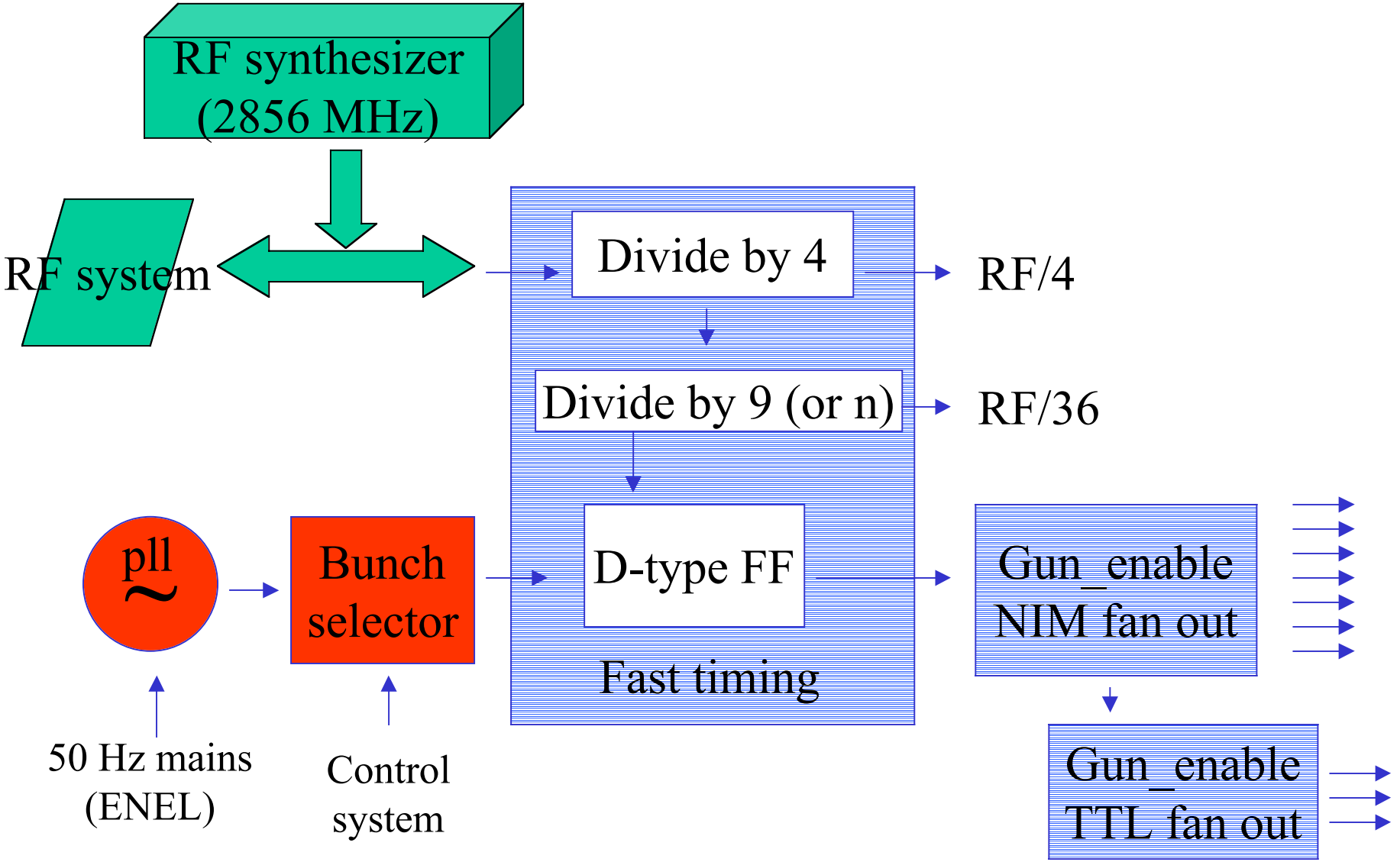
Trigger requirements

- Gun_enable (max jitter ~1 ps, freq.: 0.1-10 Hz)
- Laser clock (max jitter ~1 ps, frequency: RF/36)
- Oscilloscopes (level: NIM, max jitter: ~10 ps, frequency: gun _enable)
- Digitizers (level: NIM, max jitter: ~10 ps, frequency: gun _enable)
- Cameras (level: TTL, max jitter: ~500 ps, frequency: gun _enable)
- Streak camera (max jitter ~2 ps, frequencies: RF/36 and gun_enable)

Timing System Block Diagram



Divider-by-2 specifications

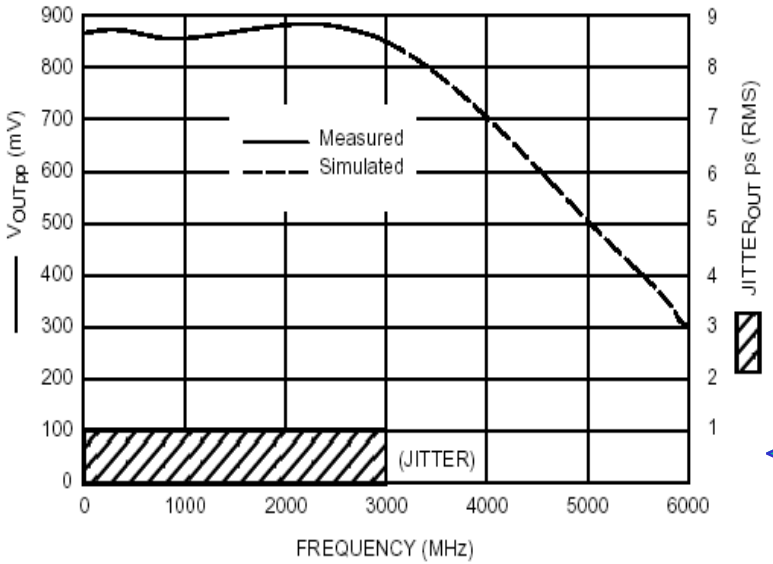


Figure 3. F_{max}/Jitter

AC CHARACTERISTICS V_{CC} = 0 V; V_{EE} = –3.0 V to –5.5 V or V_{CC} = 3.0 V to 5.5 V; V_{EE} = 0 V (Note 21.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Frequency (See Figure 3. F_{max}/JITTER)		> 4			> 4			> 4		GHz
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential CLK to Q, $\overline{Q}$ 10 Series RESET to Q, $\overline{Q}$ 100 Series RESET to Q, $\overline{Q}$	250 220 320	330 290 400	420 390 480	270 250 320	350 300 400	450 390 480	320 320 375	400 380 450	480 460 525	ps
t_{RR}	Set/Reset Recovery	200	175		200	175		200	175		ps
t_{PW}	Minimum Pulse width RESET	550	475		550	475		550	475		ps
t_{JITTER}	Cycle–to–Cycle Jitter (See Figure 3. F_{max}/JITTER)		0.2	< 1		0.2	< 1		0.2	< 1	ps
V_{PP}	Input Voltage Swing (Differential)	150	800	1200	150	800	1200	150	800	1200	mV
t_r t_f	Output Rise/Fall Times Q, $\overline{Q}$ (20% – 80%)	50	100	150	70	120	170	70	130	200	ps

21. Measured using a 750 mV source, 50% duty cycle clock source. All loading with 50 ohms to V_{CC}–2.0 V.

Synchronous binary “n” counter jitter specifications

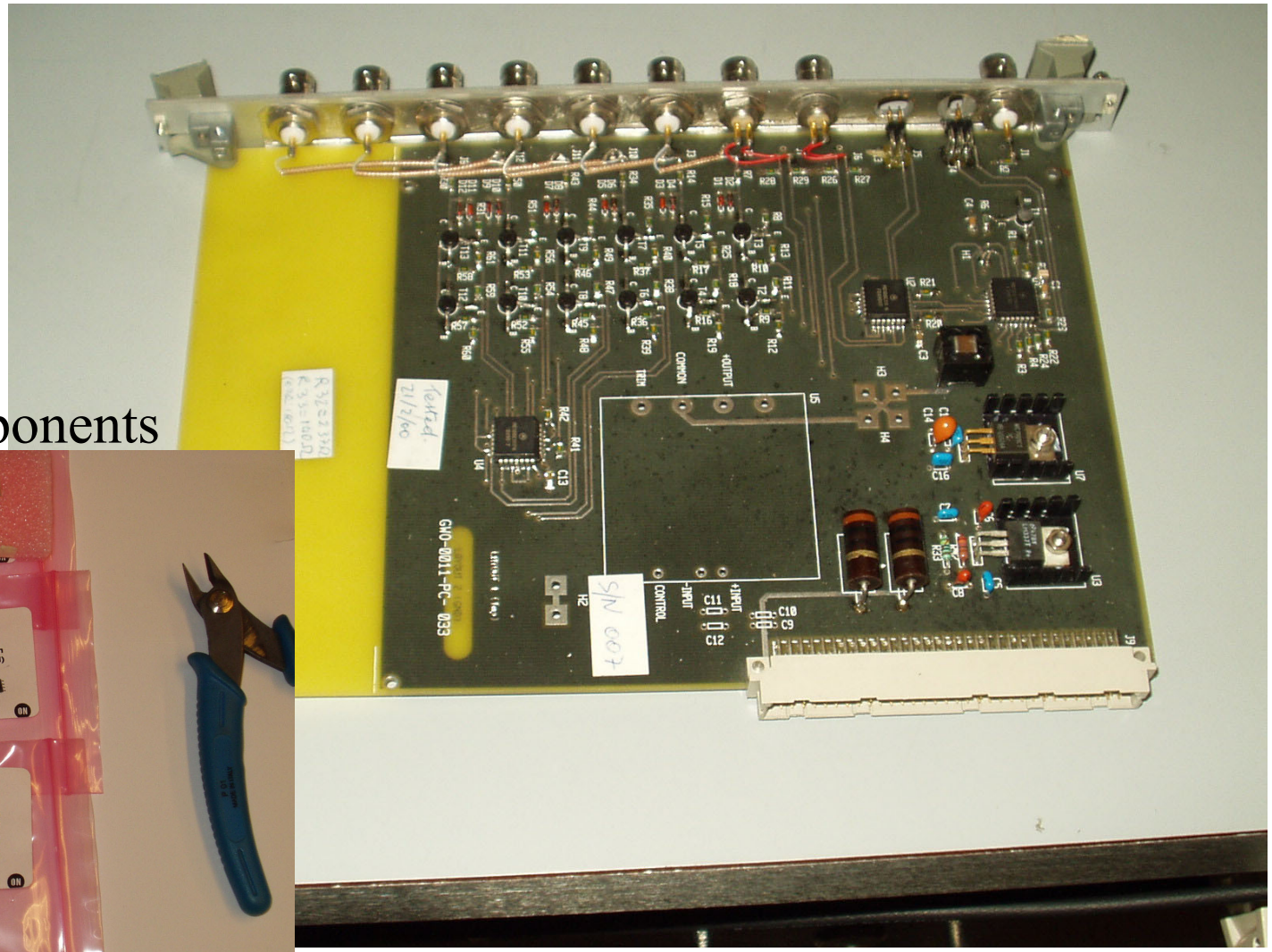
AC CHARACTERISTICS (V_{EE} = –3.0 V to –5.5 V; V_{CC} = 0 V or V_{CC} = 3.0 V to 5.5 V; V_{EE} = 0 V [Note 25])

Symbol	Characteristic		–40°C			25°C			85°C			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{COUNT}	Maximum Frequency	Q, $\overline{TC}$		> 1			> 1			> 1		GHz
		COUT/$\overline{COUT}$		> 800			> 800			> 800		MHz
t_{PLH} t_{PHL}	Propagation Delay	(10) CLK to Q	300	450	600	350	500	650	400	580	700	ps
		(10) MR to Q	300	400	500	400	500	600	450	580	700	
		(10) CLK to $\overline{TC}$	350	420	550	400	500	600	400	550	700	
		(10) MR to $\overline{TC}$	250	350	450	350	450	550	400	510	600	
		(10) CLK to COUT	400	470	650	450	550	700	450	600	800	
		(10) MR to COUT	300	400	550	400	500	650	450	580	700	
		(100) CLK to Q	350	500	650	400	550	700	480	630	780	
		(100) MR to Q	400	550	700	450	590	750	520	670	820	
		(100) CLK to $\overline{TC}$	350	500	650	400	550	700	480	630	780	
		(100) MR to $\overline{TC}$	400	550	700	450	590	750	520	670	820	
		(100) CLK to COUT	400	550	750	450	600	800	530	680	880	
		(100) MR to COUT	450	600	800	500	640	850	570	720	920	
t_S	Setup Time	Pn	100	–50		100	–50		100	–50		ps
		$\overline{DE}$	500	300		500	300		500	300		
		$\overline{PE}$	500	300		500	300		500	300		
		TCLD	500	300		500	300		500	300		
t_H	Hold Time	Pn	100	–50		100	–50		100	–50		ps
		$\overline{DE}$	500	300		500	300		500	300		
		$\overline{PE}$	500	300		500	300		500	300		
		TCLD	500	300		500	300		500	300		
t_{JITTER}	Cycle–to–Cycle Jitter			0.2	< 1		0.2	< 1		0.2	< 1	ps
t_{RR}	Reset Recovery Time		200	80		200	80		200	80		ps
t_{PW}	Minimum Pulse Width CLK, MR		550	300		550	300		550	300		ps
t_r t_f	Output Rise/Fall Times 20% – 80%		120	210	320	120	220	320	150	250	450	ps

25. Measured using a 750 mV source, 50% duty cycle clock source. All loading with 50 ohms to V_{CC}–2.0 V.

Modules and components

ECL/NIM trigger fan out



3GHz ECL components