weeroc

High-end Microelectronics Design

Recent developments in fast timing ASICs for particle physics and medical imaging

FATA 2019

3rd Sept 2019, Acireale, Catania

Salleh Ahmad

Major trends

- HL-LHC upgrade
  - Require new ASICs + timing measurements (< 50ps) for event pileup mitigation
- Better detector timing resolution for PET
  - Intrinsic time resolution of SiPM is improving (SPTR ~100ps range)
  - CTR <100ps : increase sensitivity, dose reduction & direct 3D imaging (10ps)
- High channel integration & compact (4-side abutable SiPM, TSV)
  - less space & low power budget for higher number of channels
- Cost effective
  - Order of magnitude in number of channels, not in budget…

Institution & companies

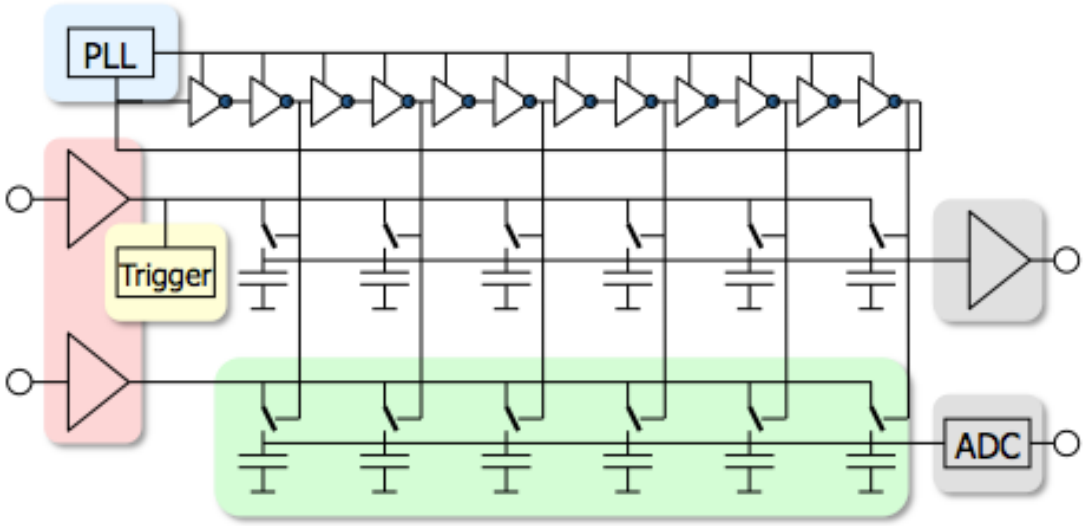
Research Institutes & Universities

- Heidelberg, Germany
- IN2P3, France
  - Micrhau, Omega, LAL
- CEA, IRFU, France
- CERN, Switzerland
- Bari, Italy
- FPACS, AGH, Krakow, Romania
- Hawaii, USA
- Chicago, USA
- PSI, Switzerland
- Sherbrooke, canada
- ICC-UB, Spain

Companies

- IDEAS
- PetSys
- Weeroc

Not exhaustive list



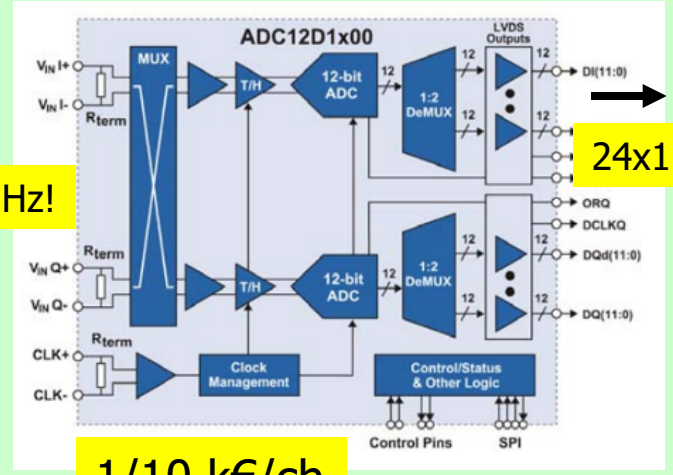
SCA WAVEFORM DIGITIZER INTEGRATED CIRCUIT

Waveform sampling & stretching time to get ps resolution

Waveform digitizers [S. Ritt]

FADCs

- 8 bits – 3 GS/s – 1.9 W → 24 Gbits/s
- 10 bits – 3 GS/s – 3.6 W → 30 Gbits/s
- 12 bits – 3.6 GS/s – 3.9 W → 43.2 Gbits/s
- 14 bits – 0.4 GS/s – 2.5 W → 5.6 Gbits/s

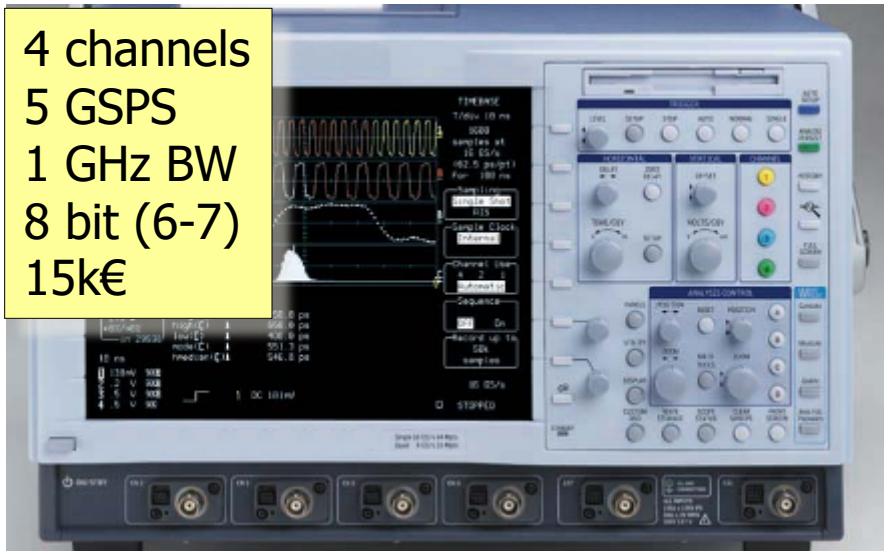


1.8 GHz!

24x1.8 Gbits/s

1/10 k€/ch

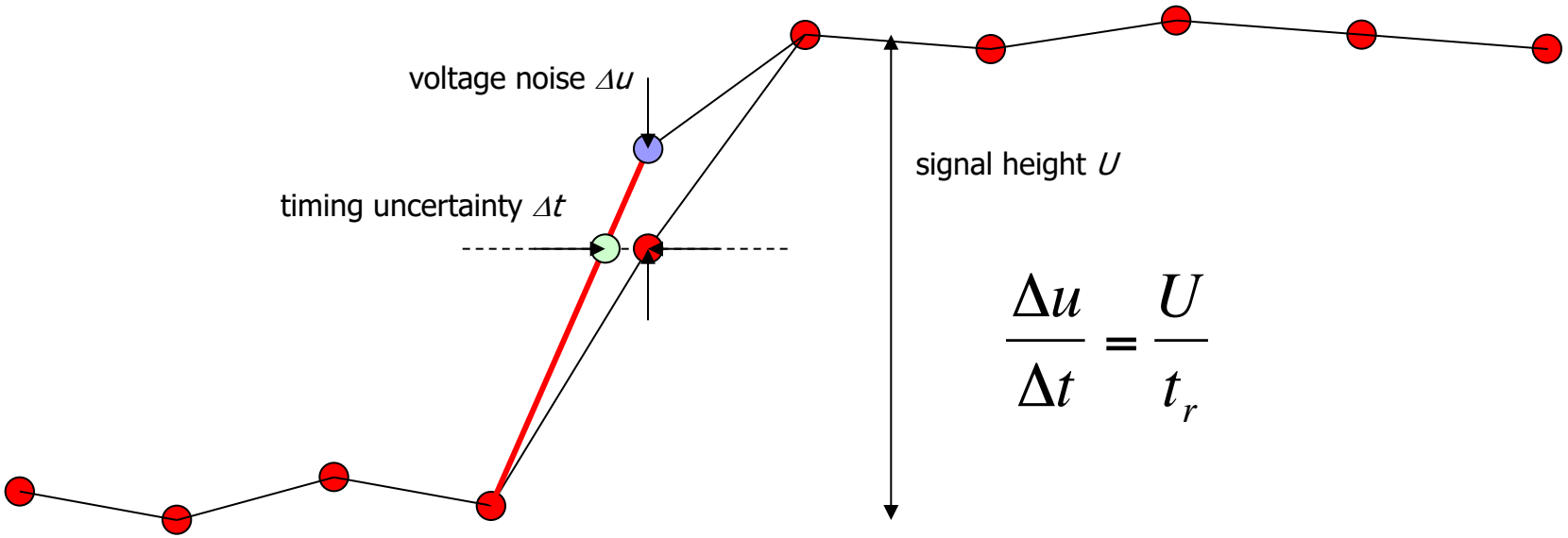
PX1500-4:
2 Channel
3 GS/s
8 bits



4 channels
5 GSPS
1 GHz BW
8 bit (6-7)
15k€

4 channels
5 GSPS
1 GHz BW
11.5 bits
900€
USB Power

How is timing resolution affected?



$$\frac{\Delta u}{\Delta t} = \frac{U}{t_r}$$

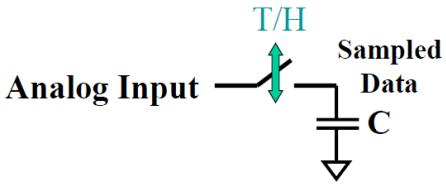
$$\Delta t = \frac{\Delta u}{U} \cdot \frac{1}{\sqrt{3 f_s \cdot f_{3dB}}}$$

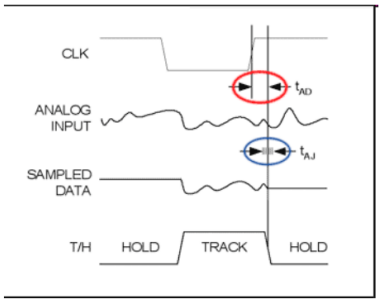
Assumes zero aperture jitter

	U	Δu	f_s	f_{3db}	Δt
today:	100 mV	1 mV	2 GSPS	300 MHz	~10 ps
optimized SNR:	1 V	1 mV	2 GSPS	300 MHz	1 ps
next generation:	1V	1 mV	10 GSPS	3 GHz	0.1 ps

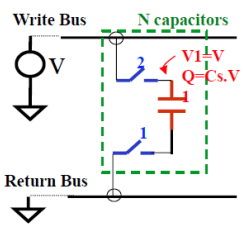
Underlying technology

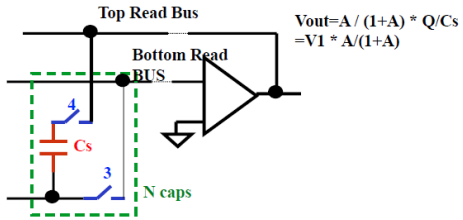
- Track and Hold (T/H)



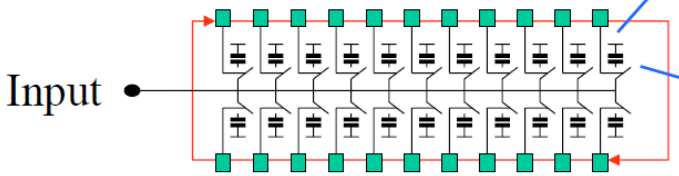


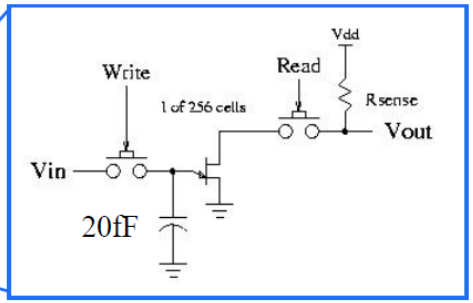
- Pipelined storage = array of T/H elements, with output buffering



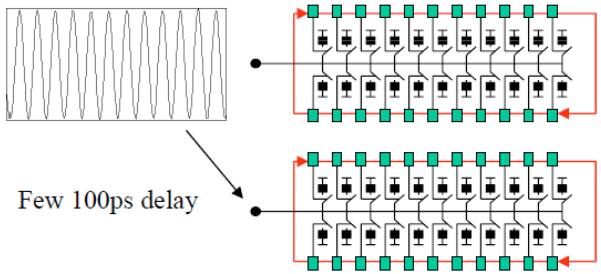


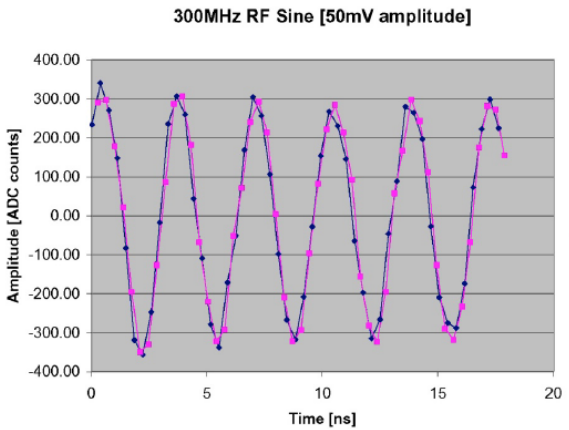
- Write pointer is ~few switches closed @ once





Tiny charge: 1mV ~ 100e-



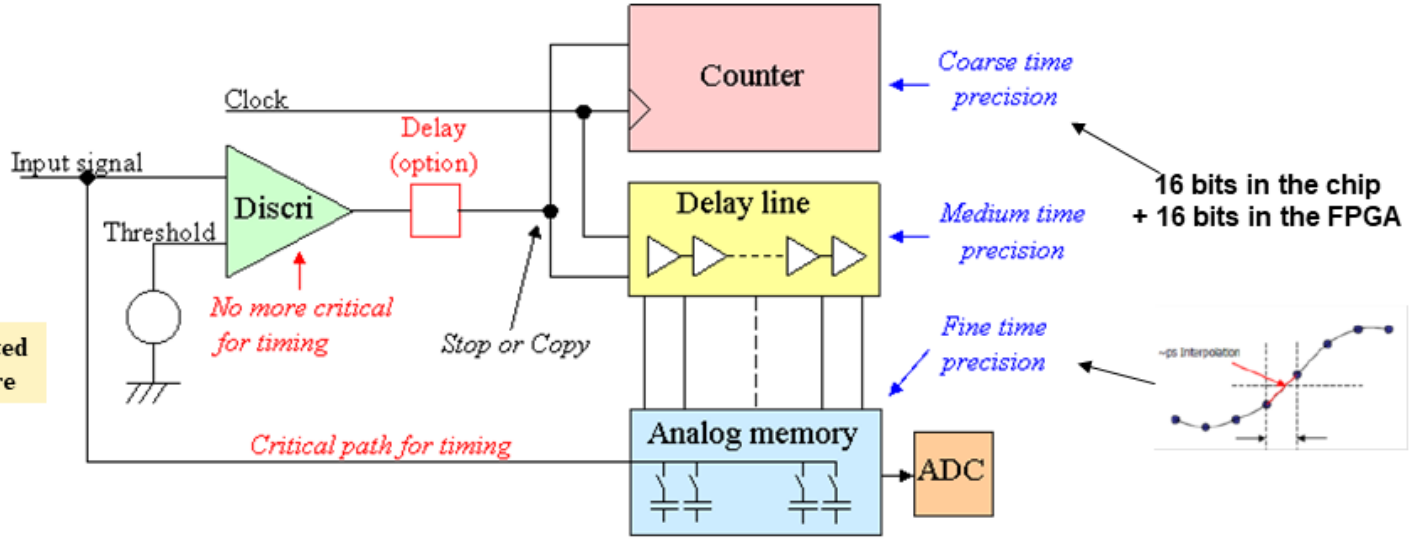


Courtesy : Gary Varner

Recent ASIC : SAMPIC v3

THE NEW « WAVEFORM TDC » STRUCTURE

- The **Waveform TDC**: new concept based on **our know-how and innovating ideas**
- **Mix of DLL-based TDC and of analog-memory based Waveform Digitizer**
- Time information is given by association of contributions:
  - **Coarse** = Timestamp Gray Counter (few ns step)
  - **Medium** = DLL locked on the clock to define region of interest (100 ps minimum step)
  - **Fine** = **samples of the waveform** (**interpolation** will give a precision of a few ps rms)
- **Digitized waveform shape will give access to amplitude and charge**
- **Conversely to TDC, discriminator is used only for triggering, not for timing**



© Patented Structure

Courtesy: Dominique Breton/Eric Delagnes & al → See talk by D. Breton : Fast electronics for TOF in Nuclear Physics

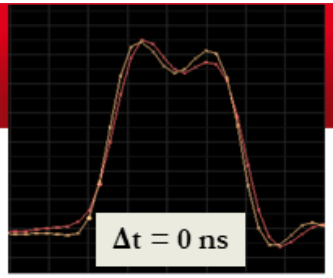
SAMPIC v3 Time Resolution

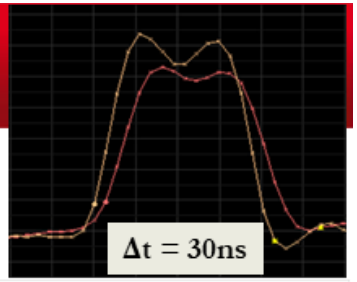
TIME RESOLUTION

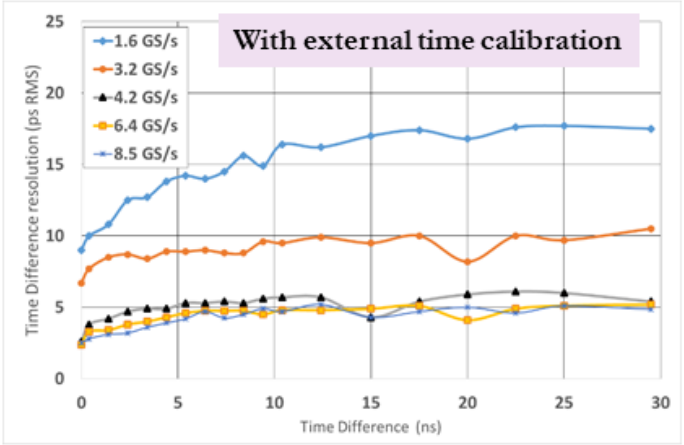
- The new DLL has been re-worked for improving the resolution for the lower sampling frequencies
- Delays made by a cable box => rise time degrades with delay …

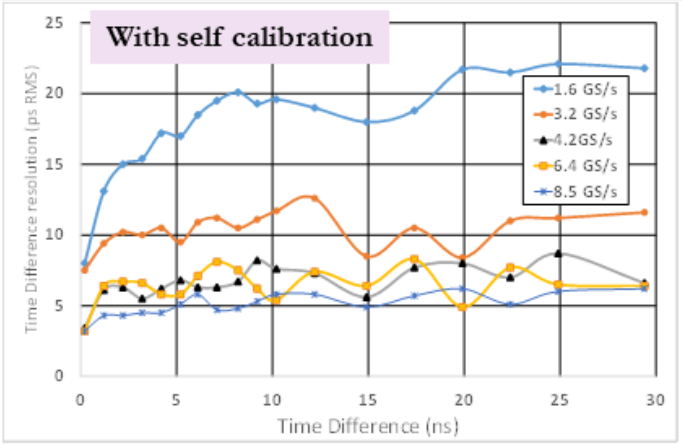
- With external time-calibration :
  - A TDR of ~5 ps rms if 4.2< Fs<8.5 GS/s
  - The TDR < 10 ps rms for 3.2 GS/s
  - TDR < 18 ps rms for 1.6 GS/s

- WITH **self-calibration**
  - Limited jitter degradation (~20%)
  - Permits full integration in compact detection systems …



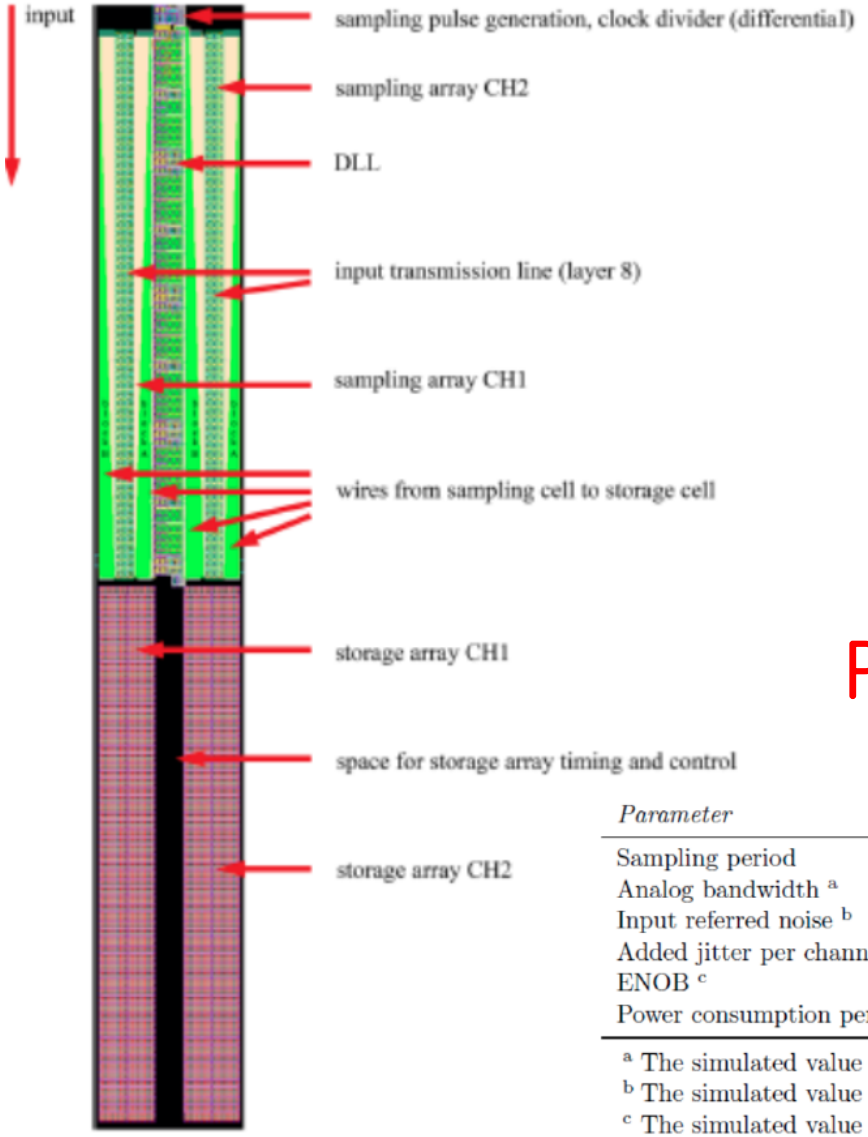






Courtesy: Dominique Breton/Eric Delagnes & al → See talk by D. Breton : Fast electronics for TOF in Nuclear Physics

Example of ASIC in development (Univ of Hawaii)



RFpix1 ASIC Design Status

Key Design components verified

Work still needed on the digital control/address decoding

Pushing towards fs resolution

Parameter	*Desired value*	*Simulated value*
Sampling period	50 ps @20 GS/s	50 ps @20 GS/s
Analog bandwidth [a]	$\approx 3\ GHz$	$\approx 3.56\ GHz$
Input referred noise [b]	$\leq 0.5\ mV_{RMS}$	$\approx 1.05\ mV_{RMS}$
Added jitter per channel	$\approx 40\ fs$	$\approx 29\ fs$
ENOB [c]	≥ 10	≈ 9.6
Power consumption per channel [b]	$40\ mA$	$41.71\ mA$

[a] The simulated value is the tracking bandwidth of the SCA.
[b] The simulated value does not take into account the input buffer.
[c] The simulated value does not take into account distortion.

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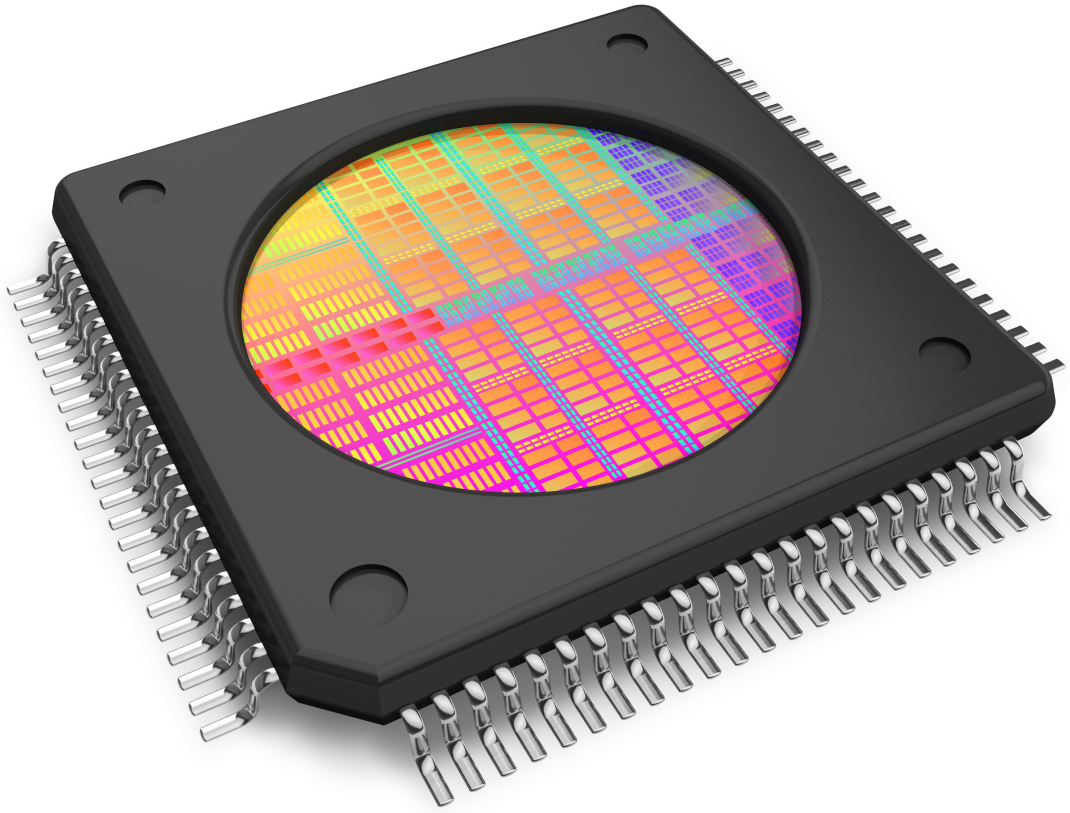
Courtesy : Gary Varner

Waveform digitizer worldwide state of the art

ASIC	# chan	Depth/chan	Time Resolution [ps]	Vendor	Size [nm]	Year
LABRADOR 3	8	260	16	TSMC	250	2005
BLAB	1	65536	1-4	TSMC	250	2009
STURM2	8	4x8	<10 (3GHz ABW)	TSMC	250	2010
DRS4	8	1024	~1 (short baseline)	IBM	250	2014
PSEC4	6	256	~1 (short baseline)	IBM	130	2014
RITC3	3	Continuous	TBD	IBM	130 ?	---
PSEC5	4	32768	TBD	TSMC	130	---
DRS5	8/16?	128x32	TBD	UMC	110	---
SamPic	16	64	~few [pic 0]	AMS	180	[2014]
RFpix	128?	TBD	<= 100fs (target)	TSMC	130 ?	---

Courtesy : Gary Varner



MICROELECTRONICS CIRCUITS

Things you can use to build a system based on detector readout

Readout ASIC (SiPM, Si Diode & LGAD)

Circuit name	Institute	# ch.	Input	Info
NINO	CERN	8	Current	Differential, ToT, ToF, 32 ch.
PETA6	ZITI,Heidelberg	36	Current	Integrator, ADC,TDC
PETIROC2	IN2P3/Omega-Weeroc	32	Voltage	ADC, TDC, 2 Trigger, ToF
Triroc1	IN2P3/Omega-Weeroc	64	Current	ADC,TDC, 2 trigger
PARISROC2	IN2P3/Omega	16	Voltage	SoC for large PM area
TOFPET2	Petsys	64	Current	ToT, TDC 25ps bin, ToF
STIC	KIP,Heidelberg	64	Current	ToT, 2 threshold, ToF
MuTrig	KIP,Heidelberg	32	Current	Differential,TDC, 2 threshold
Flextot/HRFlextot	ICC-UB	32	Current	Differential,TDC, 2 threshold
ALTIROC	IN2P3/Omega, LAL,LPC, SLAC...	25	Current	ToA, TOT
HGCROC	IN2P3/Omega, LLR, IRFU, Imperial, CERN....	32	Current	ADC, ToA, TOT
SKIROC2_CMS	IN2P3/Omega, CERN...	64	Current	ADC, ToA, TOT

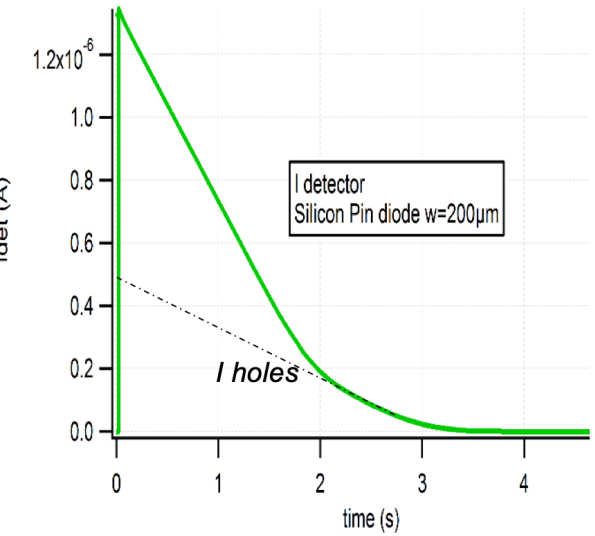
Timing needs in particle physics

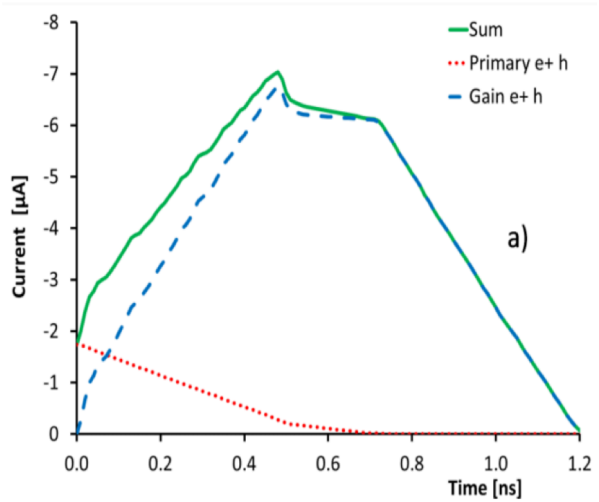
- HL-LHC → time of arrival for events pileup mitigation
- Medical imaging (PET) → Single photo electron timing resolution & Coincidence Timing Resolution

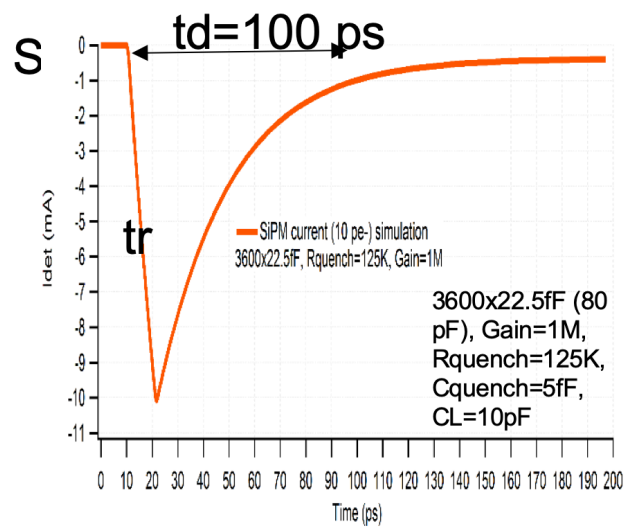
- PN diode w =200µm
- Very short rise time : tr~10ps
- Relatively long «drift time» : td~2ns

- LGAD sensor w =50µm
- rise time : tr~500ps
- Decay time» : td~700ps

- SiPM detector (10pe-)
- very short rise time : tr~10 ps
- Short duration : td~100ps),



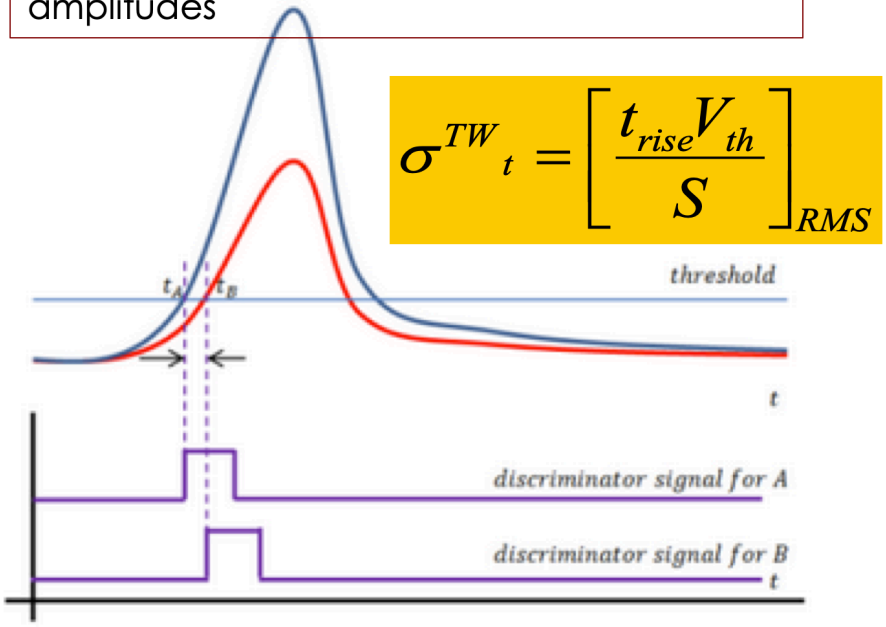




© Harmut Sadrozinski (Santa Cruz) "the beautiful risetime of the detector is spoilt by the electronics"

Timewalk and Jitter

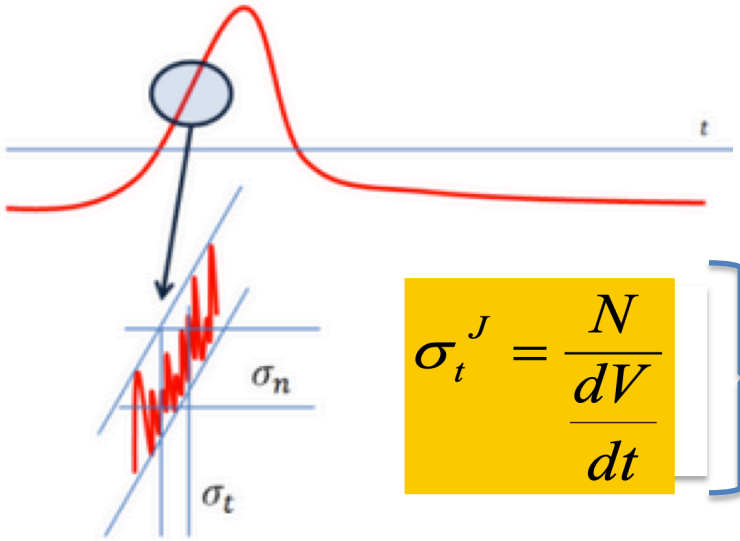
Time walk: the voltage value Vo is reached at different time for signal of different amplitudes



$$\sigma^{TW}{}_t = \left[\frac{t_{rise} V_{th}}{S}\right]_{RMS}$$

Time walk effect

Jitter: the noise is summed to the signal, causing amplitude variations



$$\sigma_t{}^{J} = \frac{N}{\frac{dV}{dt}}$$

prop to 1/√BW

Jitter effect

Due to the physics of signal formation **Mostly due to electronic noise**

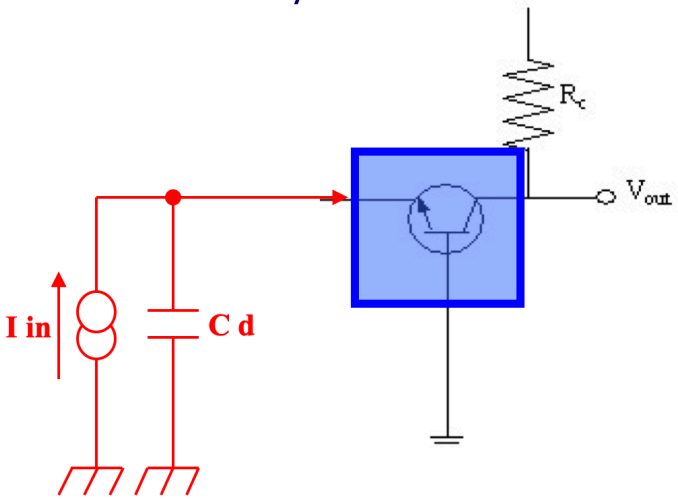
$$\sigma_t{}^2 = \left(\frac{t_{rise}}{S/N}\right)^2 + \left(\left[\frac{t_{rise} V_{th}}{S}\right]_{RMS}\right)^2 + \left(\frac{TDC_{bin}}{\sqrt{12}}\right)^2$$

Jitter | Time Walk | TDC

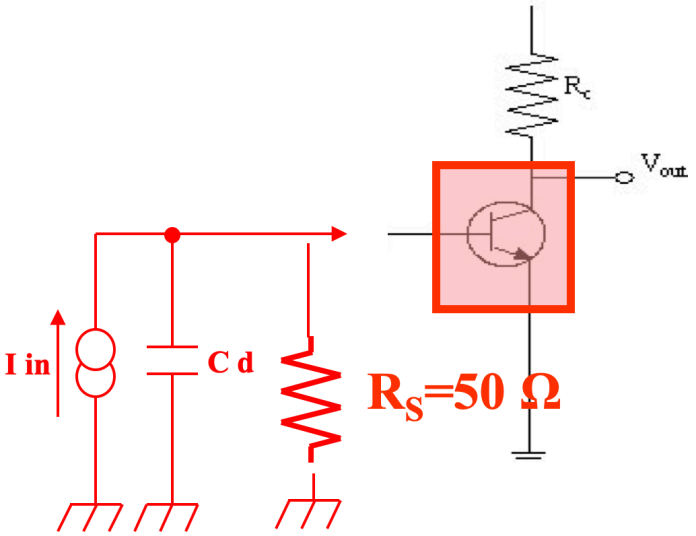
High Speed configuration

- Open loop configurations : current conveyors, RF amplifiers
- Usually designed at transistor level MOS or SiGe

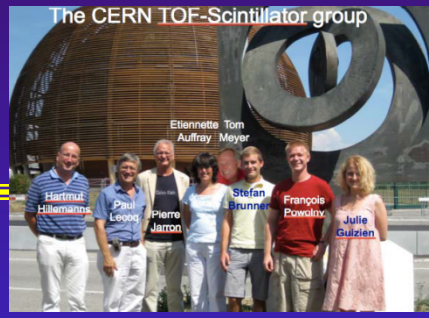
- **Current conveyors**
- Small Zin : current sensitive input
- Large Zout : current driven output
- Unity gain current conveyor
- E.g. : (super) common-base configuration
- Low input impedance : Rin=1/gm
- Transimpedance : Rc
- Bandwitdth : 1/2πRcCu > 1 GHz



- **RF amplifiers**
- Large Zin : voltage sensitive input
- Large Zout : current driven output
- Current conversion with resistor R_S
- E.g. common-emitter configuration
- Transimpedance : -gmRcRs
- Bandwitdth : 1/2πRsCt



NINO for PET

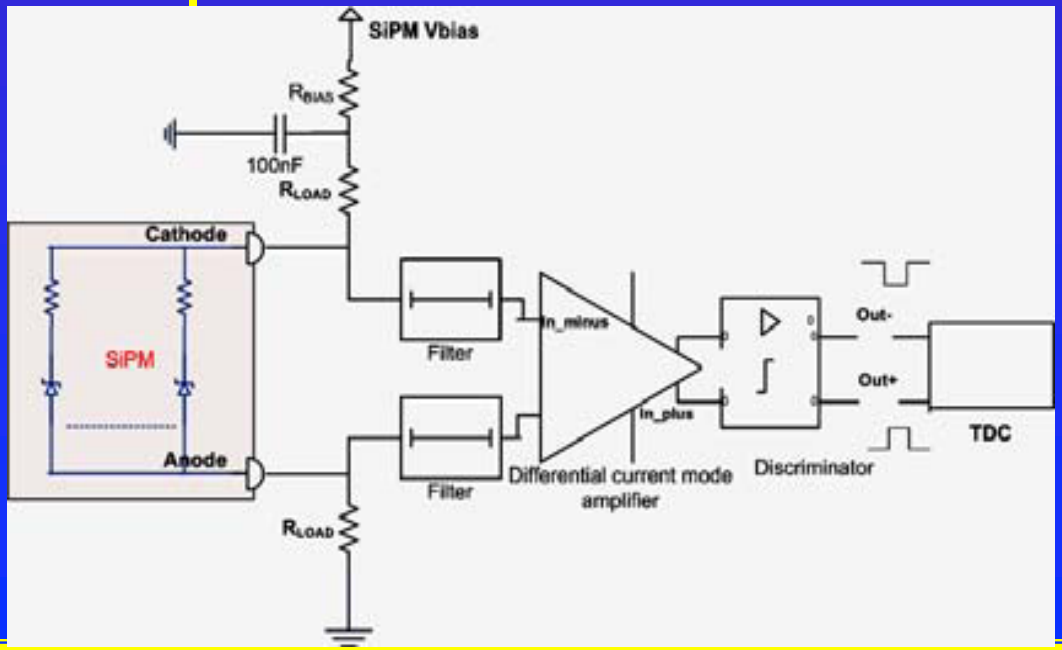


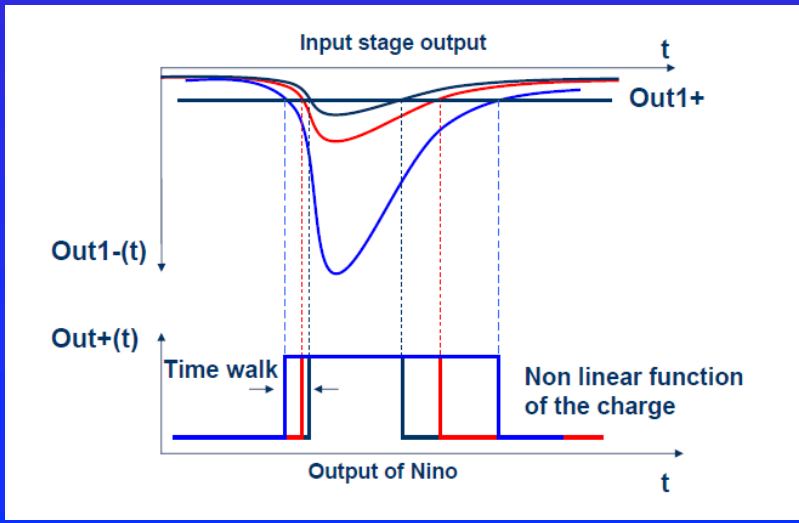
Application for TOF-PET

[P . Jarron, E. Auffray, S.E. Brunner, M. Despeisse, E. Garutti, M. Goettlich, H. Hillemanns, P. Lecoq, T. Meyer, F. Powolny, W. Shen, H.C. Schultz-Coulon, C. Williams - Time based readout of a silicon photomultiplier (SiPM) for Time Of Flight Positron EmissionTomography (TOF-PET) - 2009 IEEE Nuclear Science Symposium Conference Record, p. 1212 and NIM 617 (2010), p. 232

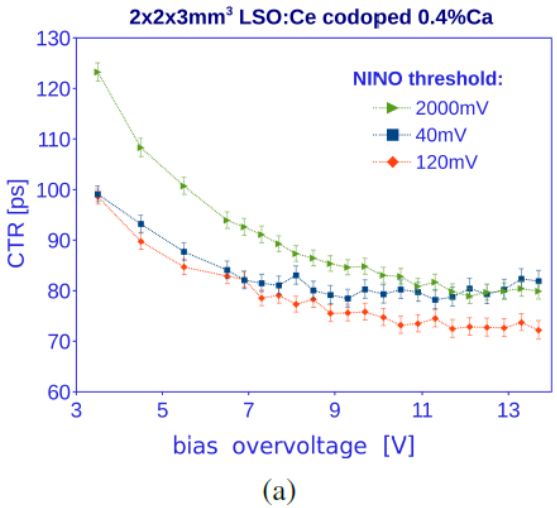
Differential connection of NINO to SiPM

NINO followed by CERN 25 ps HPTDC





NINO timing performances



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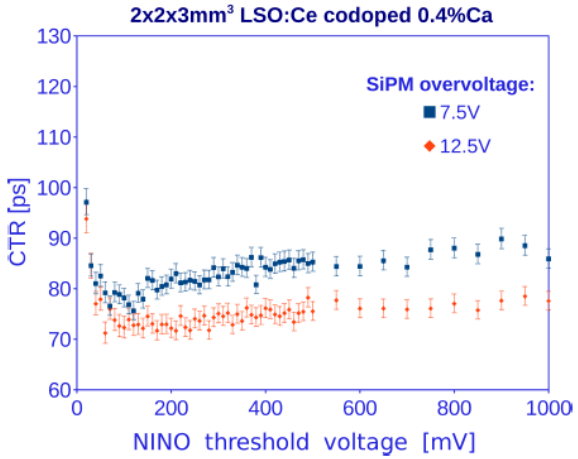

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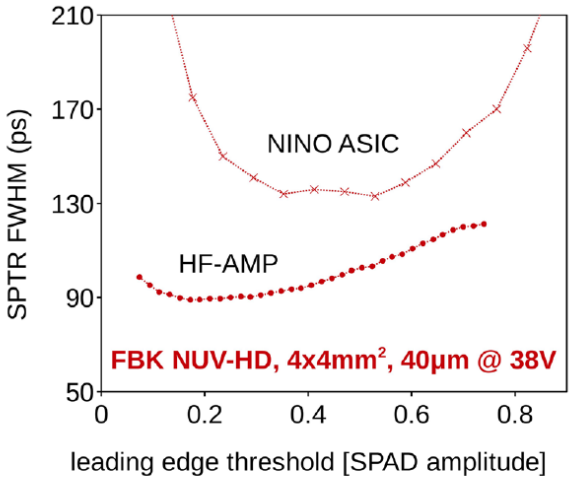
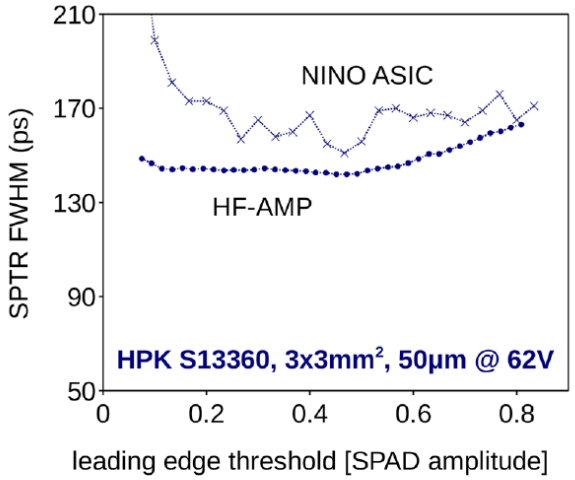


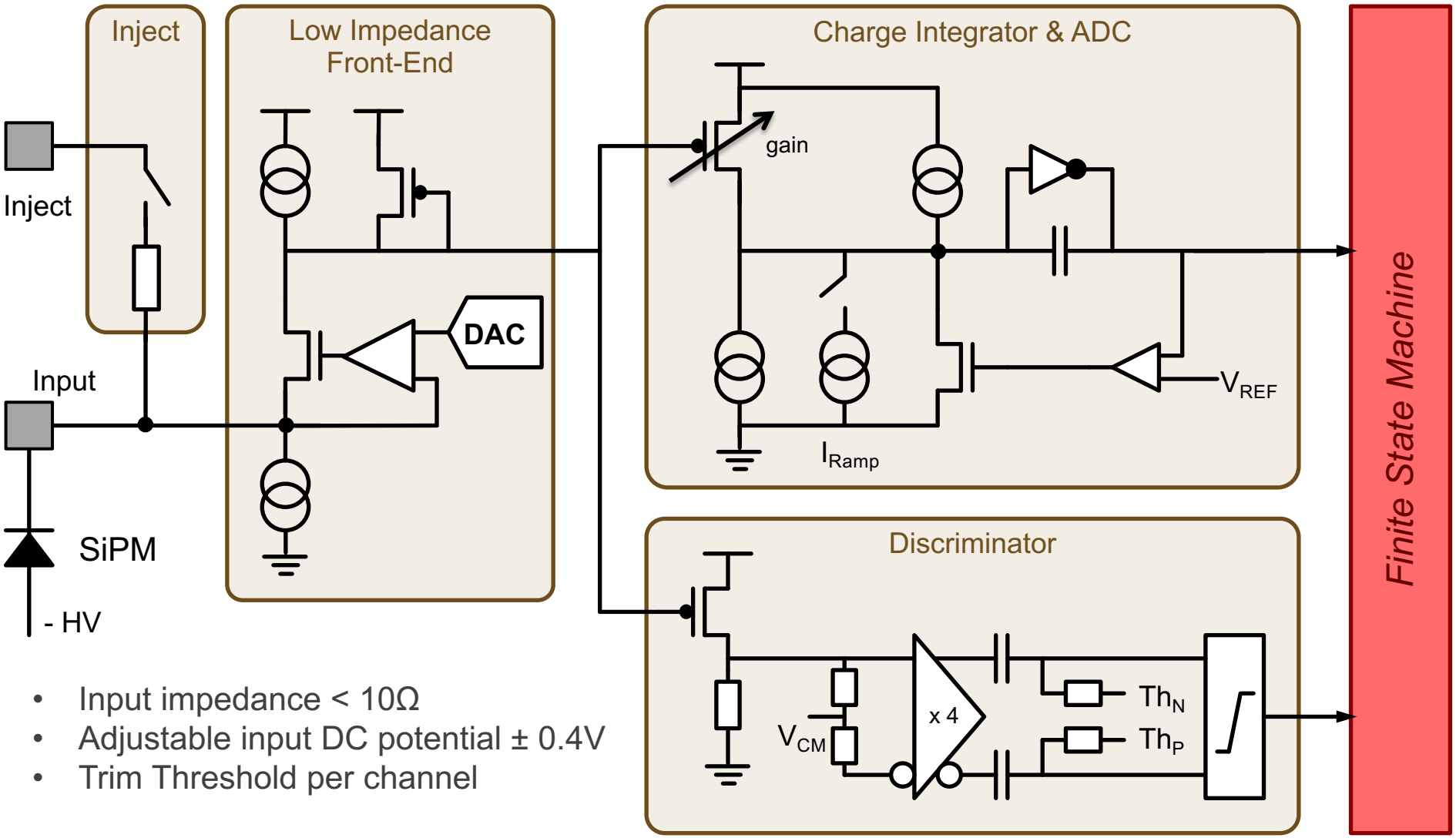
(a)



(b)

Nemallapudi et al, "Single photon time resolution of state of the art SiPMs" J. Instrum. 2016
Gundacker et al, "High-frequency SiPM readout advances measured coincidence time resolution limits in TOF-PET", Phys. Med. Biol. 2019

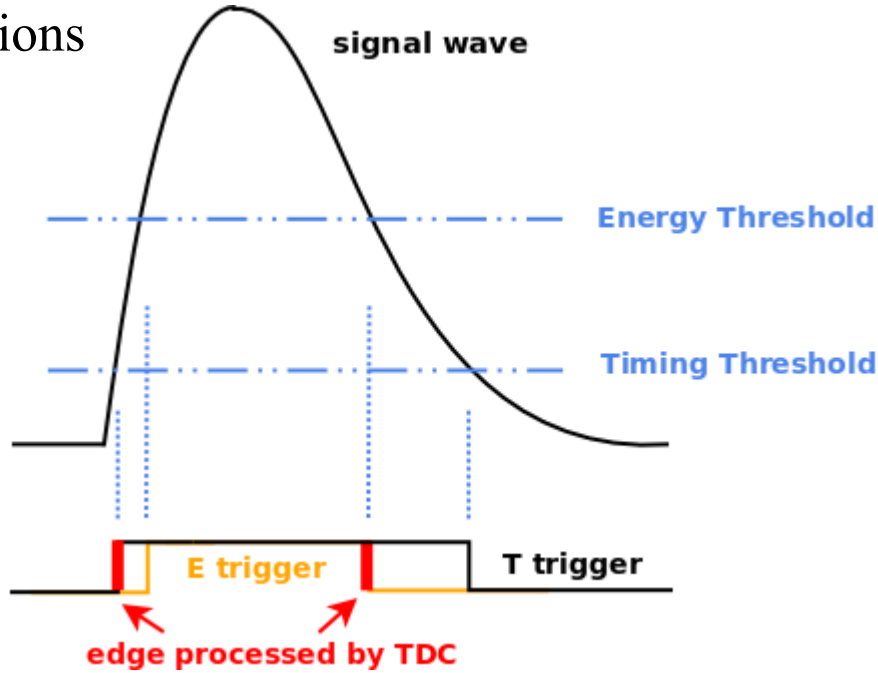
Single-Ended Front-end Channel PETA6

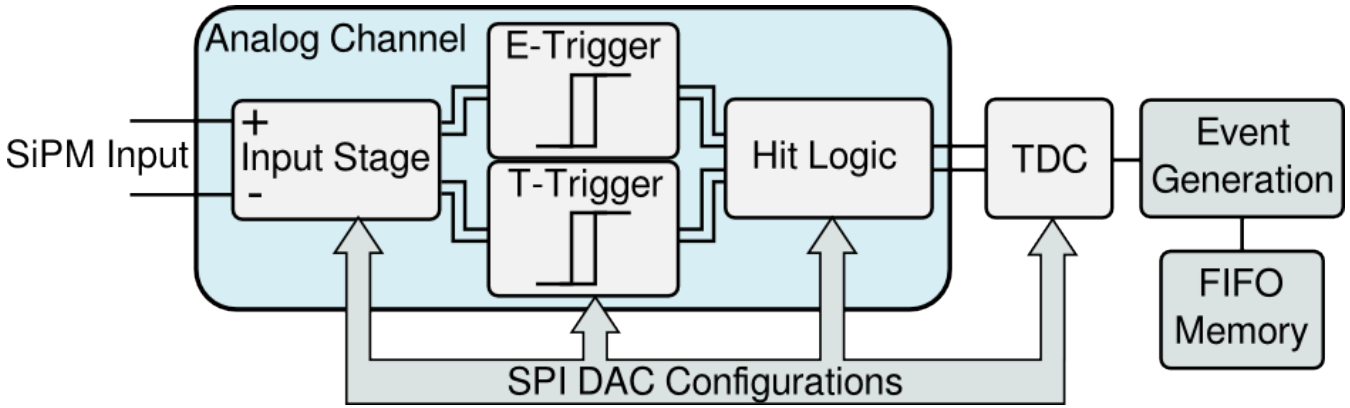


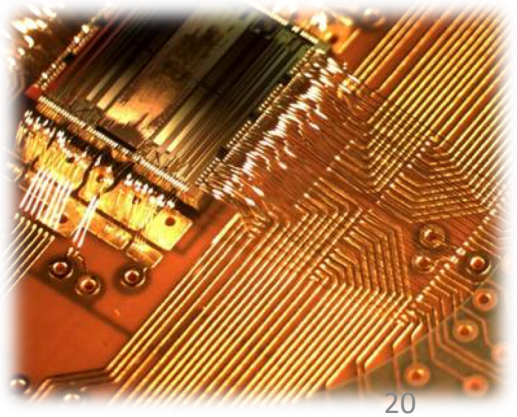
- Input impedance < 10Ω
- Adjustable input DC potential ± 0.4V
- Trim Threshold per channel

STiC : basic readout principle (Heidelberg, Wei Shen)

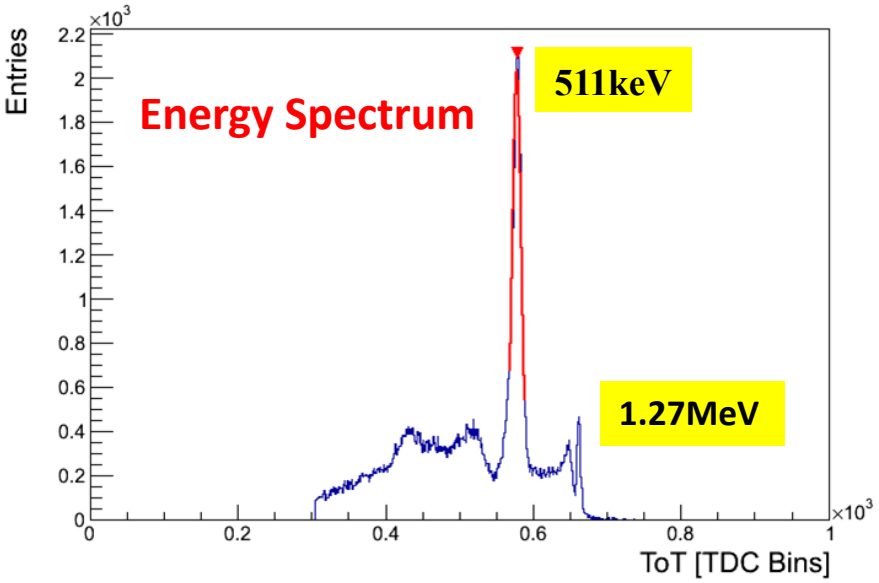
- 64-ch SiPM readout ASIC for ToF applications
- UMC 0.18μm CMOS
- Time + (linearized) Energy based on TDCs
- Analog Frontend + TDC + Digital
- SiPM bias tuning (~500mV)
- jitter < 20 ps
- Coincidence Resolution ~ 210ps FWHM
- Energy Resolution ~ 11%
- SiPM Dark Counts pile-up suppression

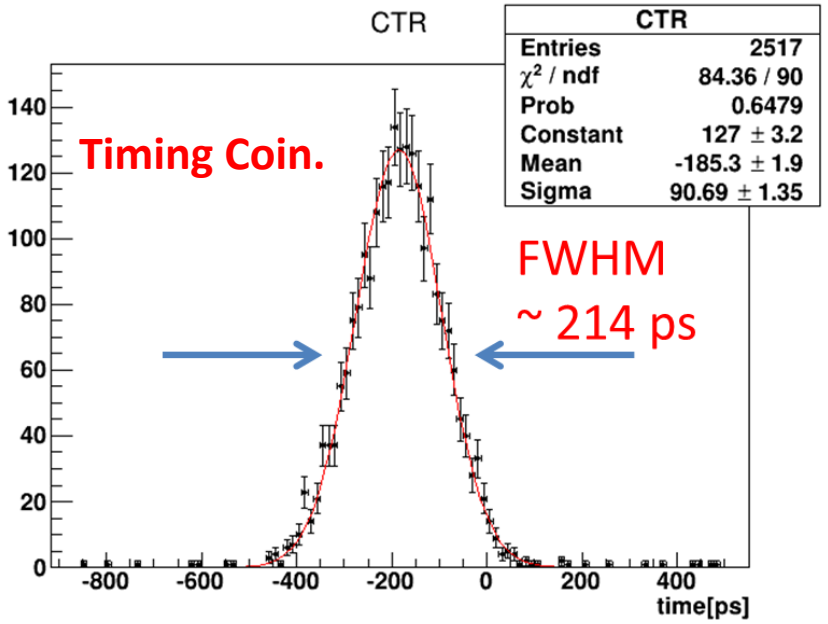




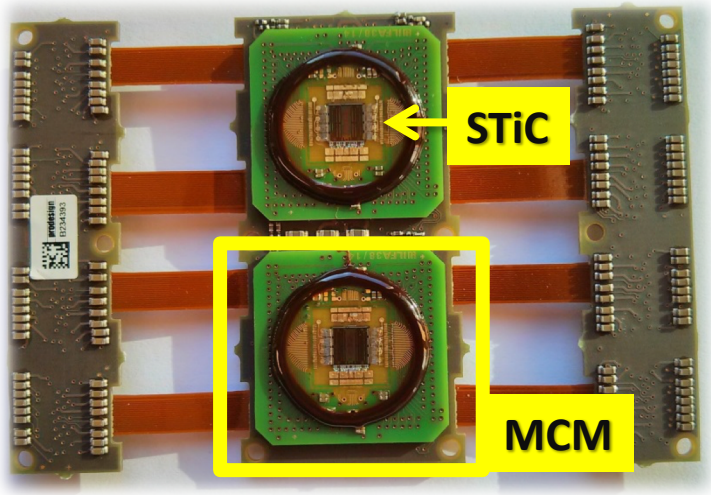


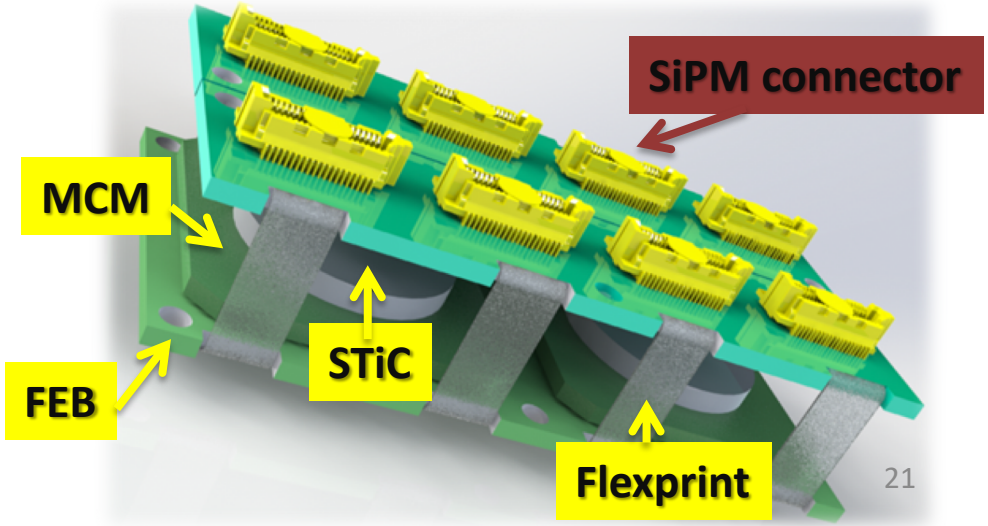
Na^{22} β^+ decay → coincidence with LSO 3.1x3.1x15 mm^3 +MPPC-S10625-33-50





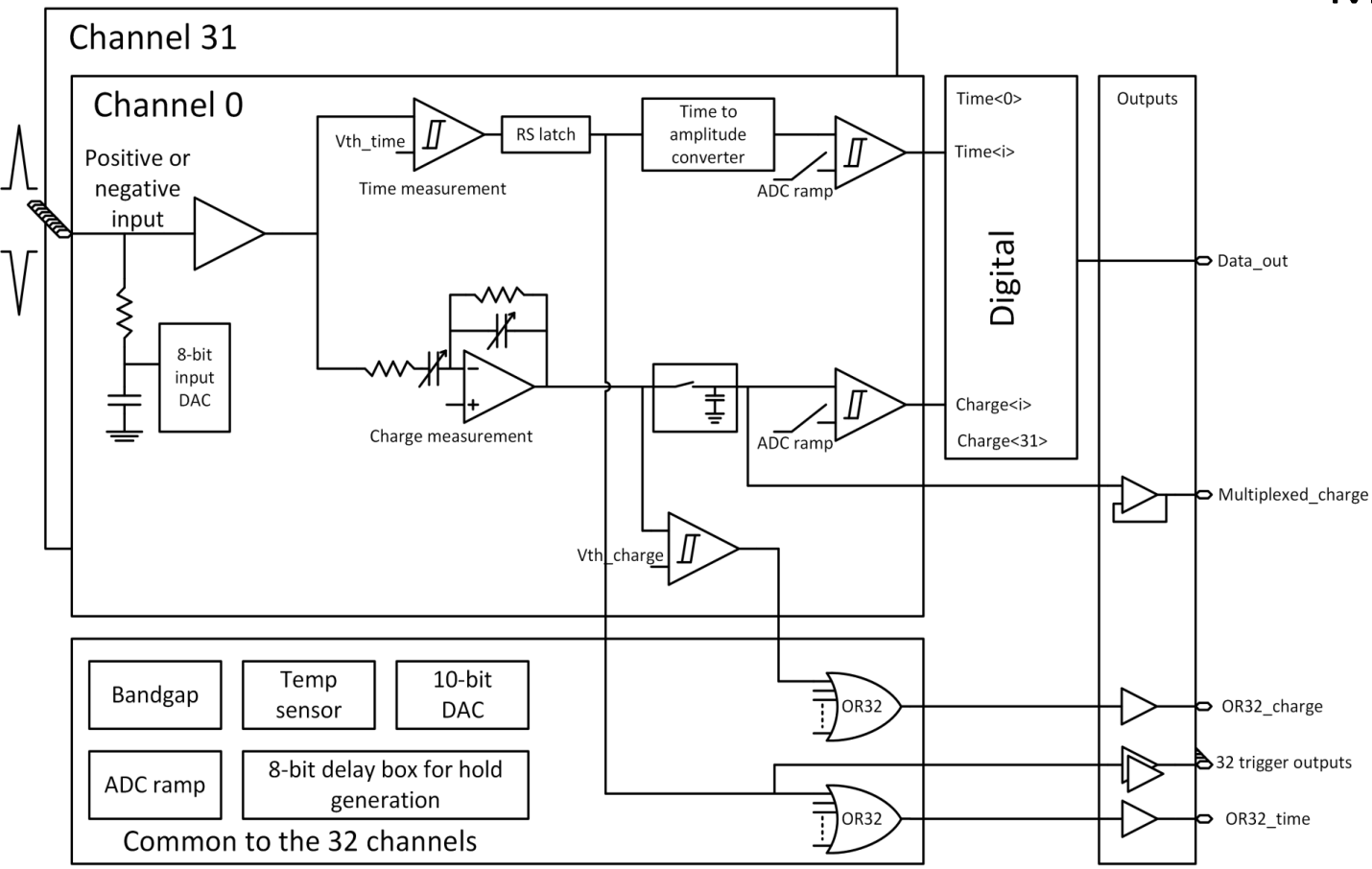
128 – ch frontend detector system : 2 STiCs wire-bonded on 2 MCMs then BGA-soldered on 1 FEB, MPPCs connected by Flexprint, yield > 96%

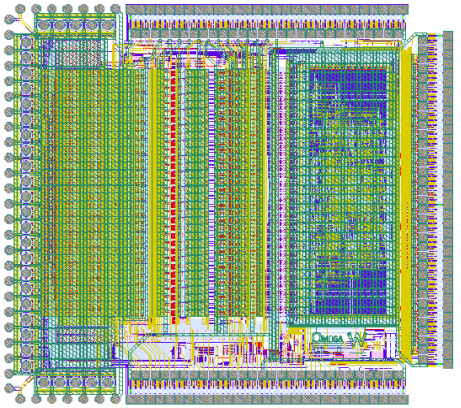




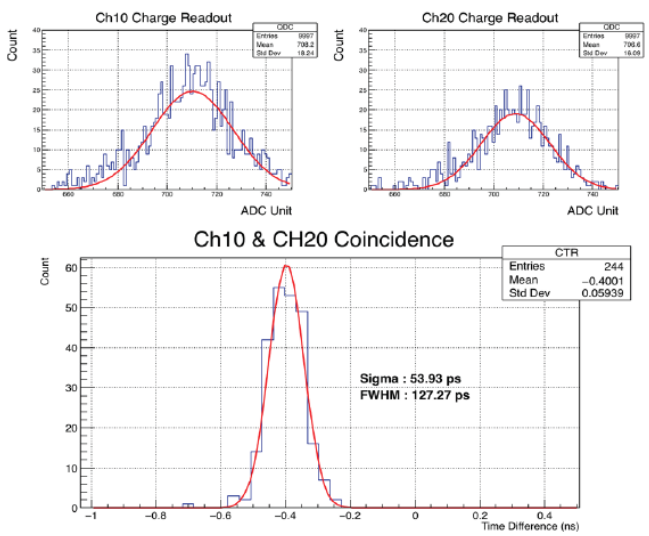
Petiroc 2

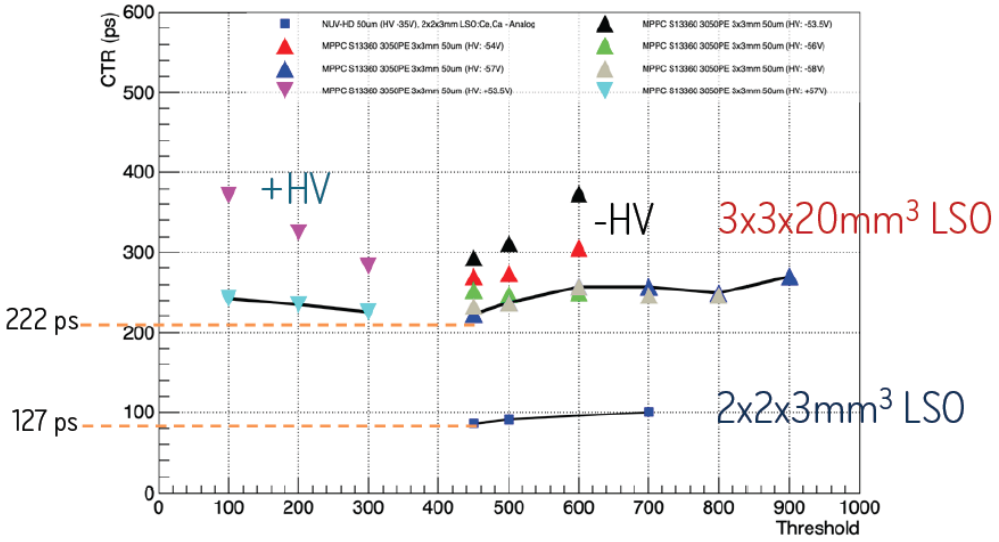
- 32 ch SiPM GHz readout ASIC, dual polarity, 100 fC-400 pC, 6 mW/ch
- 32 trigger outputs and multiplexed data output
- Embedded 10 bit ADC and 20 ps TDC
- Dual threshold : first photons and energy



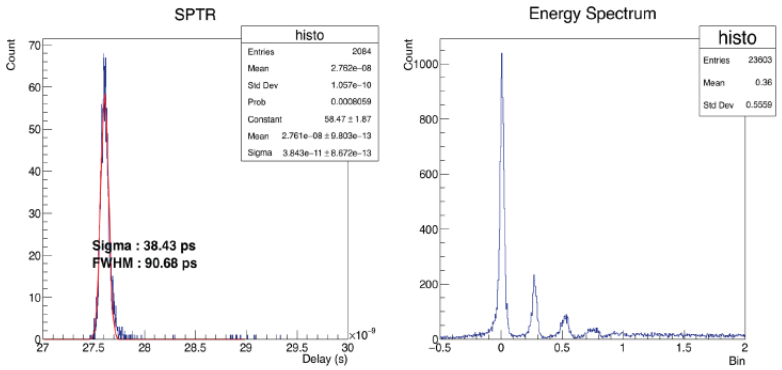


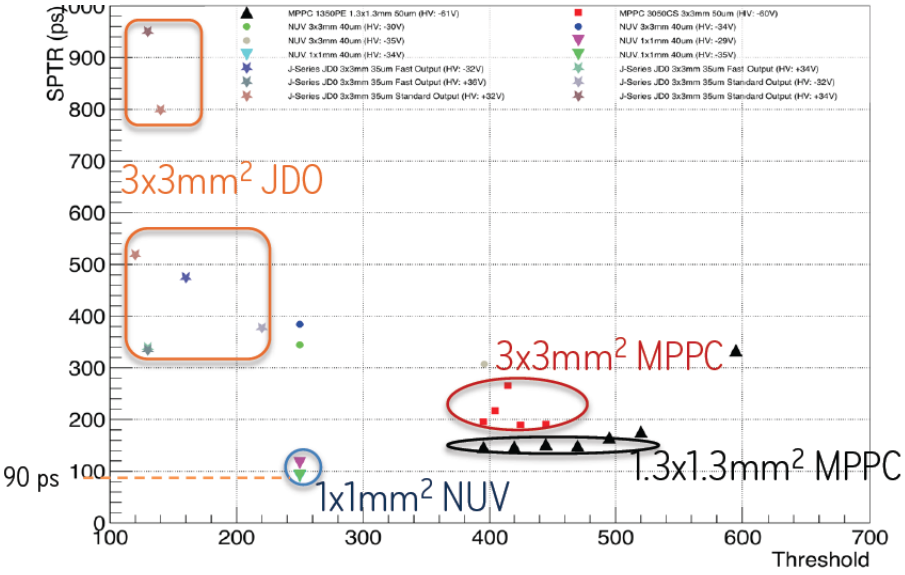
PETIROC2 timing performances





CTR ~ 127.3 ps FWHM (FBK NUV-HD & LSO:Ce,Ca 2x2x3 mm^3)

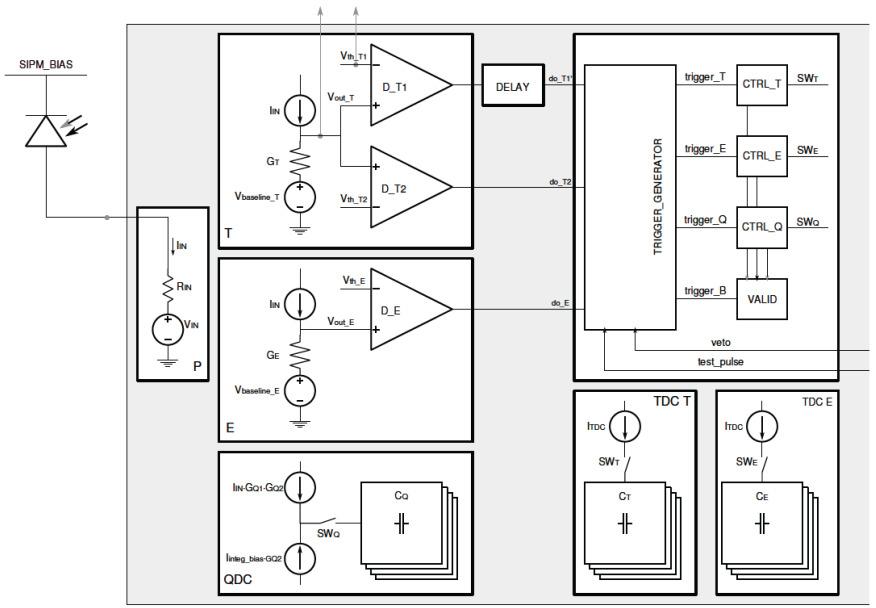


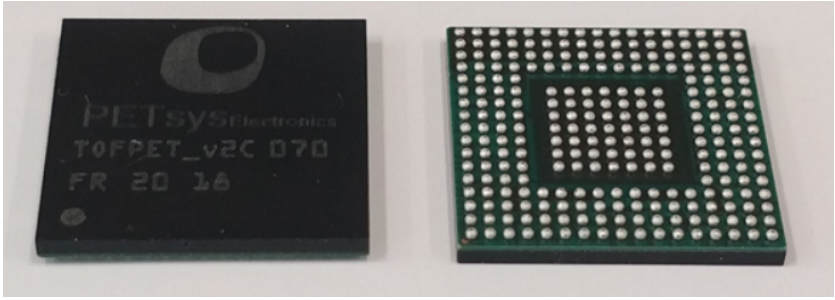


SPTR ~ 90.7 ps FWHM (FBK NUV 1x1mm^2)

TOFPET2 (Petsys Electronics)

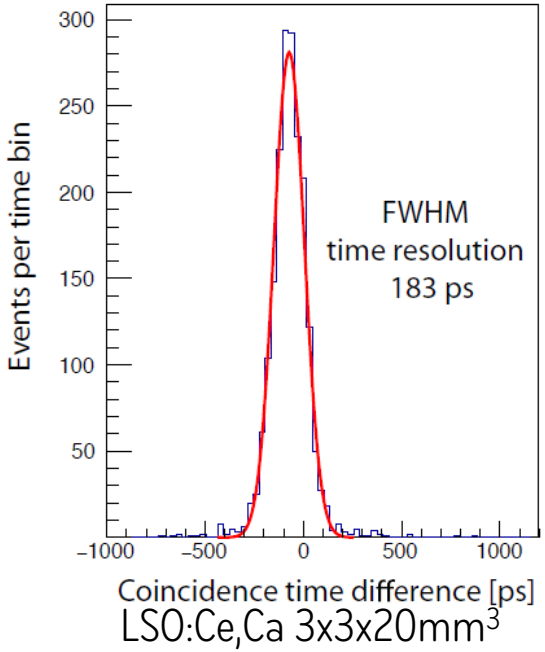
- Designed in standard CMOS 110 nm technology.
- Signal amplification and discrimination for each of 64 independent channels.
- Separately configurable t1, t2 and energy thresholds for each channel.
- Rejects dark counts without triggering, allowing to handle large dark cou rates.
- Configurable charge integration time up to one microsecond.
- Quad-buffered TDCs and charge integrators for each channel.
- The first branch is used for timing measurement.
- The second branch can either be used for time-over-threshold (ToT) or charge measurement with a Wilkinson ADC.
- Dynamic range: 1500 pC.
- TDC time binning: 30 ps.
- Gain adjustment per channel in the charge branch: 1, 1/2, 1/4, 1/8.
- On-chip charge calibration pulse generator with 6-bit programmable amplitude.
- Main clock frequency: 160-200 MHz.
- Configurable digital data output over 1, 2, or 4 LVDS data links at 2x the main clock frequency and single data rate (SDR) or double data rate (DDR).
- Max output data rate per ASIC: 3.2 Gb/s.
- Max event rate per channel: 600 kevents, 80 bits per event.
- Power dissipation per channel: 8.2 mW, for the recommended settings

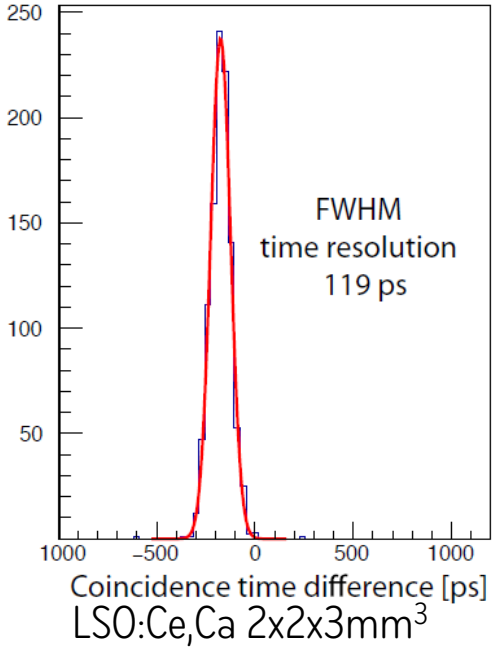




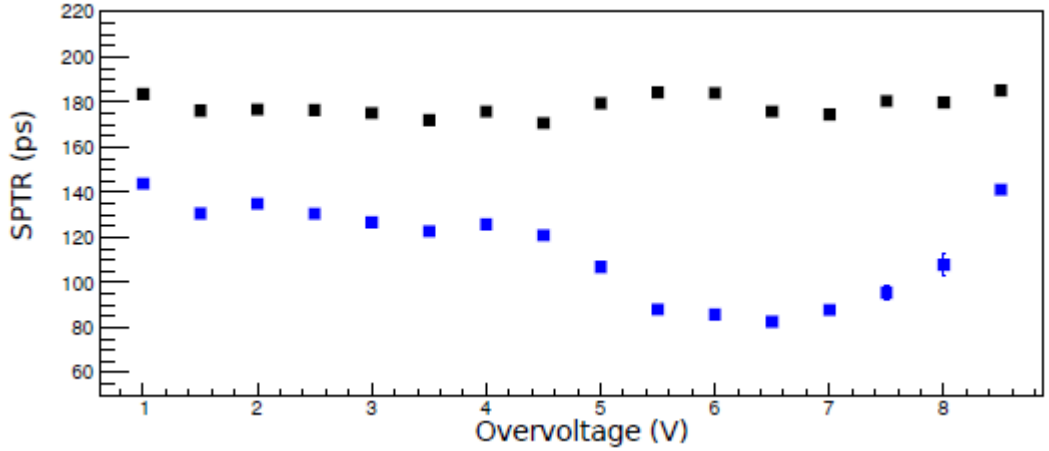
Bugalho et al, "Experimental characterization of the TOFPET2 ASIC" JINST 14 P03029 2019

TOFPET2 – Timing measurement





HPK S14160-3050HS & LSO:Ce,Ca



HPK S14160-3050HS

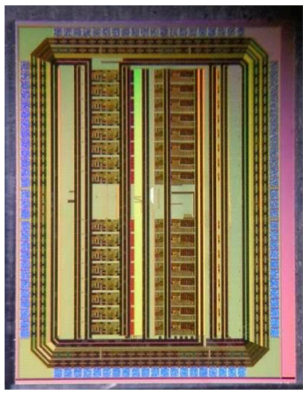
Bugalho et al, "Experimental characterization of the TOFPET2 ASIC" JINST 14 P03029 2019

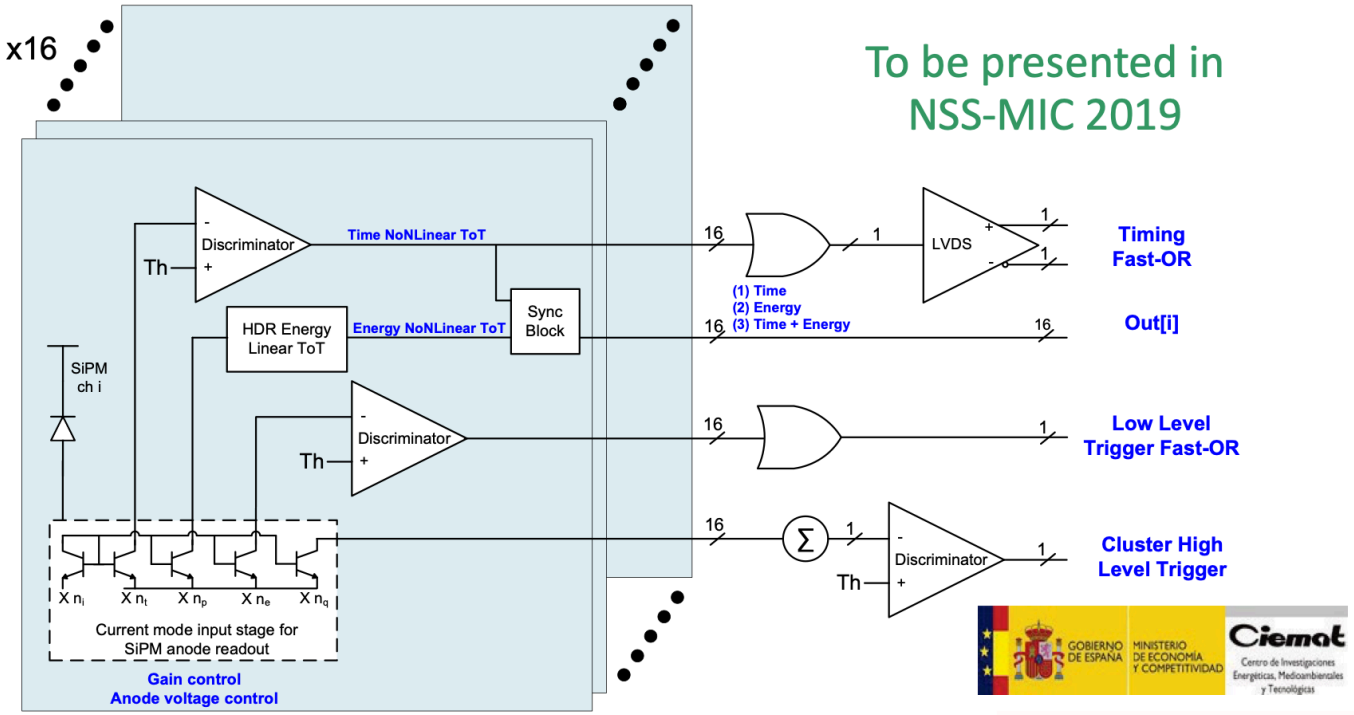
HRFlexToT: linearized ToT RO chip

- A new version of the FlexToT has been recently developed.
  - A linear Time over Threshold with higher resolution (>8bits)
  - Lower power consumption (about 3.5 mW/ch)
  - Different trigger levels and cluster trigger for monolithic crystals.
  - Different scintillator time constants.

HRFlexToT

180 nm CMOS

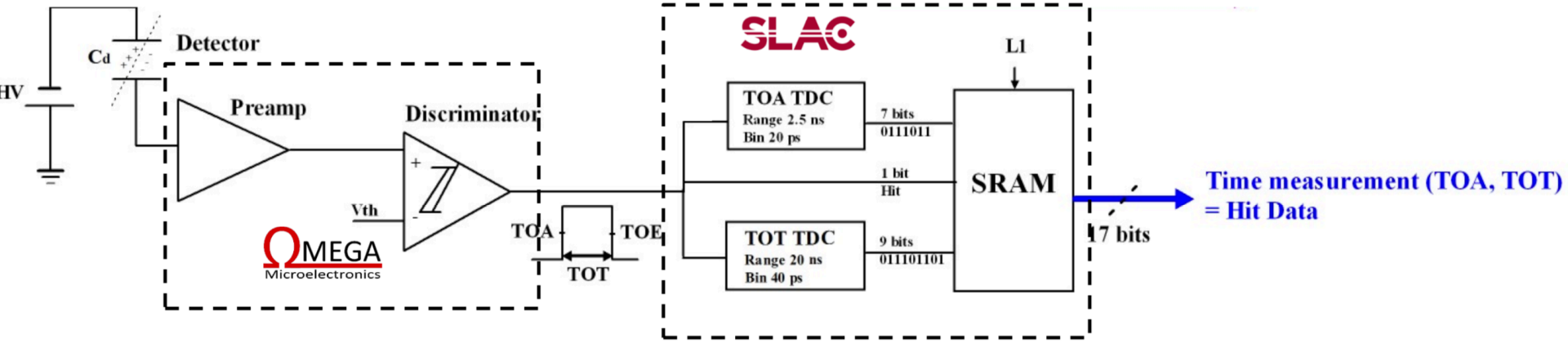




To be presented in NSS-MIC 2019

Institute of Cosmos Sciences

Altiroc1 - 25 ps time resolution ASIC for ATLAS HGTD



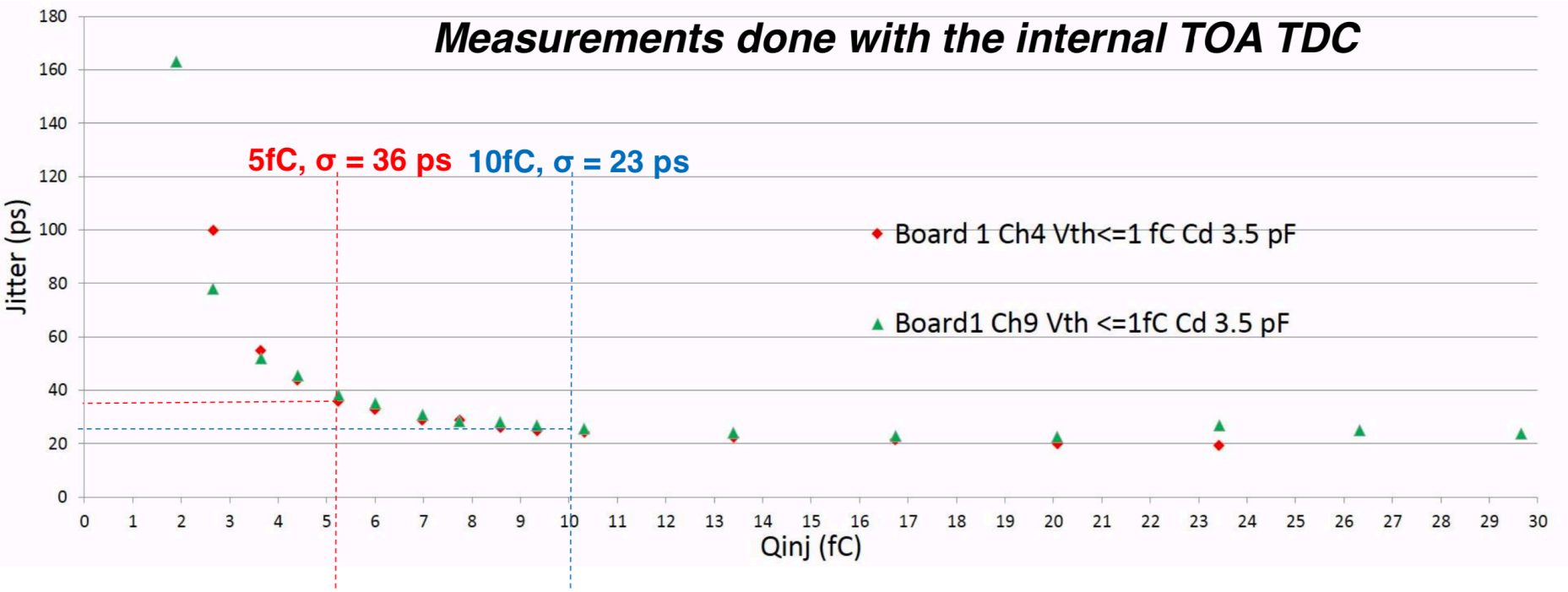
ALTIROC1 FE integrates:

- A **preamplifier** followed by a **discriminator**: Time walk correction made with a Time over Threshold (TOT) architecture
- **Two TDC** (Time to Digital Converter) to provide digital **Hit data** =Time of Arrival (TOA) + Time Over Threshold (TOT) measurement
  - ✓ TOA: range of 2.5 ns and a bin of 20 ps (7 bits)
  - ✓ TOT: range of 20 ns and a bin of 40 ps (9 bits)
- One Local memory (**SRAM**): to store the 17 bits of the time measurement (Hit data) until L0/L1 trigger (~ 1 MHz) => trigger latency = 35 μs

Altiroc1 integrates a standalone phase shifter designed by SMU

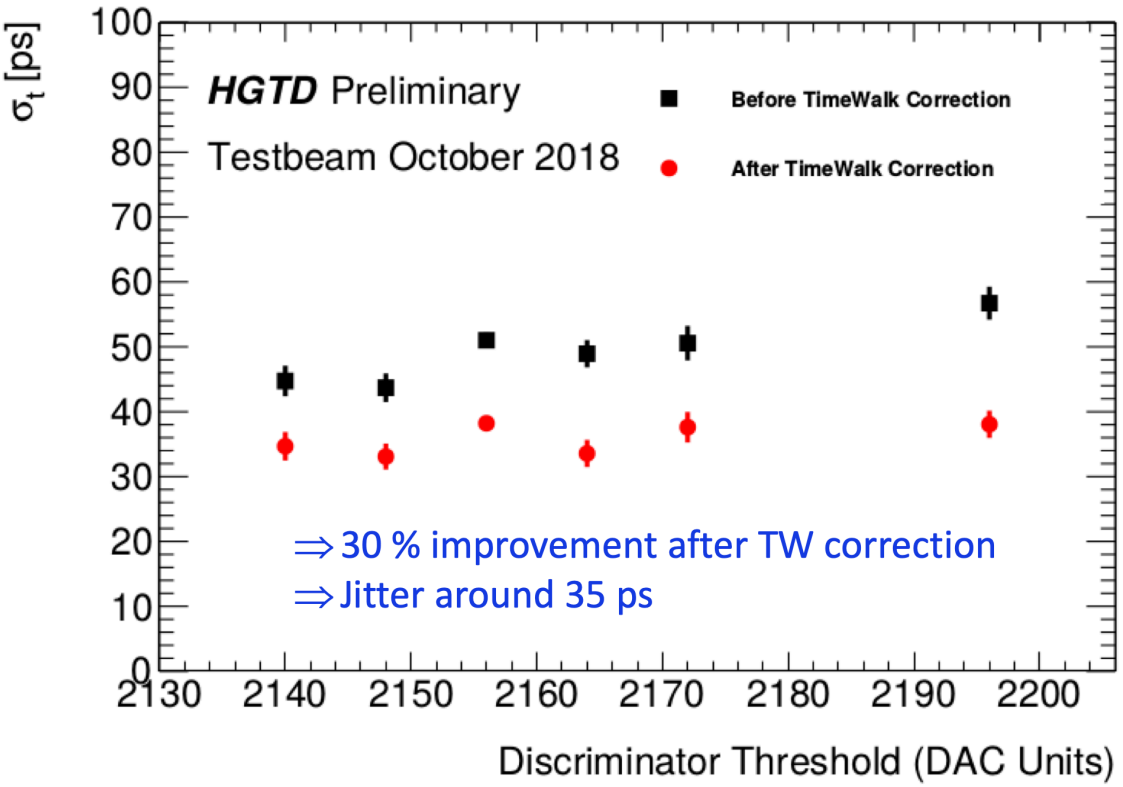
SMU

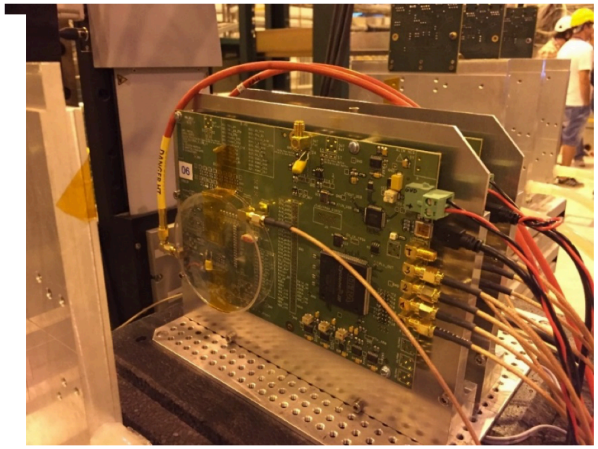
Altiroc1 – Jitter measurement



Altiroc0_v2 - Testbeam (2018)

- Time resolution of a 2x2 x1x1 mm2 LGAD array bump bonded on an Altiroc0 ASIC as a function of the discri threshold (DAC Units) before (black points) and after TW correction (red points)





Time reference given by SiPM with a resolution = 40 ps , which has been substracted

Conclusion

- Whatever FEE is used (SCA WS or single point read-out), microelectronics is now the mainstream choice for large system design
- Strong push for high speed front-end > GHz
  - Essential for timing measurements
  - Several configurations to get GBW > 10 GHz
  - Optimum use of SiGe bipolar transistors
- Voltage sensitive front-end
  - Easiest : 50Ω termination, many commercial amplifiers (mini circuit…)
  - Beware of power dissipation
- Current sensitive front-end
  - Potentially lower noise, lower input impedance
  - Largest GBW product
- In all cases, importance of reducing stray inductance
- Deep submicronic technology will allow disruptive results from FEE for both power and timing

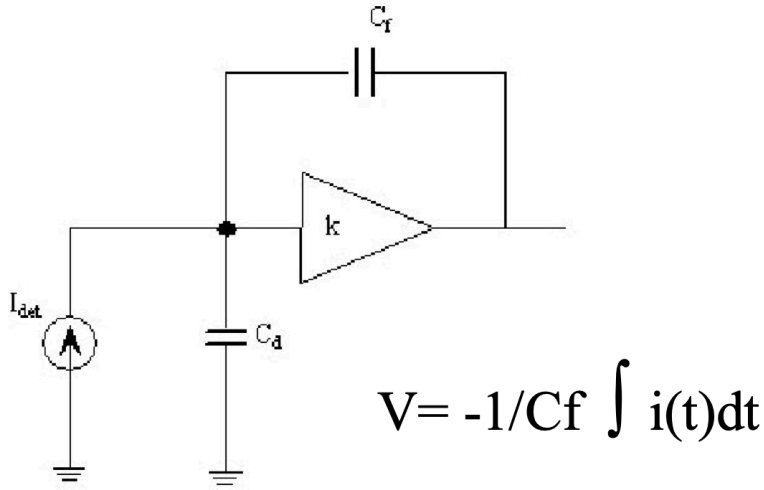
References and thank you

- Christophe de La Taille & Nathalie Seguin-Moreau : review talk on electronics, Si Pin & LGAD readout
- Gary Varner, Stefan Ritt & Eric Delagnes : SCA & weveform electronics
- Wei Shen, Davide Gascon, Joao Varela, Stefan Gundacker : SiPM readout
- General thank you to all people from labs and companies who provided me all the required material to prepare that talk/ I wanted to thank them all nominatively but it doesn't fit on the page.

Thank you

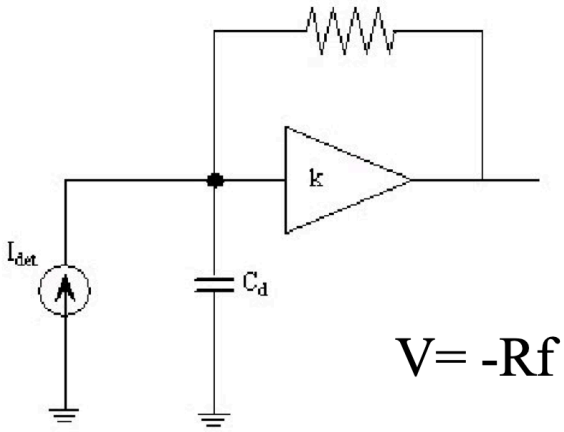
Readout configuration

- Charge preamp
- Capacitive feedback Cf
- Vout/Iin = - 1/jωCf
- Perfect integrator : vout=-Q/Cf∫
- Difficult to accomodate large SiPM signals (200 pC)
- Lowest noise configuration
- Need Rf to empty Cf



$$V = -1/Cf \int i(t)dt$$

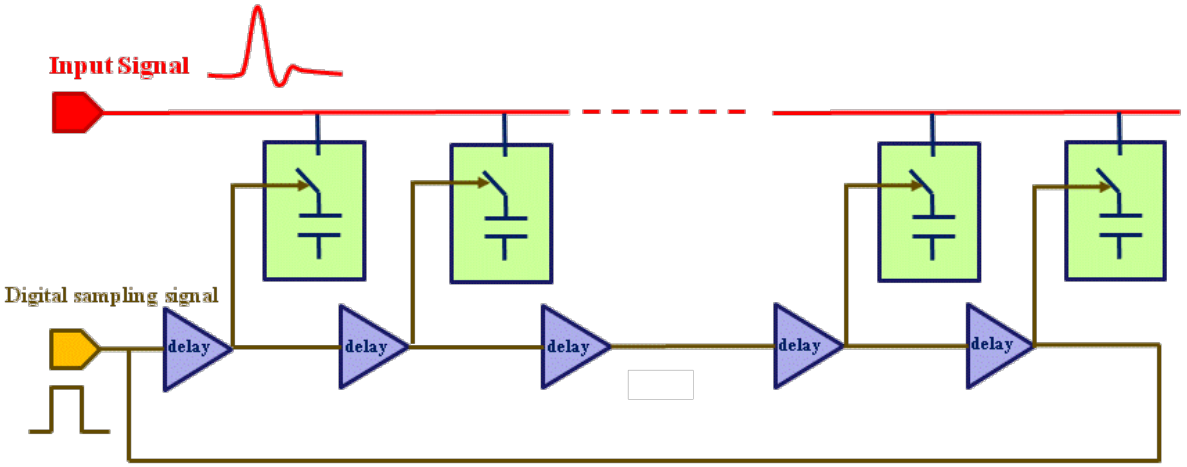
- Current preamp
- Resistive feedback Rf
- Vout/Iin = - Rf
- Keeps signal shape
- Need Cf for stability



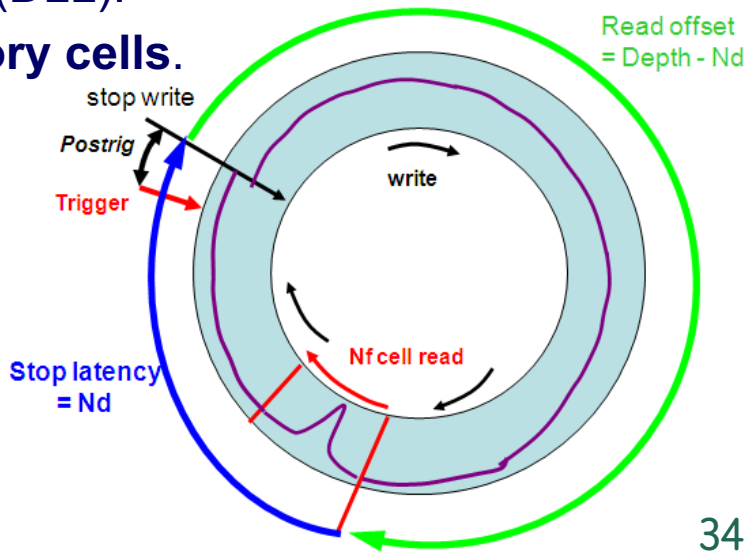
$$V = -Rf\ i(t)$$

Circular analog memories: basic principles

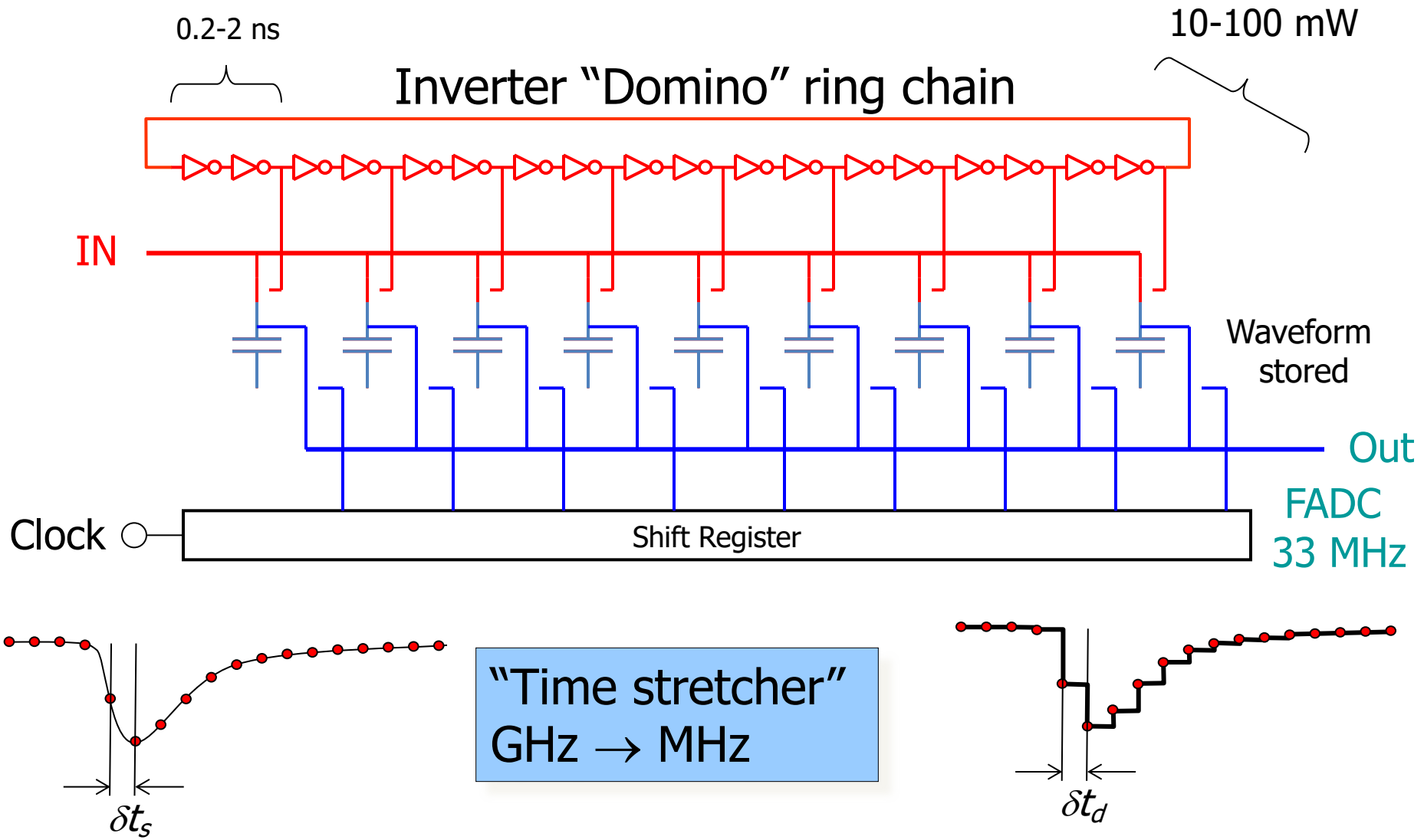
An analog memory can record waveforms at very high sampling rate (>>GS/s)
After trigger, they are digitized at a much lower rate with an ADC (~20 MHz)



- A write pulse is running along a folded **delay line** (DLL).
- It drives the recording of signal into **analog memory cells**.
- Sampling stops upon **trigger**.
- **Readout** can target an area of interest, which can be only a **subset** of the whole channel
- **Dead time** due to readout has to remain as small as possible **(<100ns / sample)**.

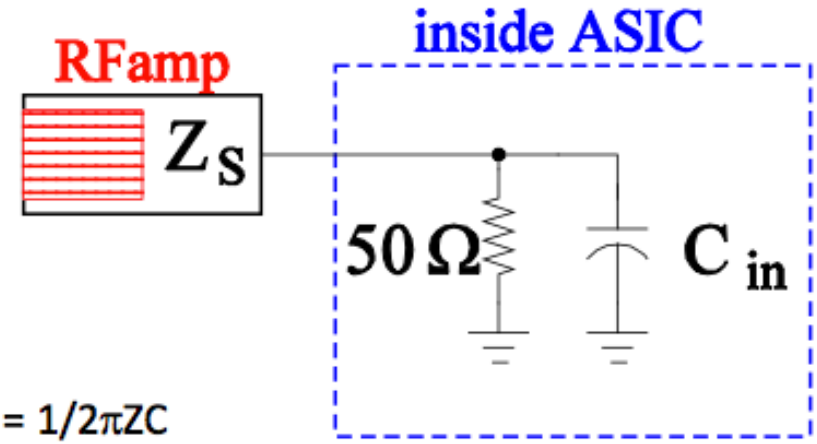


Switched Capacitor Array (Analog Memory)

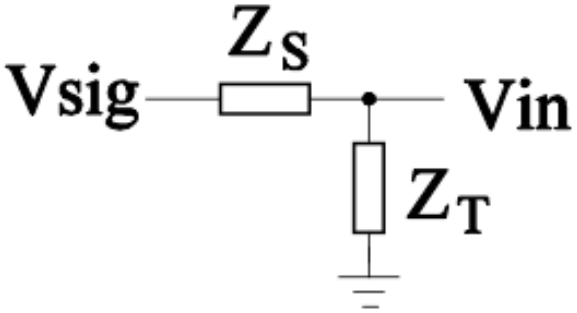


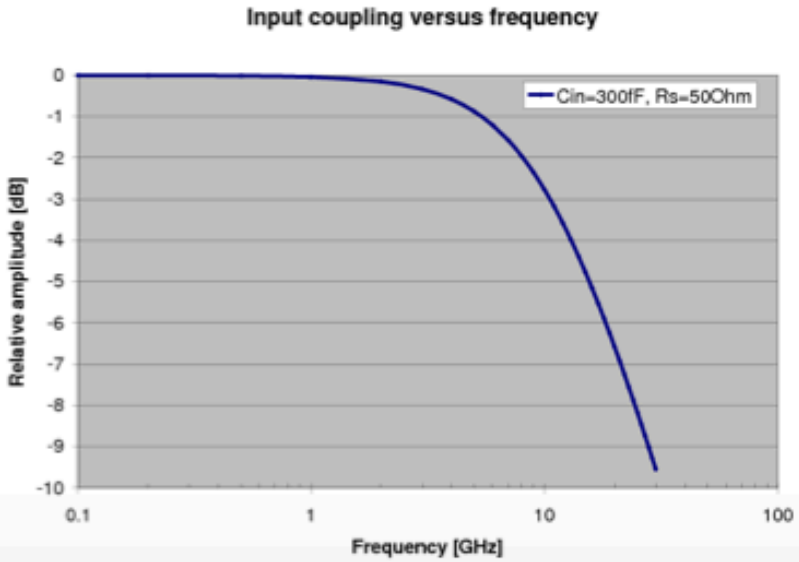
Design constraint 1

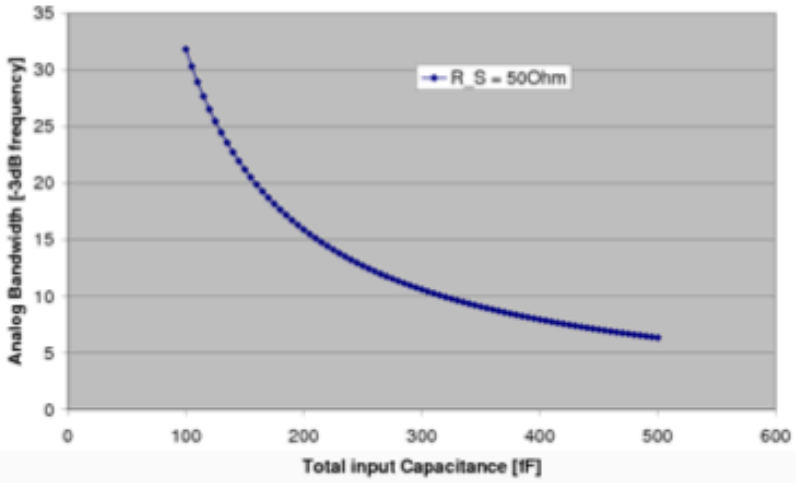
Difficult to couple in Large BW (C is deadly)



$f_{3dB} = 1/2\pi ZC$



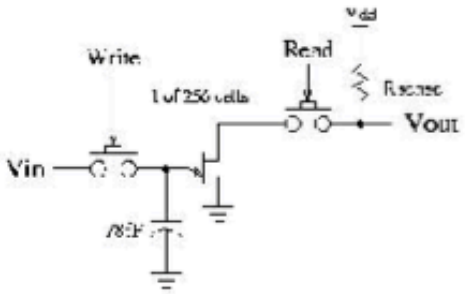




Courtesy : Gary Varner

Design constraint 2

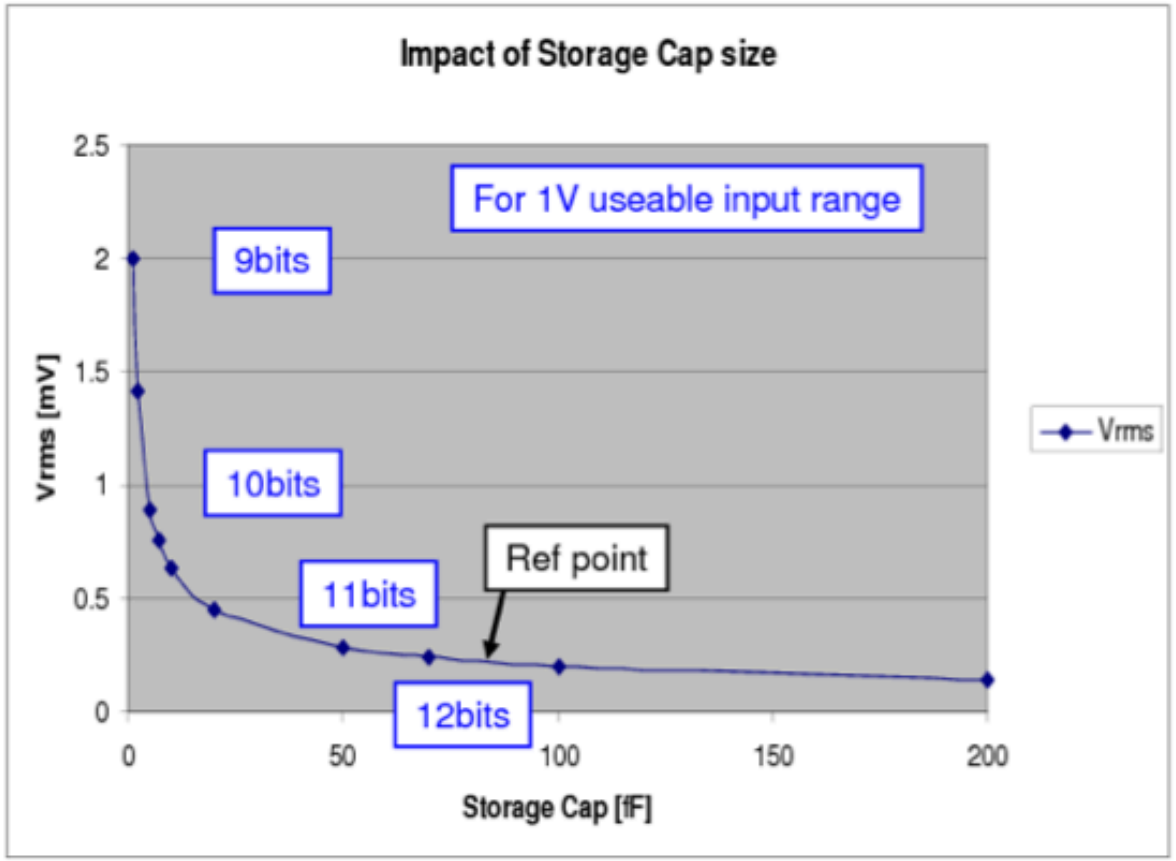
Want small storage C, but…



$$v_{rms} = \sqrt{\frac{kT}{C_{store}}} = 0.23mV$$

C_{store} = 78fF

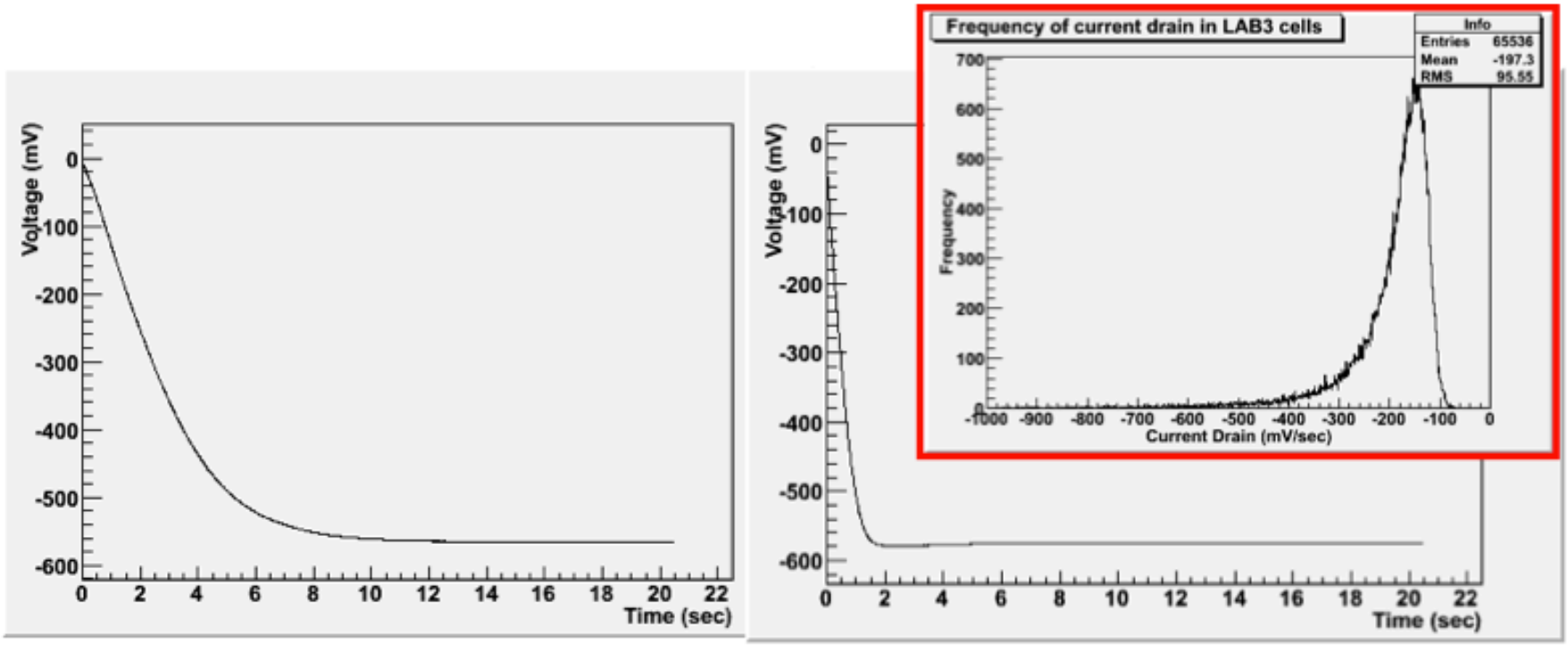
1mV on 16fF is only 100e- !



Courtesy : Gary Varner

Design constraint 3

Increase C or reduce conversion time << 1mV



Sample channel-channel variation

~ fA → nA leakage (250nm → 130nm)

Courtesy : Gary Varner

NINO

Chip designed by CERN group for ALICE TOF RPCs

[F. Anghinolfi, P. Jarron et al. NINO: an ultra-fast and low-power front-end amplifier/discriminator ASIC designed for the multigap resistive plate chamber, NIM A, 2004, Vol. 533 page 183-187]

8 channels amplifier and discriminator