Top Tracker electronics status

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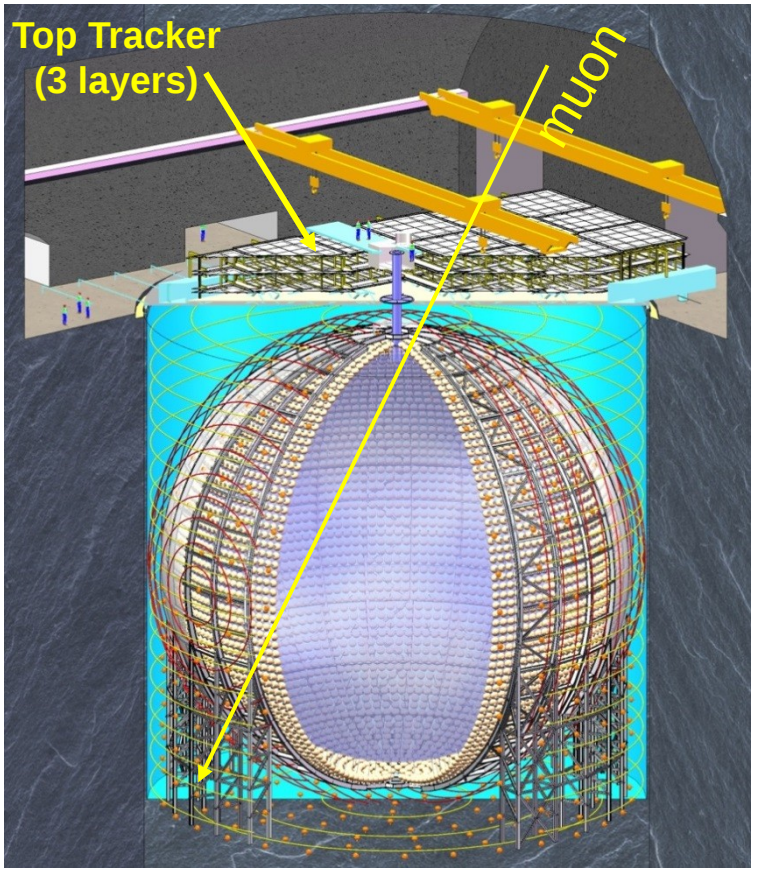
INFN – LNF

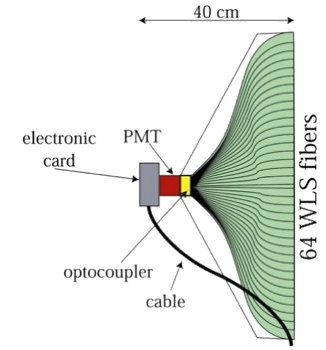
JUNO Italian groups meeting
Ferrara
9-10 May 2019

JUNO Top Tracker

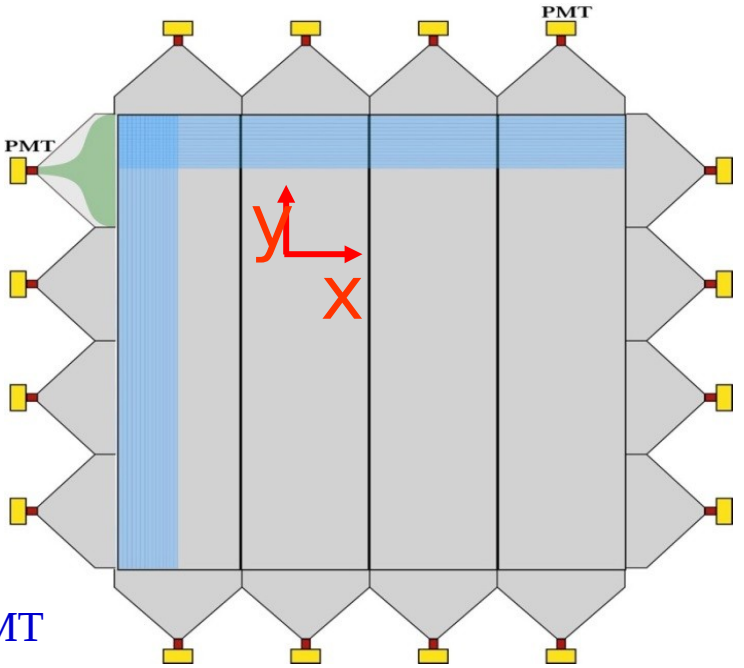


Needed to:

- Studies on cosmogenic background.
- Monitor Central Detector and Water Cerenkov efficiency and tracking performances on cosmic rays.



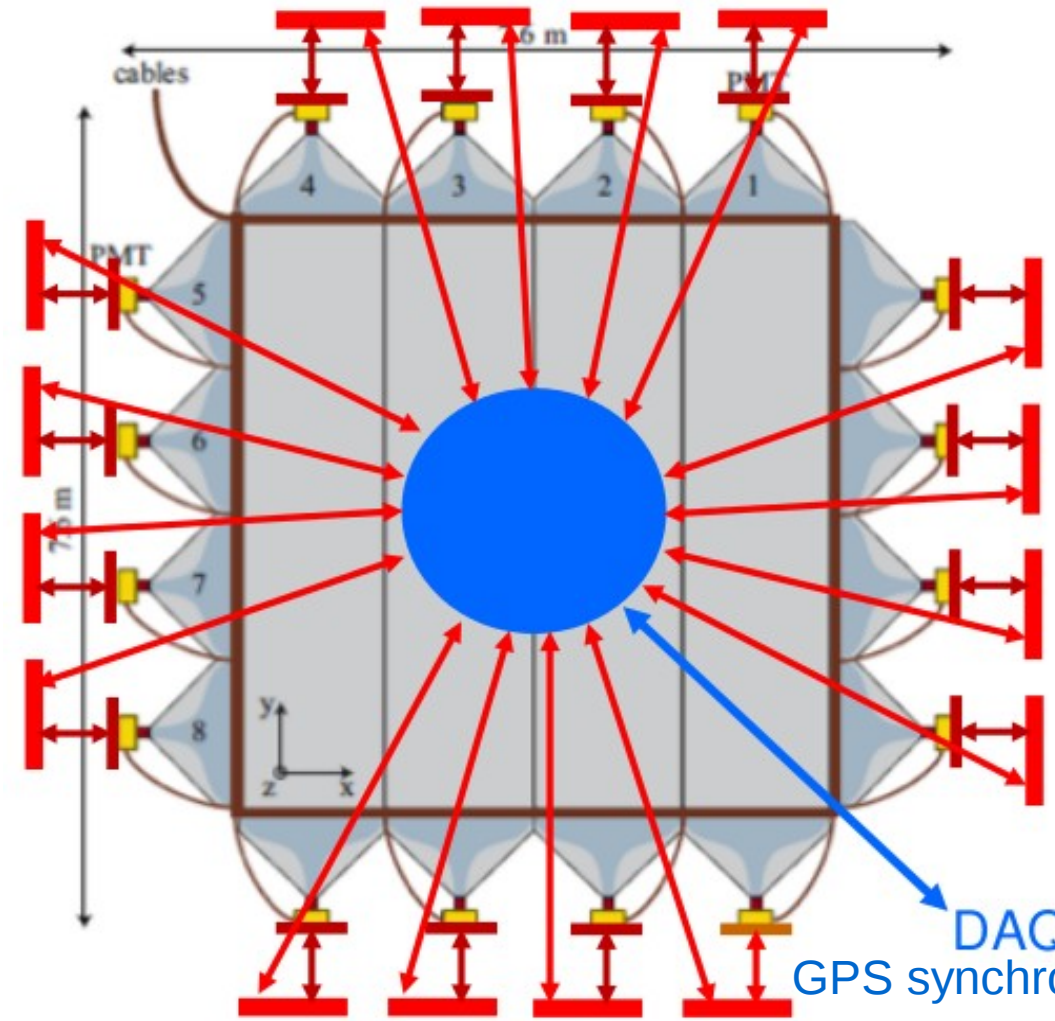
Hamamatsu MA-PMT
(3x3 cm^2)



- 62 walls (496 modules)
- 32 k scintillator strips (2.6 cm)
- 6.8x6.8 m^2 sensitive area/wall
- 64 k channels in total

Top Tracker electronics

Top Tracker modules recovered from OPERA.
Electronics needs to be replaced given the higher environment radioactivity.

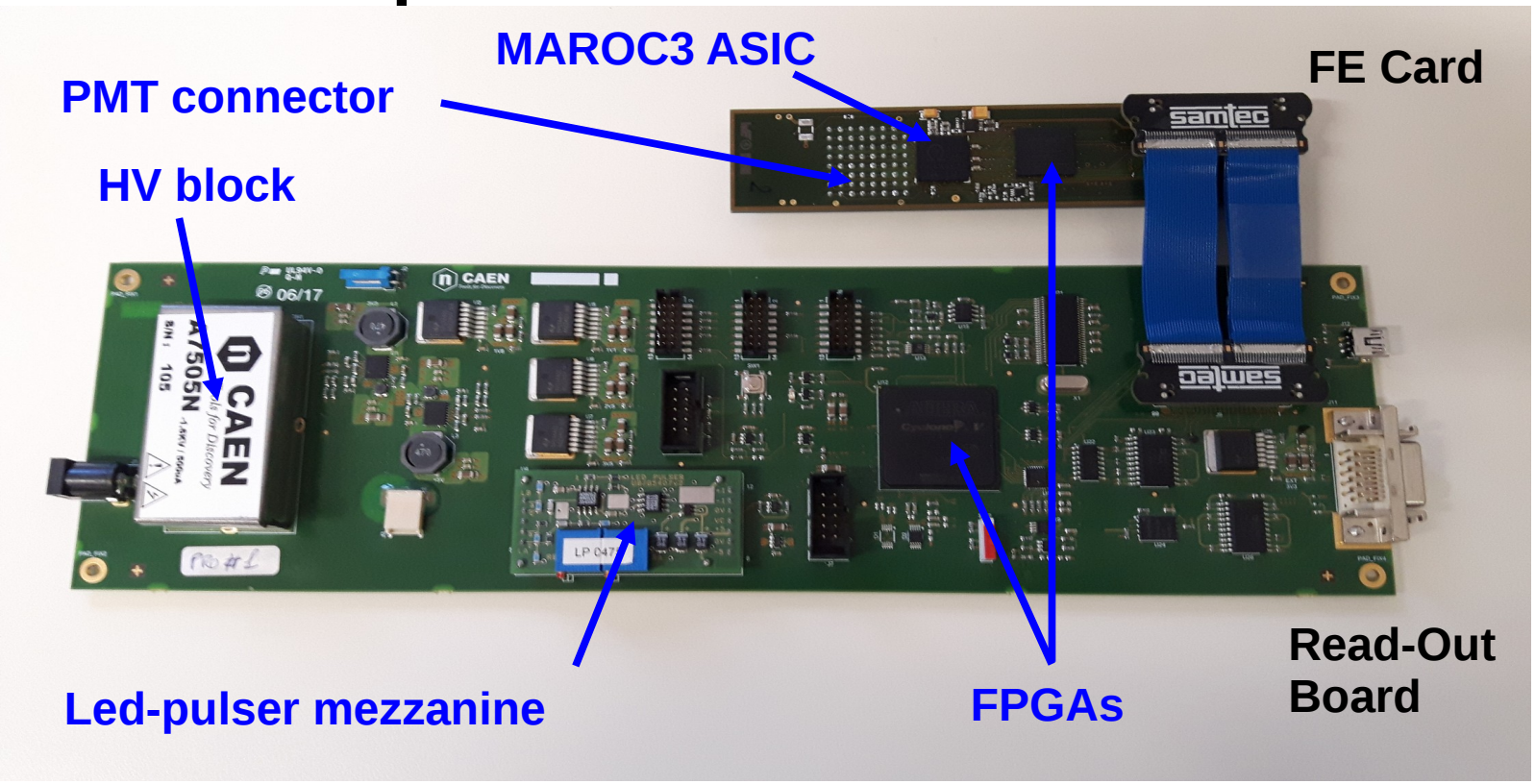


- MAROC3 board (FEC): **Strasbourg**
  It hosts MAROC3 chip and logic strictly required to make it work.

- Read-out board: **Frascati-CAEN**
  Manages MAROC3 setting and read-out.
  Hosts PMT HV power supply.
  Hosts FADC for charge read-out.
  Sends to Concentrator PMT OR.

- CONCENTRATOR board:
  Generates wall trigger. **Strasbourg**
  Trigger time-stamp with respect to GPS signal.
  Measures time difference between PMT Ors and trigger.
  Collect read-out board data and send them to DAQ.
  Deliver DCS commands to read-out boards.

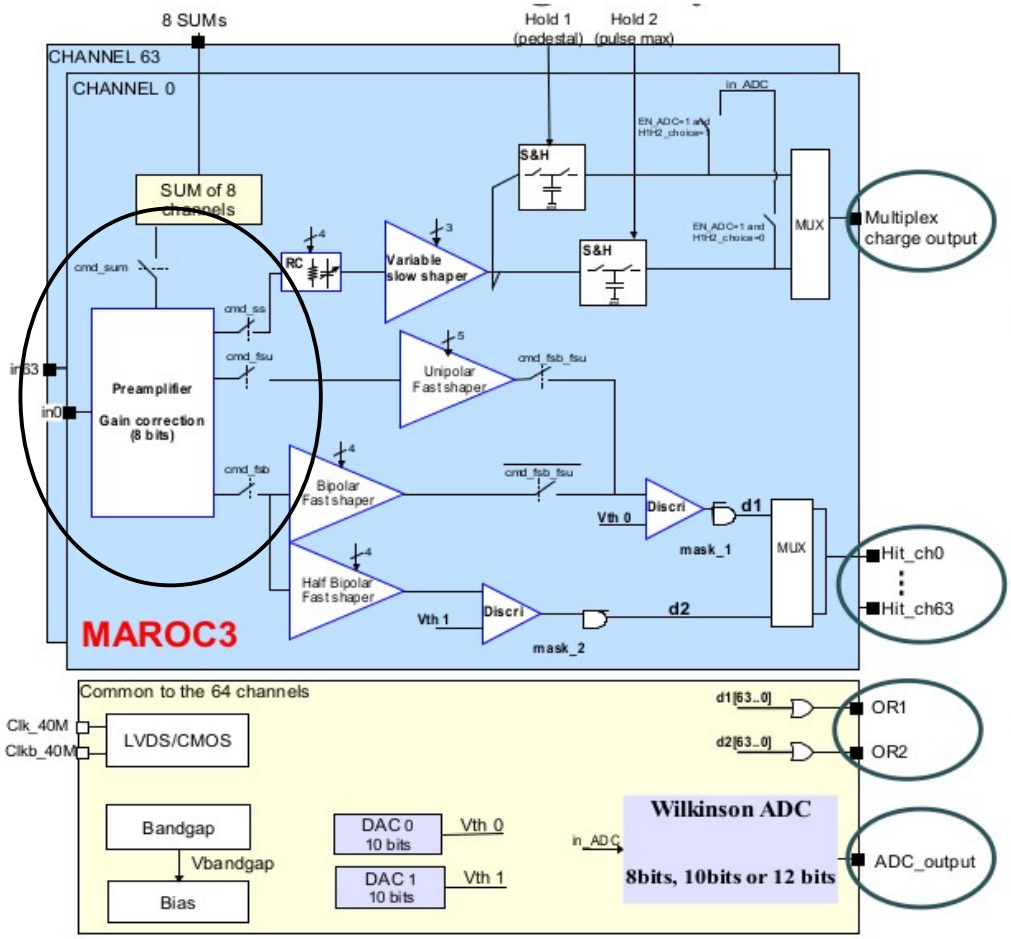
Top Tracker electronics status



FE Card and RO Board design frozen.
FEC + ROB read-out chain extensively tested, also on detector prototype.
First CONCENTRATOR prototypes ready.
Link protocol between ROB and CONCENTRATOR ready by end of 2019.
First preliminar tests ROB-CONCENTRATOR at the end of JUNE.
ROB mass production start at the beginning of 2020 (order placed).
DAQ and DCS ?

MAROC3 chip on FEC

Preamplifier



64 channels

Out_Q : Multiplex charge output

Triggers

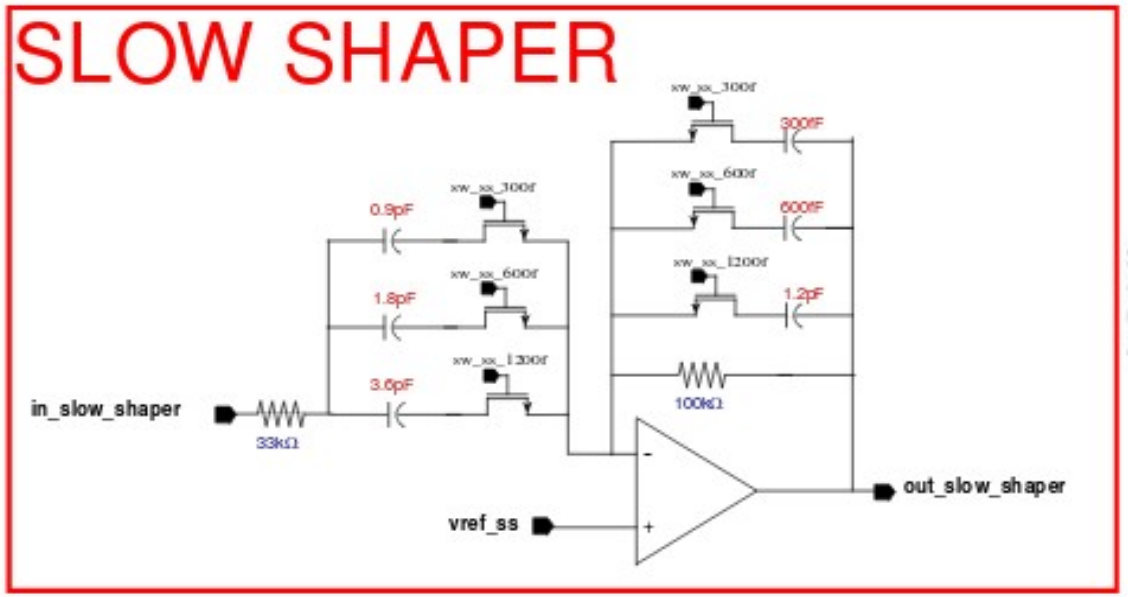
OR of triggers

Out_ADC : Internal ADC output

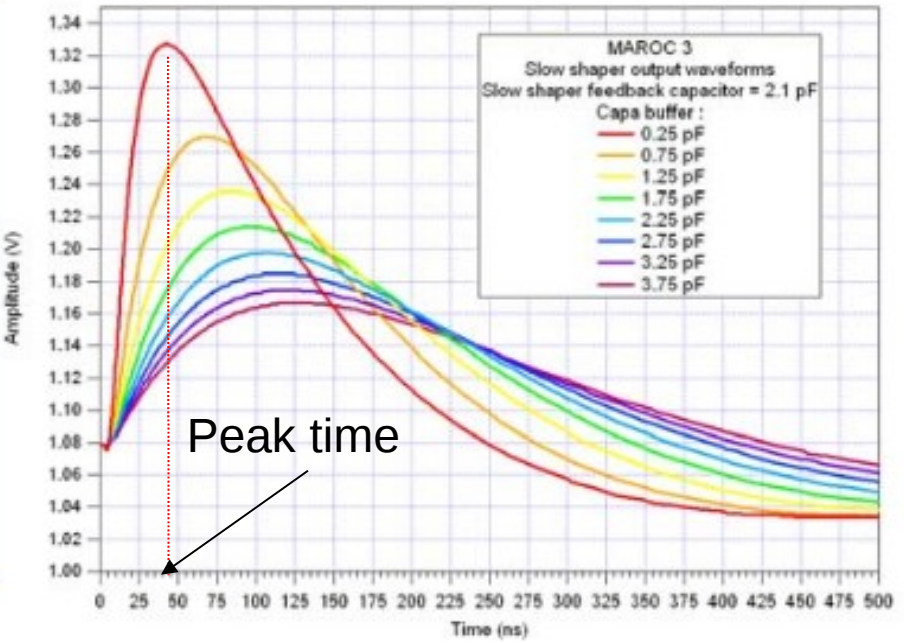
Premaplifier gain: (0-4) range. Set to 1 in present tests. In JUNO apparatus, equalization according to calibration runs.
Slow shaper parameters for charge read-out chosen according to OPERA experience.
Digital section shaper and peak-time choice according to OPERA experience.

Charge read-out

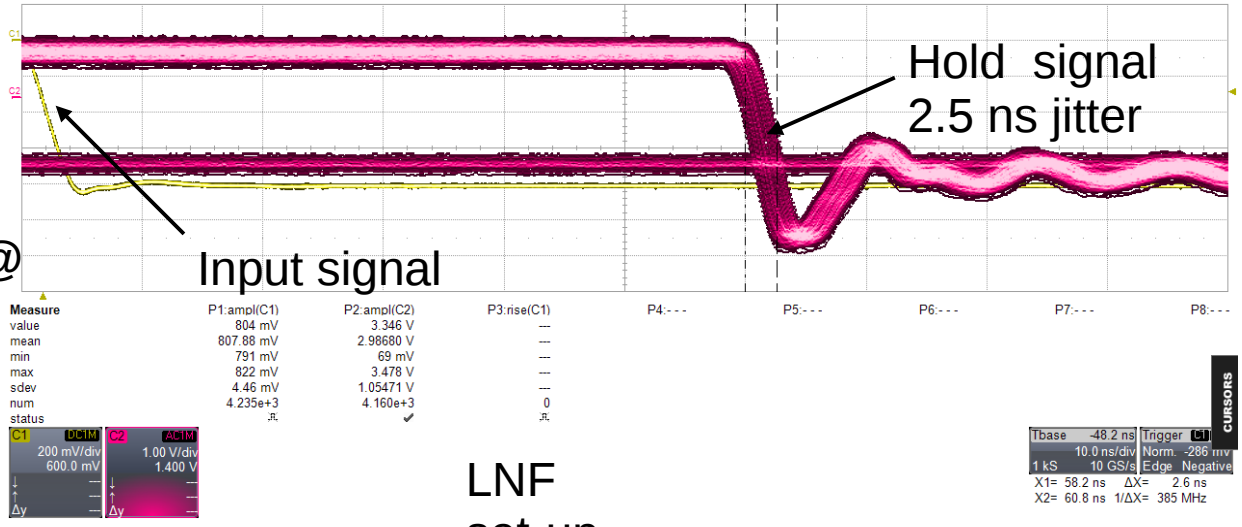
Slow shaper scheme.
Capacitor values adjustale (MAROC3 setting).



Slow shaper output simulation.
From MAROC3 manual.



MAROC3 charge read-out through sample&hold method.
Hold must be issued by ROB at the peak time of slow shaper output, with a small time jitter.
Correct delay and time jitter verified @ Strasbourg.
New firmware version in December: Hold-signal delay is programmable parameter (jitter < 1 ns).



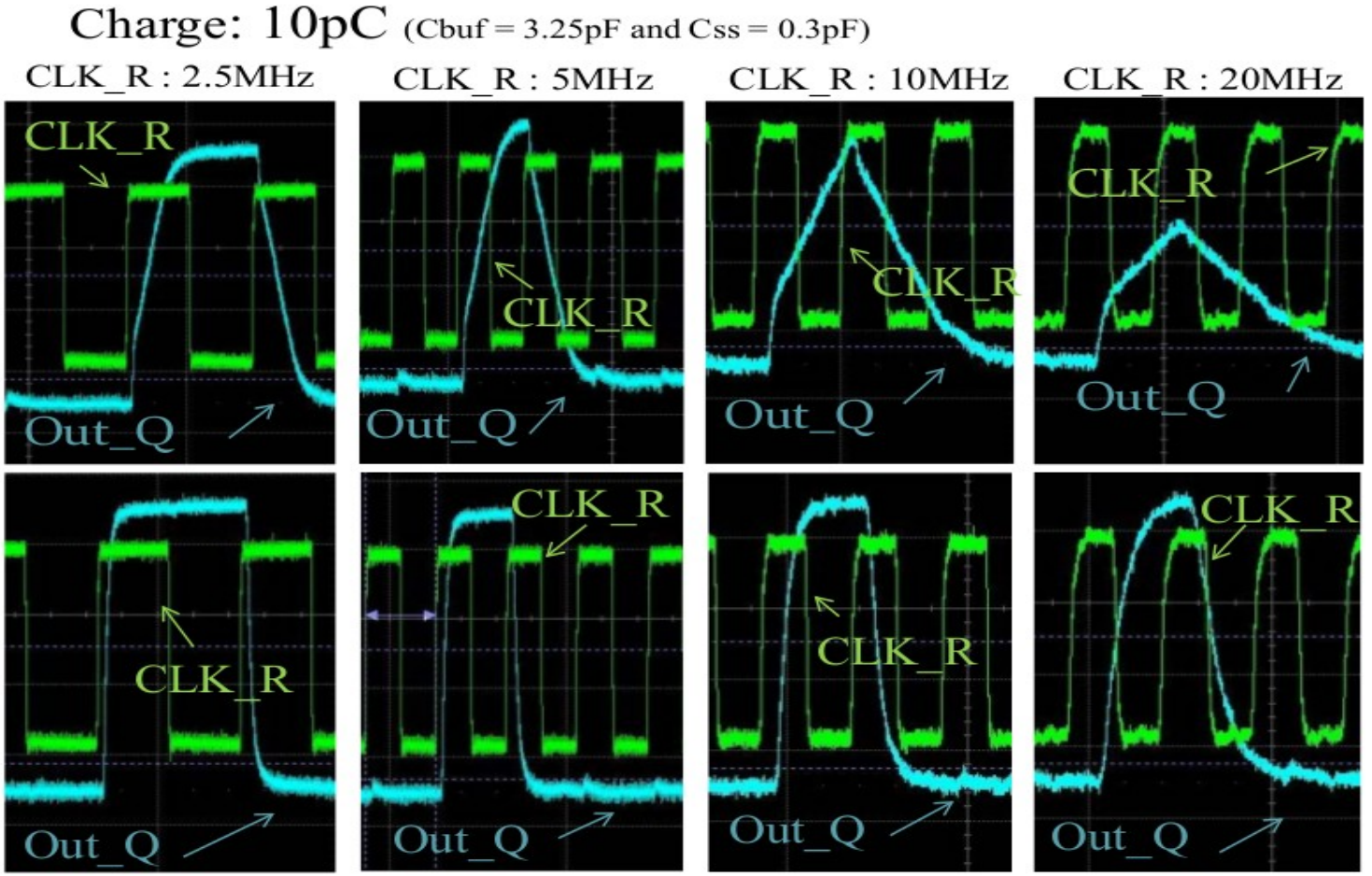
LNF
set-up

Charge read-out

Two possible options, tested with the MAROC3 evaluation board:

Internal conversion (8 bit) with Wilkinson ADC inside MAROC3. Maximum deadtime = 13.7 µs (with 80 MHz clock instead of standard 40 MHz).

External read-out with FADC on RO board. Maximum deadtime = 6.7 µs (with clock_R=10 MHz).

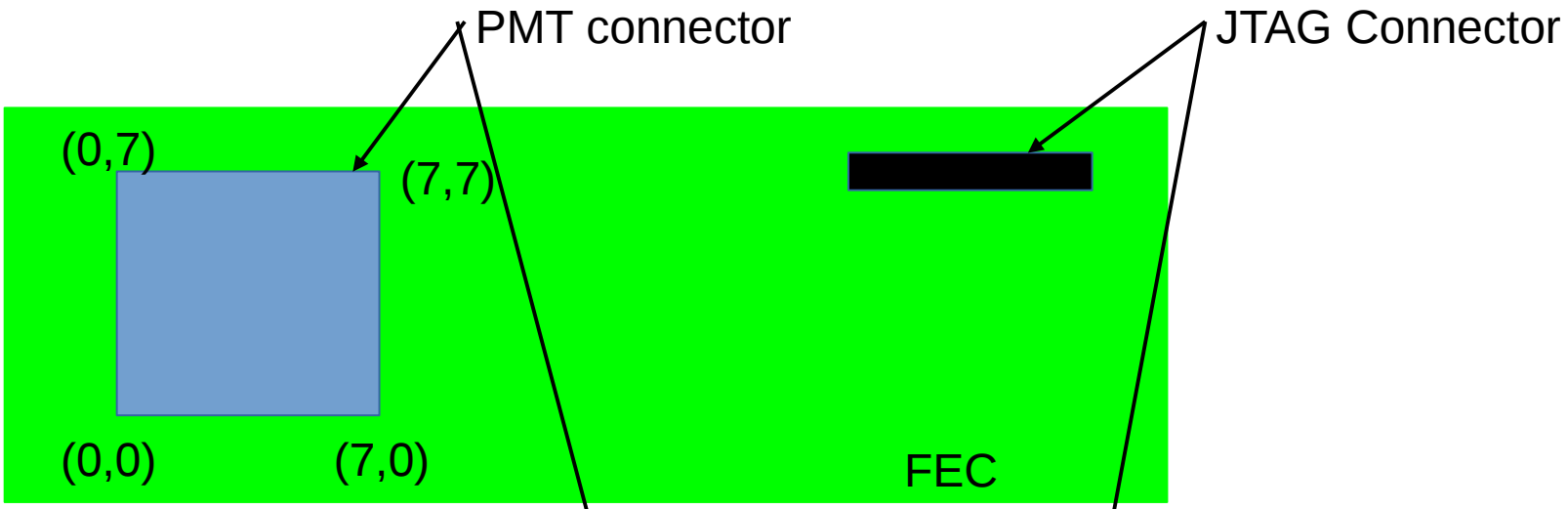


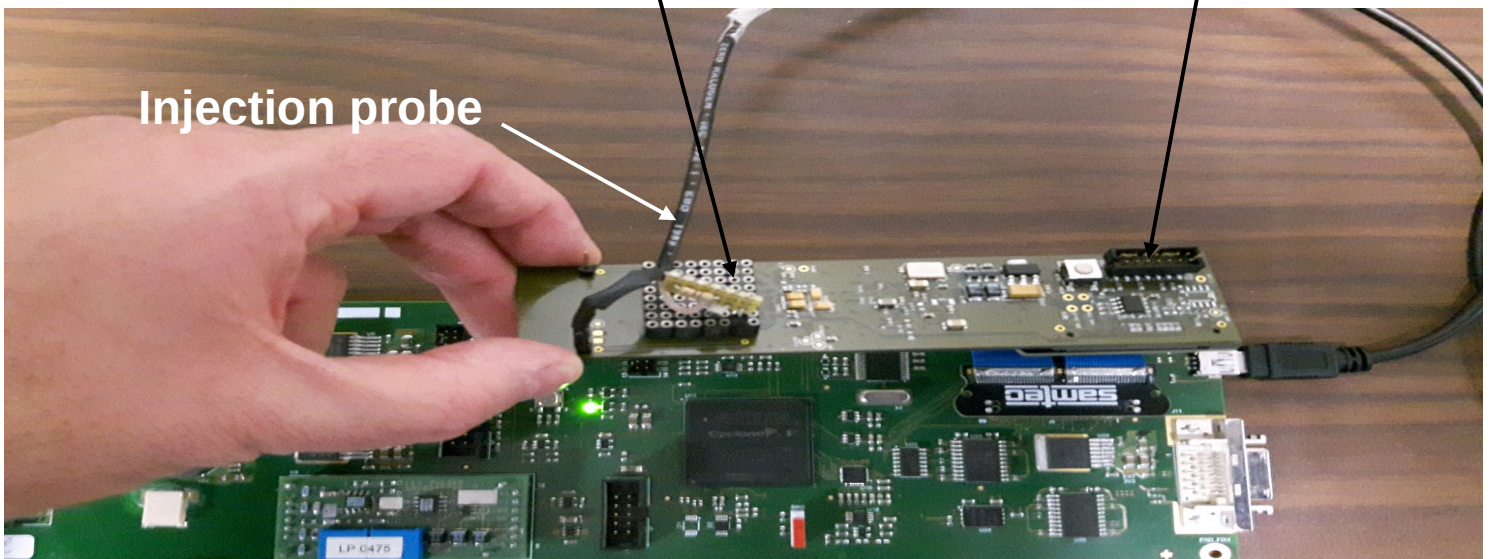
Without resistor on ib_widlar

3.6k resistor on ib_widlar

Test-pulse tests @ LNF

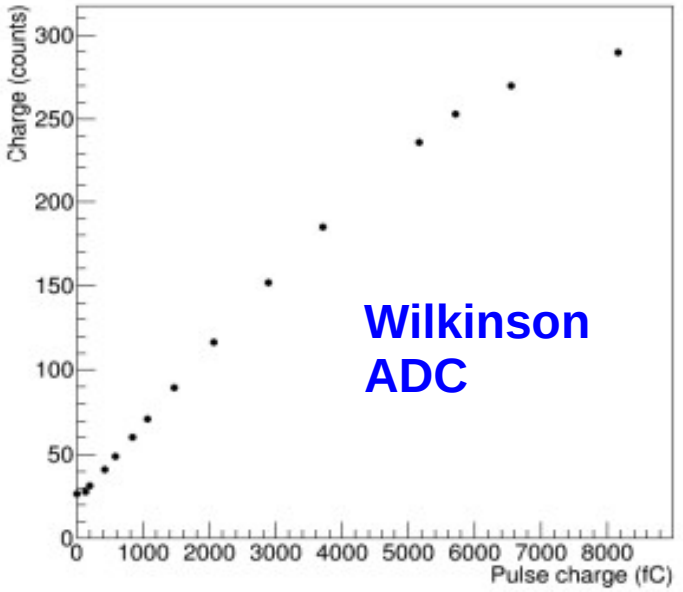
Set-up:
NIM signal + attenuation + derivation with C=10 pF
Q=C*V (V=amplitude of attenuated signal).

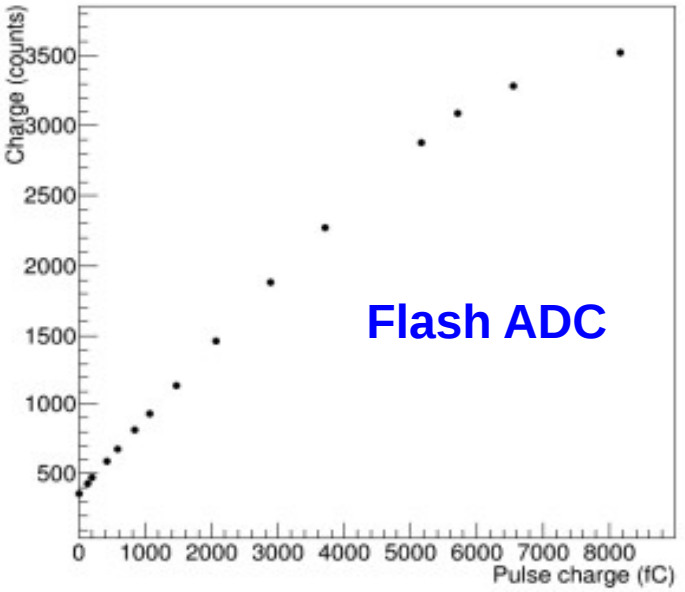




FE+ROB test results (1)

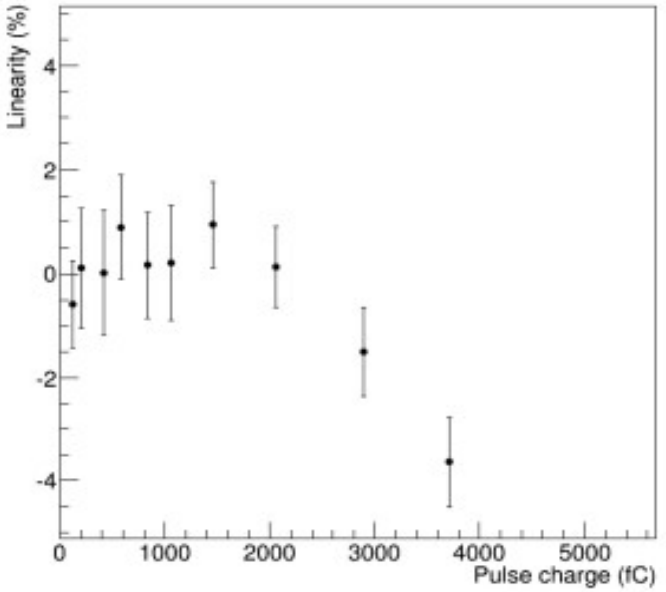
Calibration

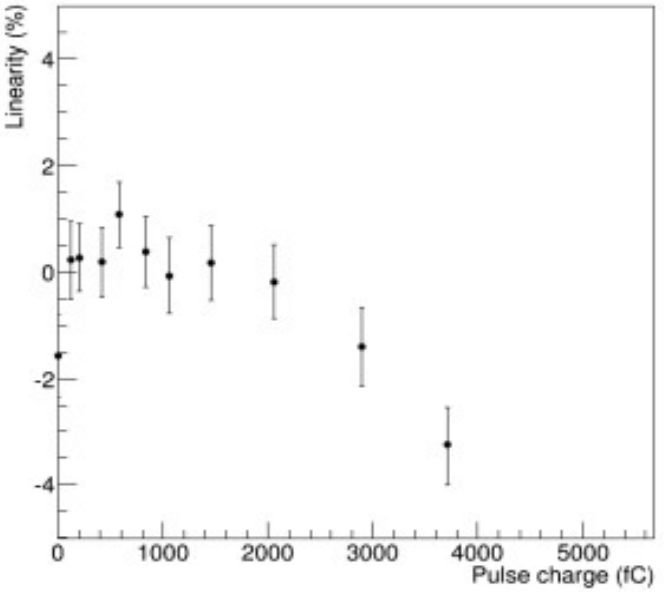




Note: 1 pe=80 fC.
Realistic MIP charges lower than 2 pC.

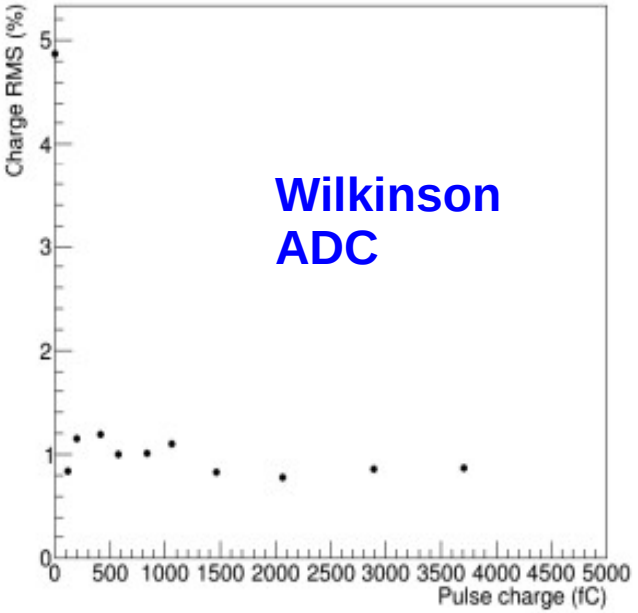
Linearity

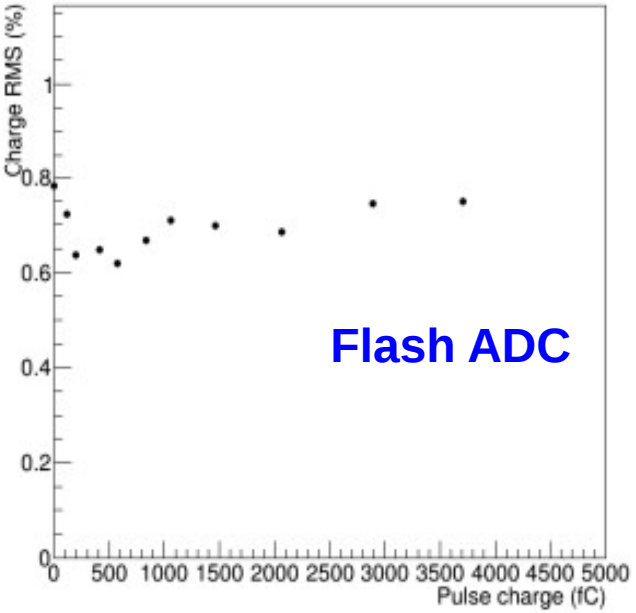




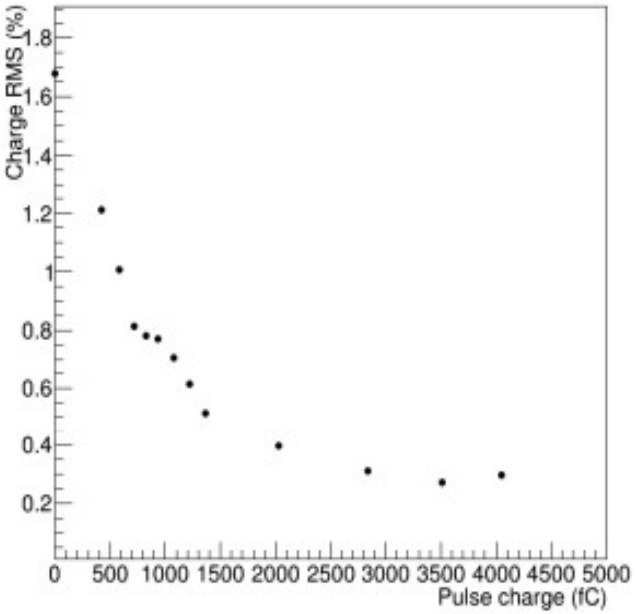
FE+ROB test results (2)

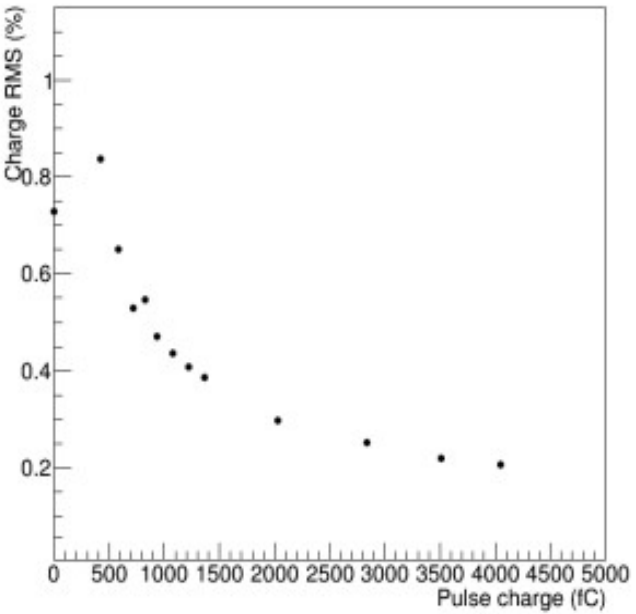
RMS with old firmware version. Hold delay with Internal FPGA circuit





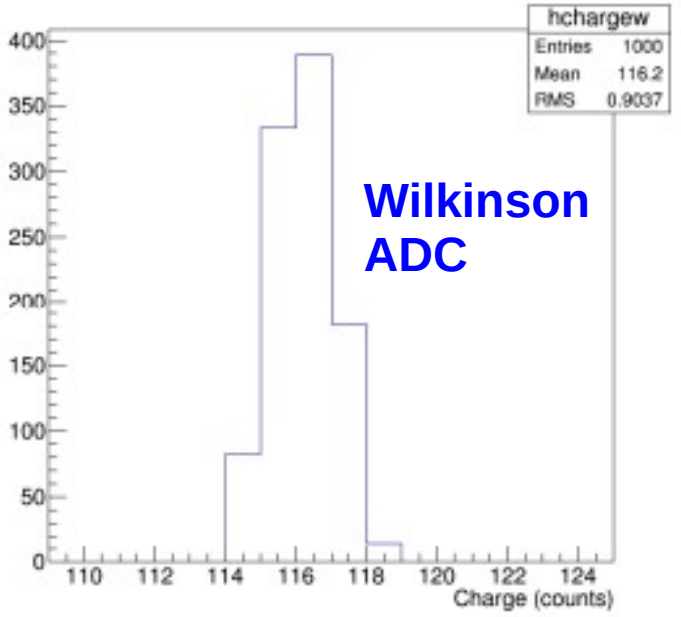
RMS with new firmware version. Hold delay with monostable circuit.



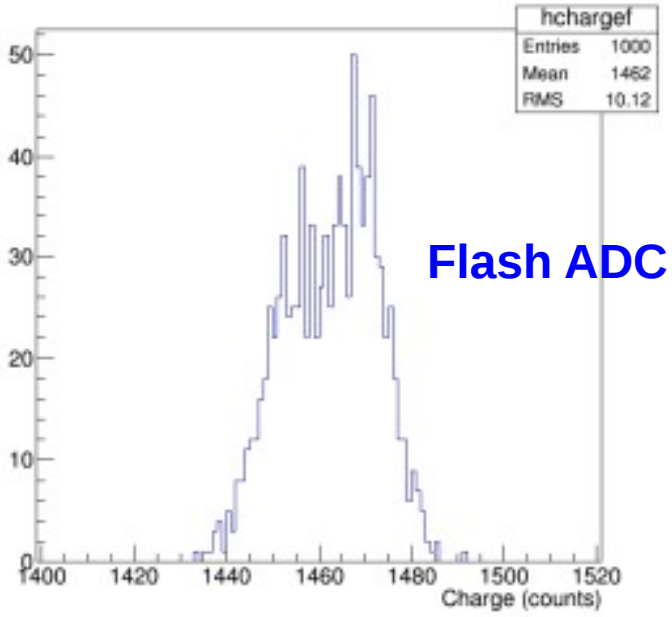


FE+ROB test results (3)

RMS with old firmware version. Hold delay with Internal FPGA circuit

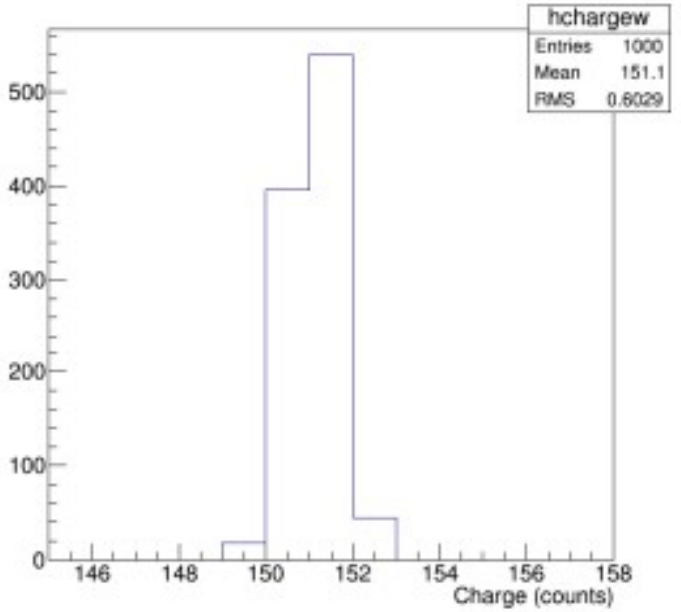


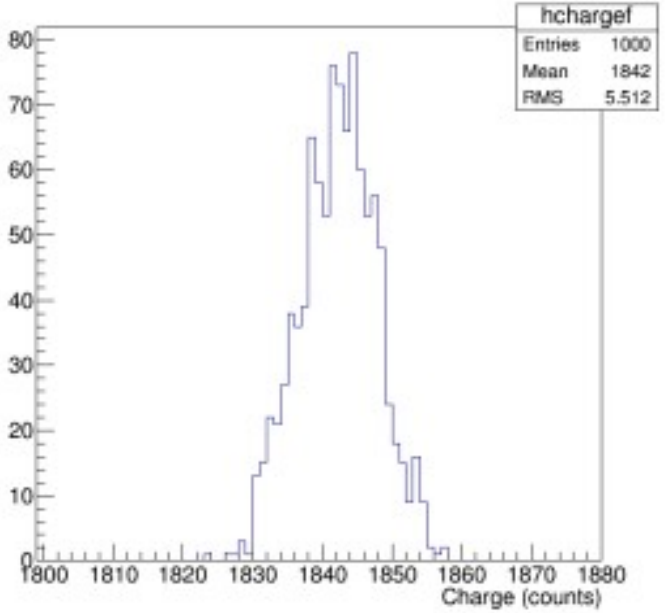
Wilkinson ADC



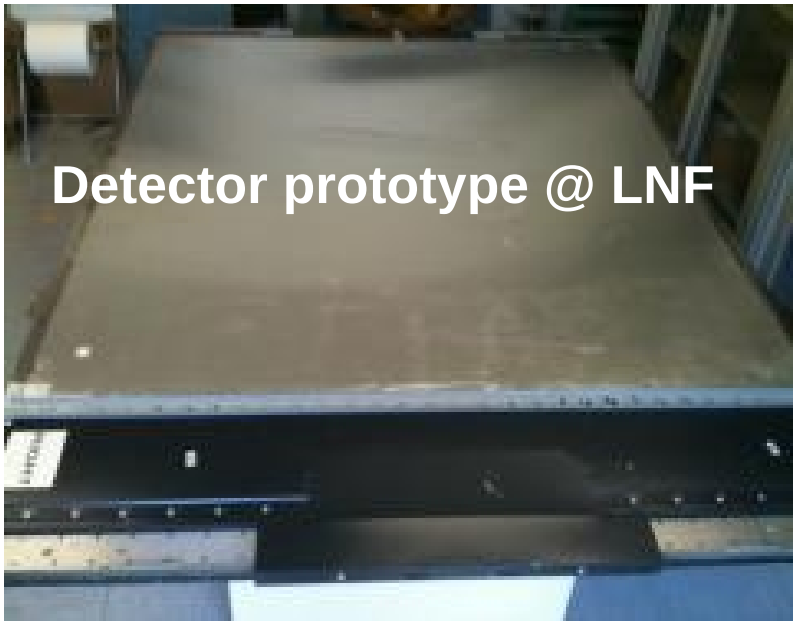
Flash ADC

RMS with new firmware version. Hold delay with monostable circuit.

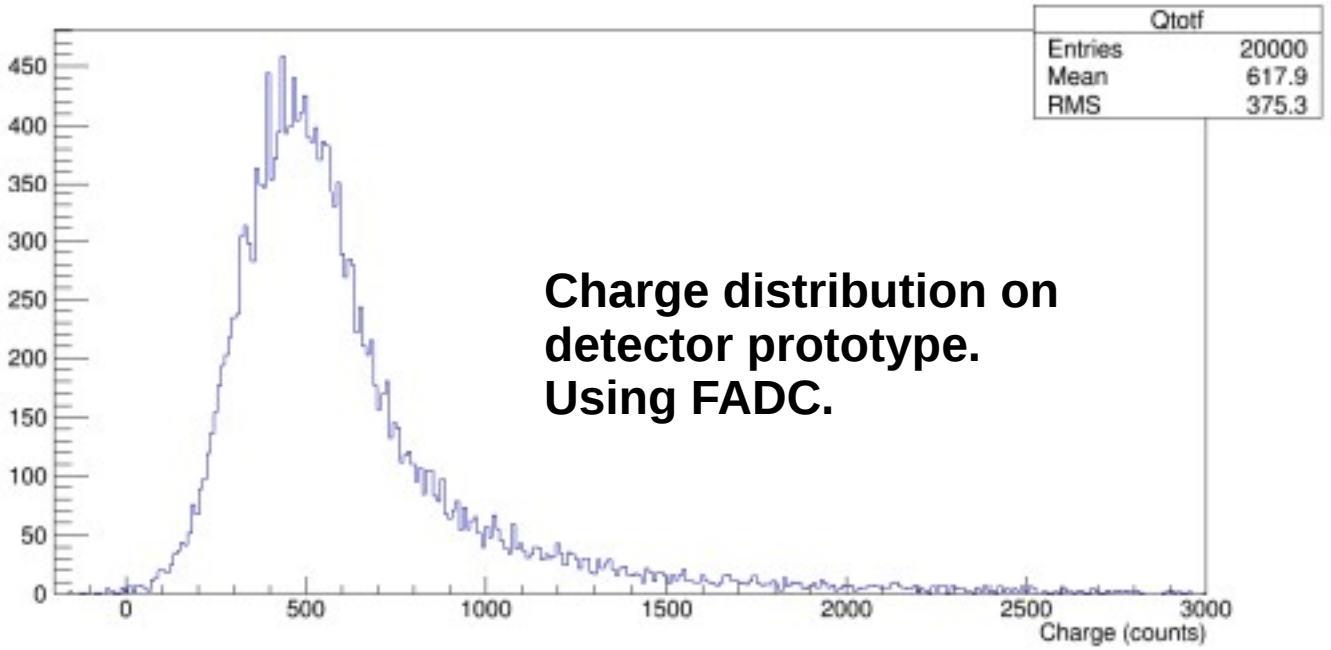




FE+ROB test results (4)



FEC + ROB read-out tested successfully also on a detetor prototype.



Charge distribution on detector prototype. Using FADC.

CAEN A7511N HV block

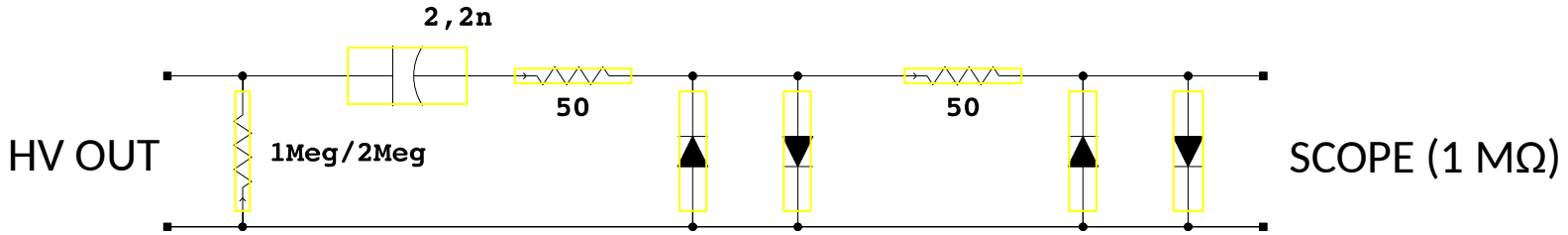
Hvmax=1100 V
Imax=1000 μA
Voltage supply = 12 V(10% tolerance)
Vset input= 0 – 2.6 V
Ripple < 10 mV ptp

Parameters:
Vset = Set Voltage
Iset = Current limitation
Vmon = Measured Voltage
Imon = Measured Current
OVC bit = 1 if Current limitation

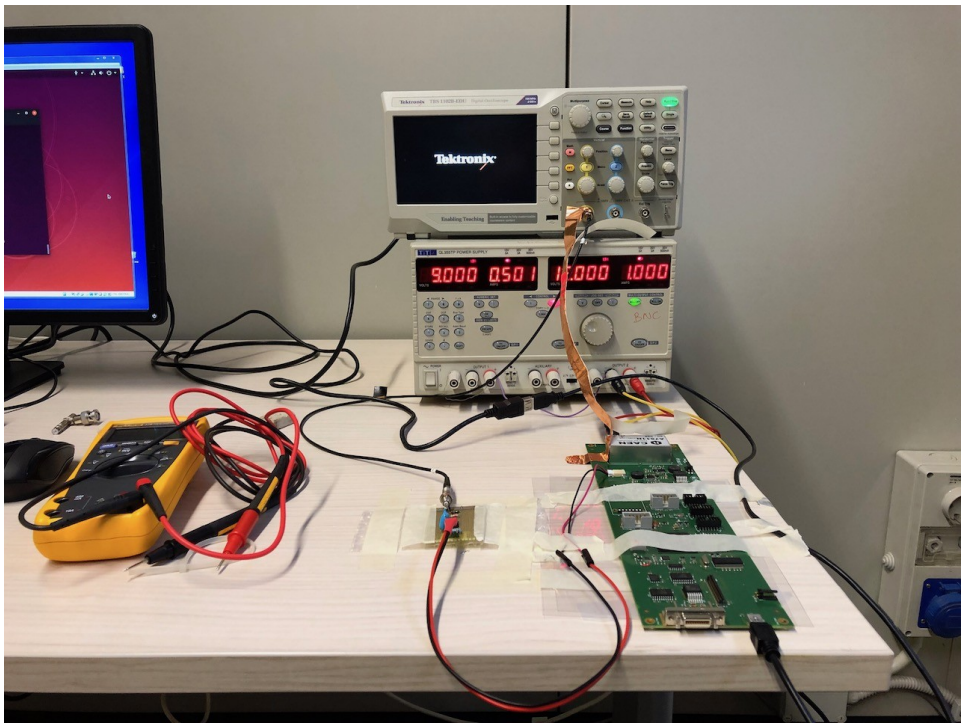
Block developed by CAEN for JUNO TT, pin-to-pin compatible with A7505N.
A7511N now in CAEN catalog.
First prototypes tested at CAEN and at LNF (on ROB):

- **Ripple lower than 10 mVptp.**
- **No visible common mode noise at mV level (Waveform observation on detector).**

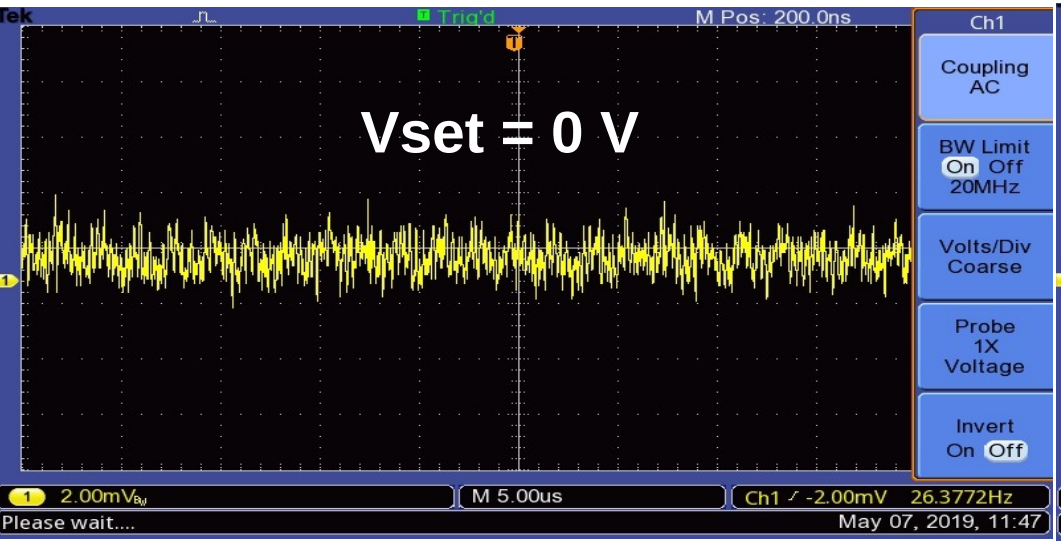
HV ripple measurement set-up

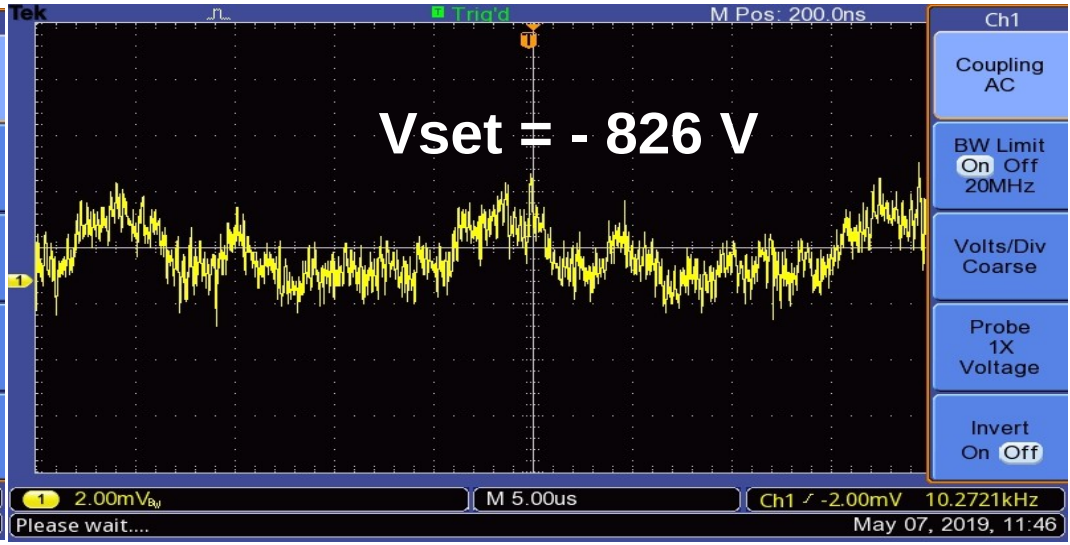


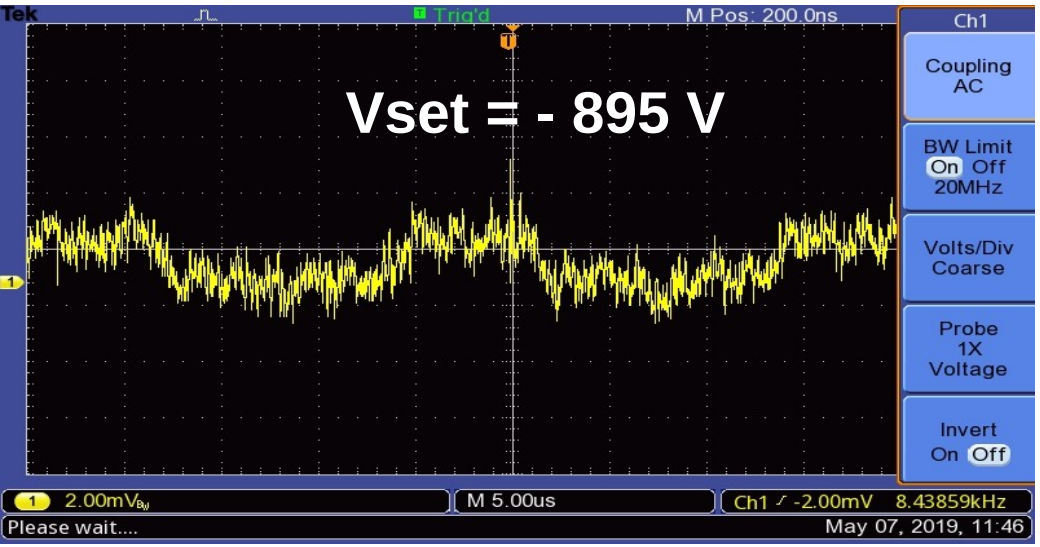
* GND board connected to Oscillosope GND

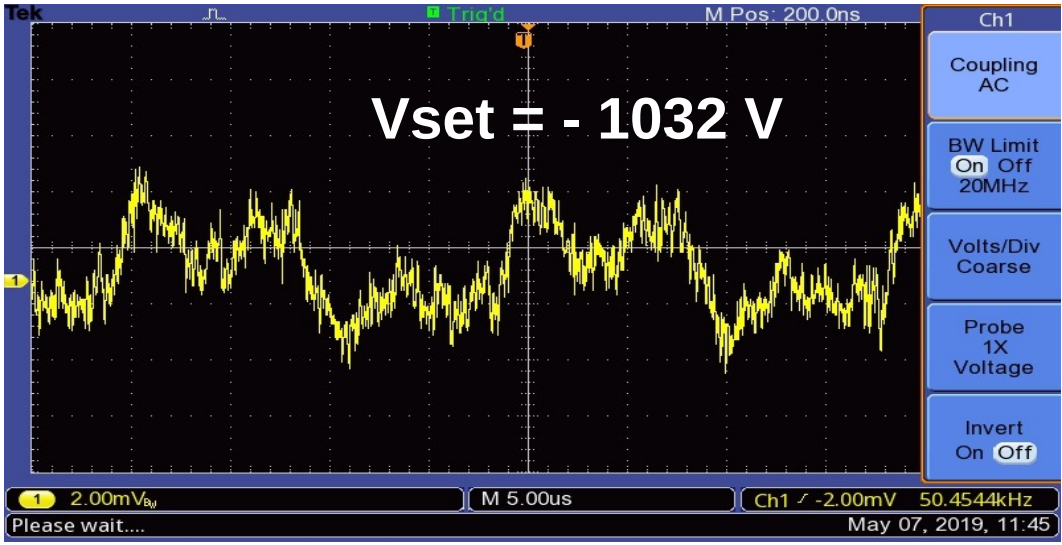


HV ripple measurement (2 MΩ)



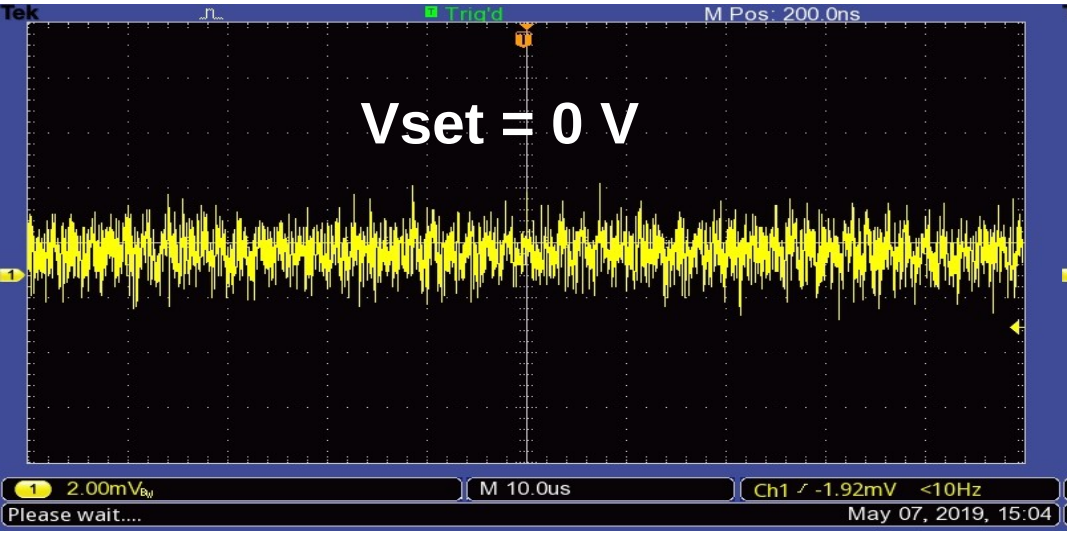


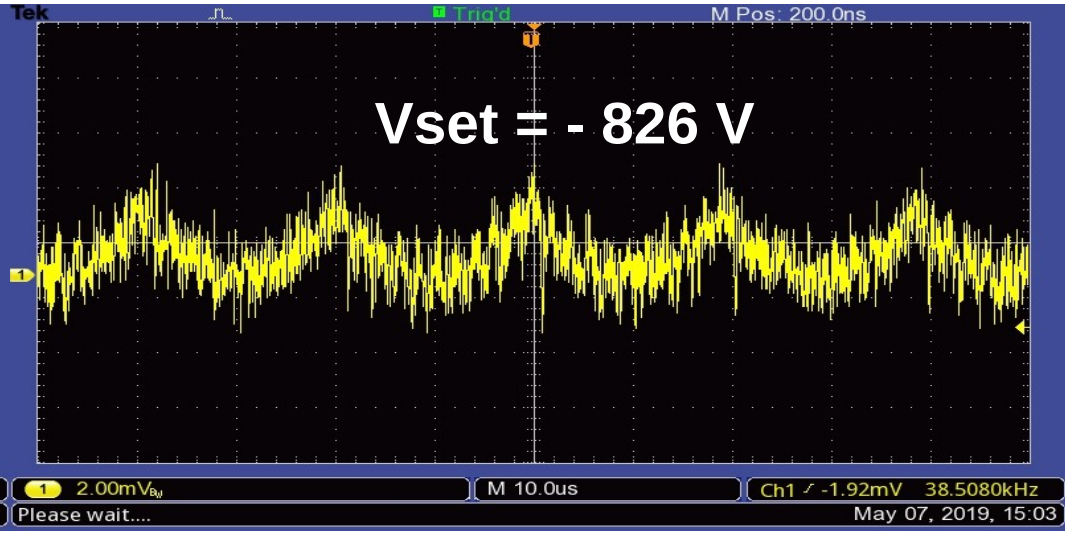


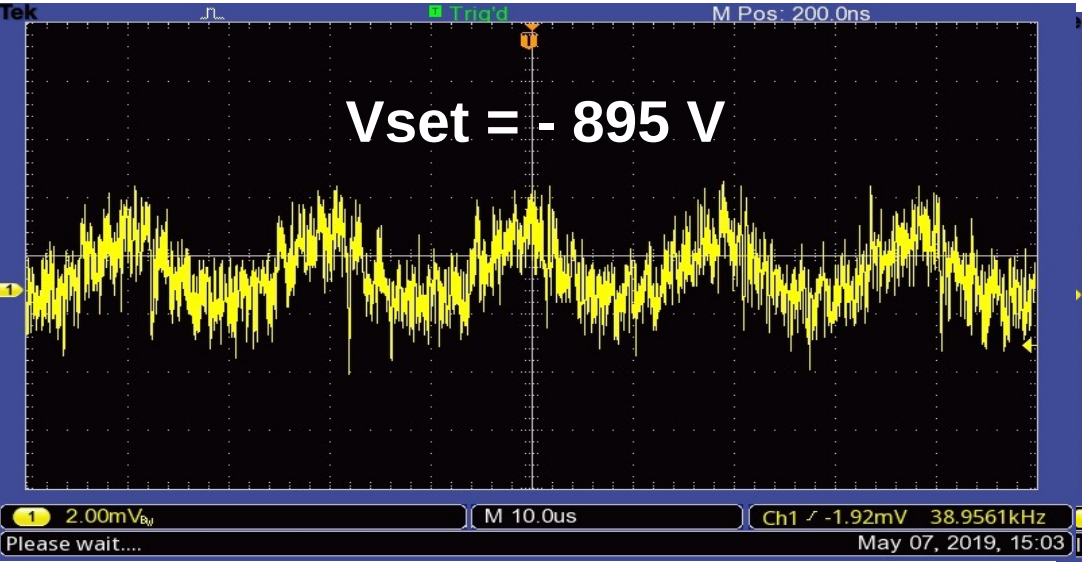


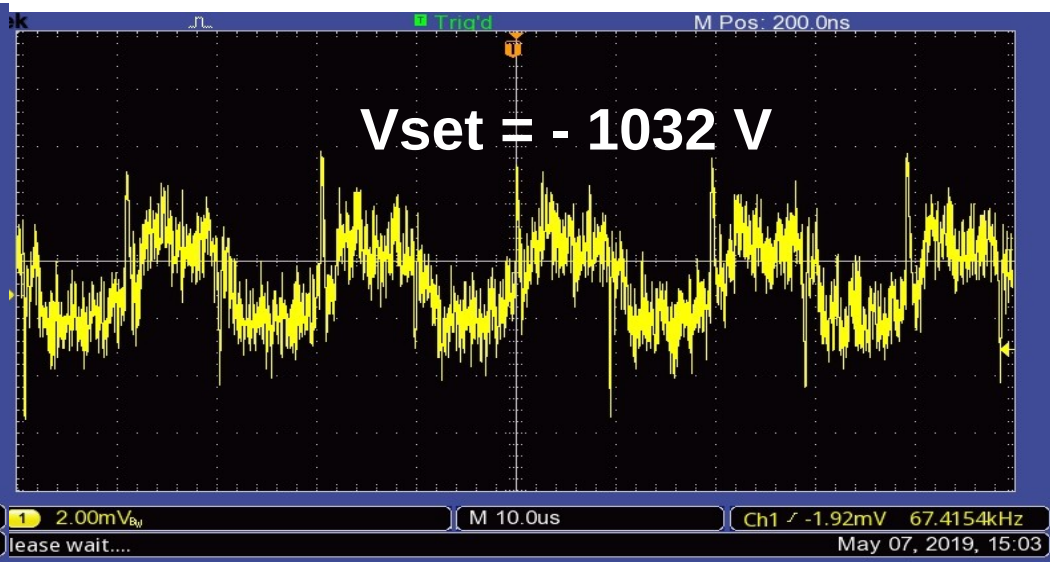
R = 2 MΩ. Ripple within specs.

HV ripple measurement (1 MΩ)





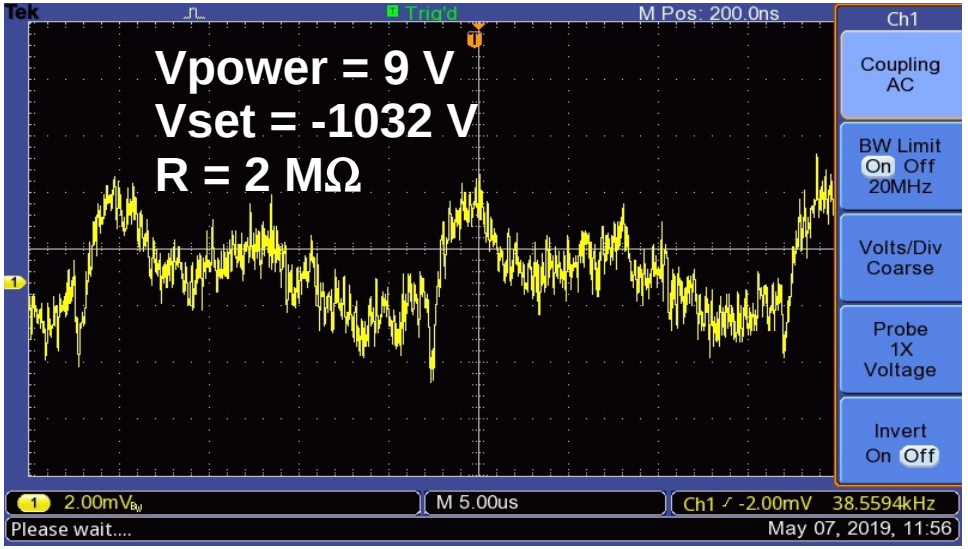


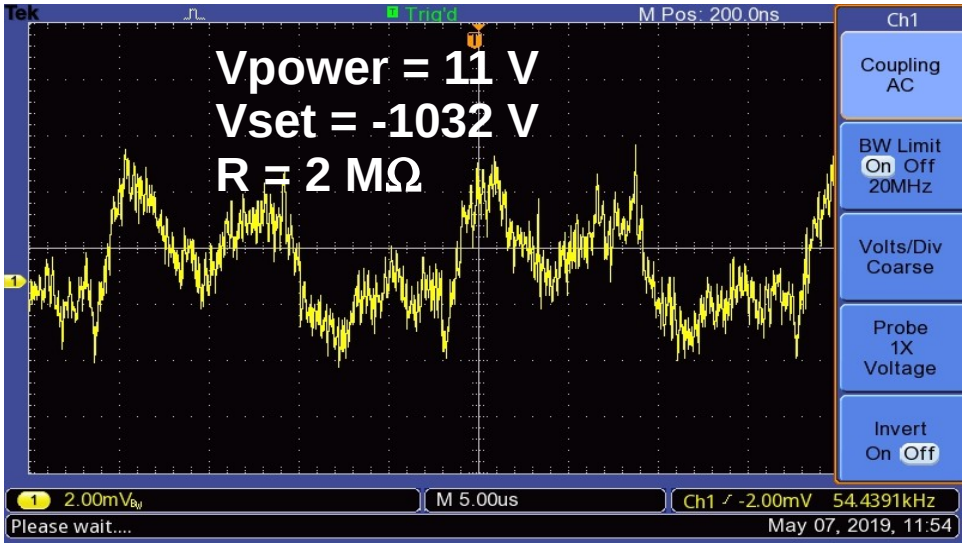


R = 1 MΩ. Ripple within specs.

HV block power tests

HV powered with 12 V (Vpower) directly from the ROB power input.
Tolerance on 12 V: 10% from datasheet.
Tested HV block power from 12 V down to 9 V.
In JUNO Top Tracker, different voltage drops according to module cable length.





Ripple within specs down to Vpower = 9 V.
Vout = Vset down to Vpower = 9.5 V; for Vpower = 9 V, Vout < Vset .
HV block can be safely operated down to Vpower = 10 V (power cable choice).
The rest of the board circuits can be safely operated down to 9 V.