# Verso un «Warm demostrator»

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Short term work plan

- Present SiPM technology has limitations in fine granularity: most common applications require big area and few channels, while we require big area with fine pitch and analogue readout of each SiPM!

- The final solution will be probably backside illumination to reduce the size of the SiPM and 3D integration for front end and readout electronics…but the timescale is well beyond few years from now.

- We want to build a demonstrator with present available SiPM matrix and warm electronics just to validate the approach with the Hadamard mask. A prototype capable to reconstruct simple pattern would be a success

What SiPM sensors are available now ?

- Hamamatsu sells matrices of 1 mm2 SiPMs:
  - 4x4, 8x8, 16x16

- We bought last year: two 8x8 and one 16x16
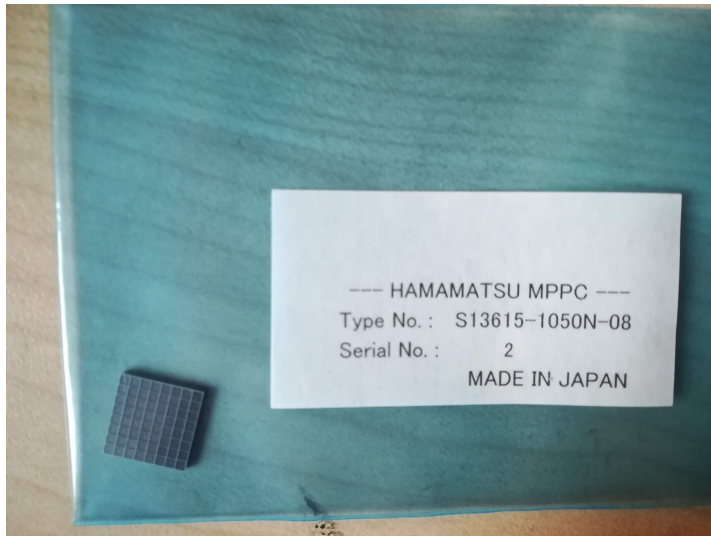
Such granularity and sizes do allow to build a demonstrator?

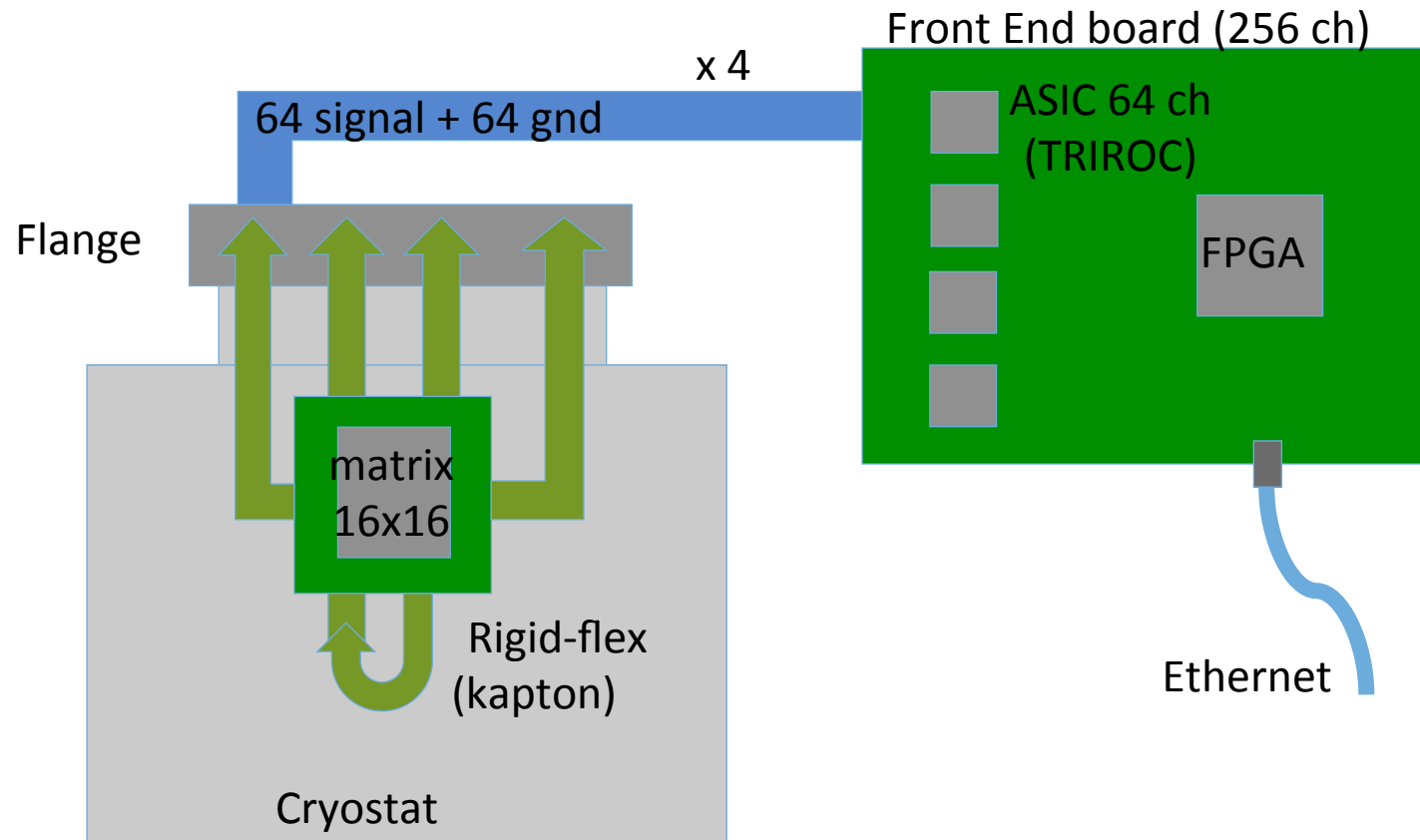-> simulation should give some input!

What available ASIC could be used?

- TRIROC from Weeroc seems to be a valid candidate:

Detector Read-Out	SiPM, SiPM array
Number of Channels	64
Signal Polarity	Positive or Negative
Sensitivity	Trigger on first photo-electron
Timing Resolution	88 ps RMS
Dynamic Range	3000 photo-electrons (10^6 SIPM gain), Integral Non Linearity: 1% up to 2000 ph-e
Packaging	BGA (12x12mm, 353 balls)
Power Consumption	Power supply: 3.3V 10mW/ch
Inputs	64 voltage inputs with DC adjustment for SiPM HV tuning
Outputs	Digital output (energy on 10 bit, time on 10 bit - 30ps bin) 1 multiplexed time trigger output 2 ASIC trigger OR outputs (64 channels, 2 levels)
Internal Programmable Features	64 HV adjustment for SiPM (64x8bits), trigger threshold adjustment (10bits), charge measurement tuning, ADC Track & Hold/Peak Sensing, 64 trigger masks, internal temperature sensor, trigger latch, Power Pulsing

TRIROC Demo Board

2 input connectors

TRIROC

FPGA
(Spartan 6)

Approccio Warm electronics

- Solamente i sensori stanno dentro criostato
- Scheda di front-end esterna
- 4x ASIC (64 ch) commerciali
- verificare connettori ad alta densita, SNR, xtalk

Front End board (256 ch)

x 4

64 signal + 64 gnd

ASIC 64 ch (TRIROC)

FPGA

Flange

matrix 16x16

Rigid-flex (kapton)

Ethernet

Cryostat

First step

- Use 8x8 device for electrical tests:
  - Mount it on a rigid-flex PCB (routing)
  - Look at individual signals(signal integrity, noise, xtalk)
  - Read the matrix with TRIROC Asic (demo board)

- Put the 8x8 matrix in liquid Nitrogen:
  - Check mechanical resistance to thermic stress (even if already verified by Hamamatsu)
  - Study the signal , noise , crosstalk etc..

Contact pads: 8x8 matrix

S13615-1050N-08 DATA SHEET
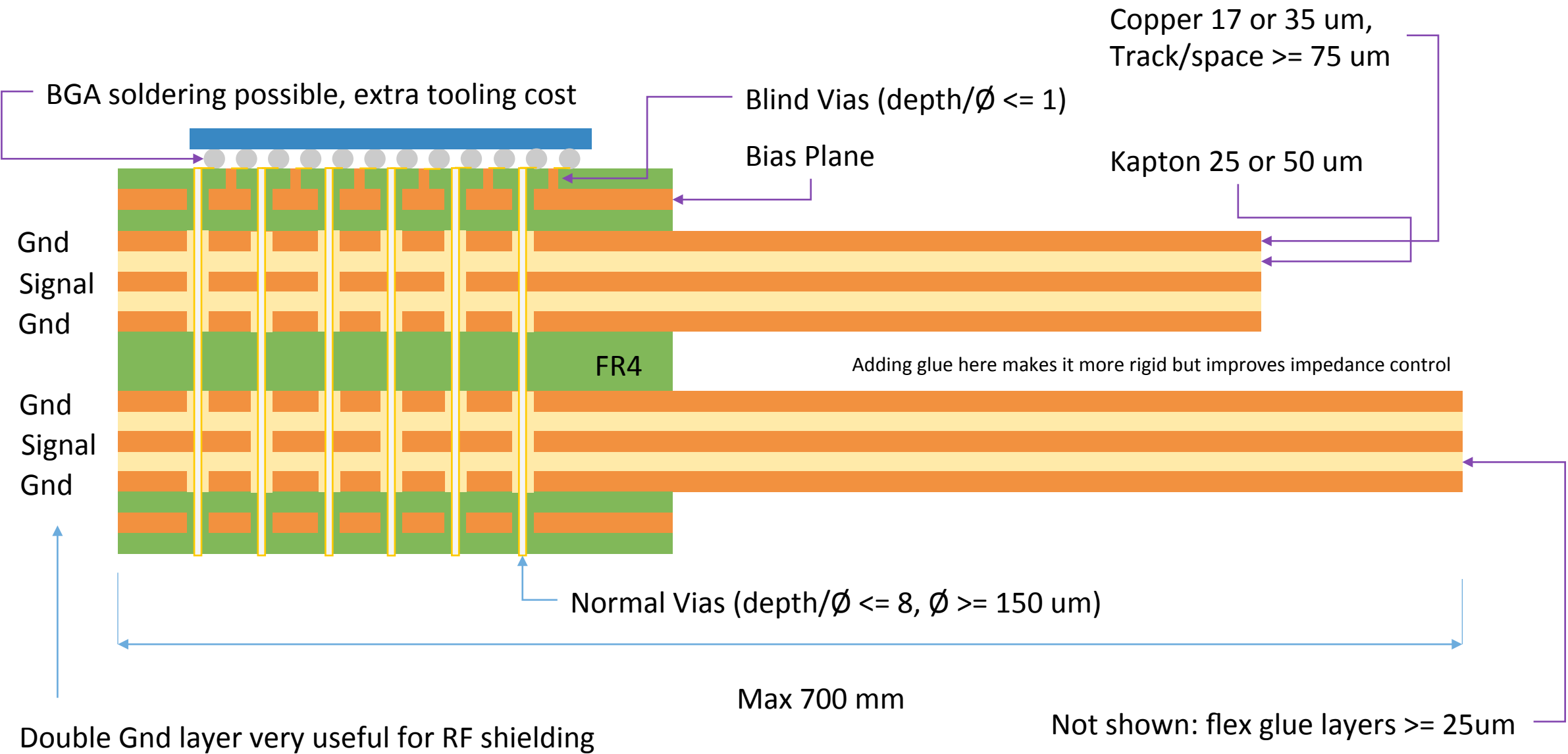
■Dimensional outline（unit: mm）
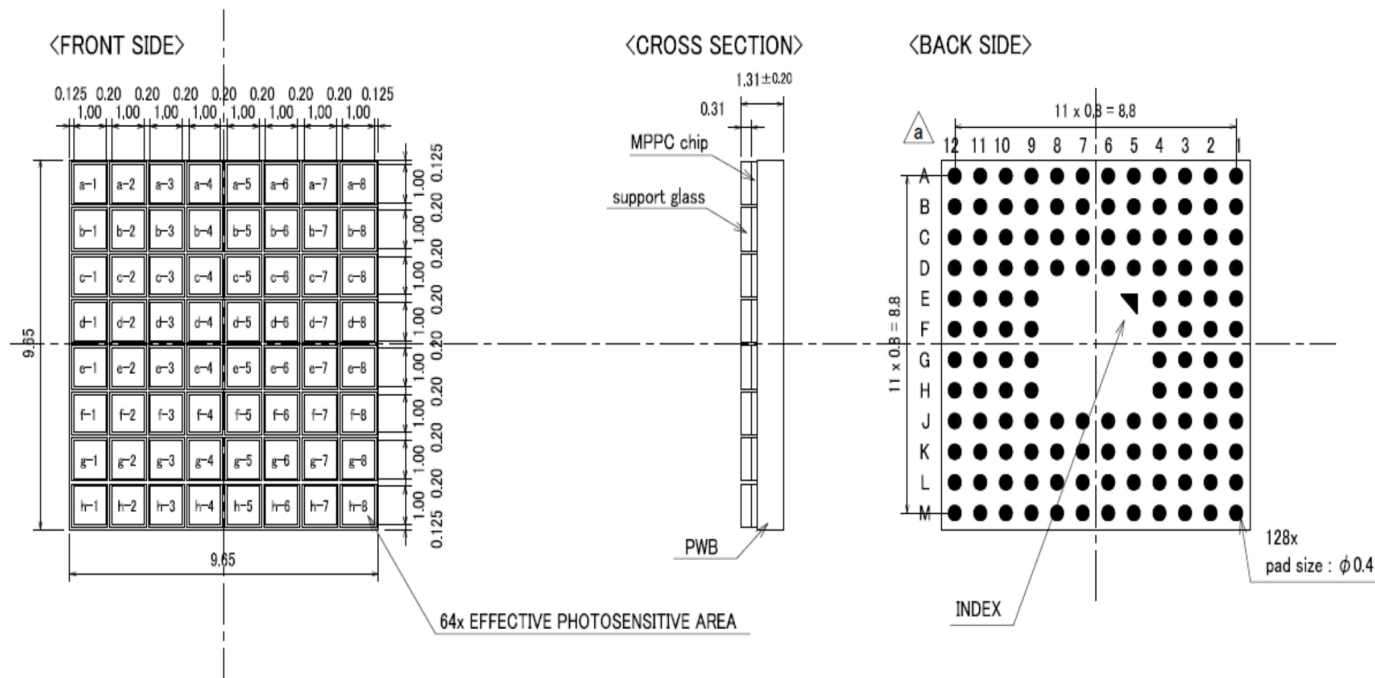
- BGA like pads
- pitch 1.2 mm
- space between pads 0.8 mm

Mounting/cabling solution for 8x8 Matrix

Rigid-Flex PCB works as mounting point for the matrix and also as cable for the 64 analog signals.
CERN workshop has already produced a few rigid-flex for cryo use, claims base materials and selected glues are ~ok.

Rigid

Flex

Rigid

Connector for TRIROC Demo-Board (32 ch each)

Optional split to improve flexibility

A few channels also on coax for testing

A little space for HV filter, a temperature sensor, a test pulse LED, …

> 20 mm

<600 mm

PCB larger than matrix to ease routing congestion
(Once more experienced, may try 2 sides edgeless to create 1kpix camera with 4 x 16x16)
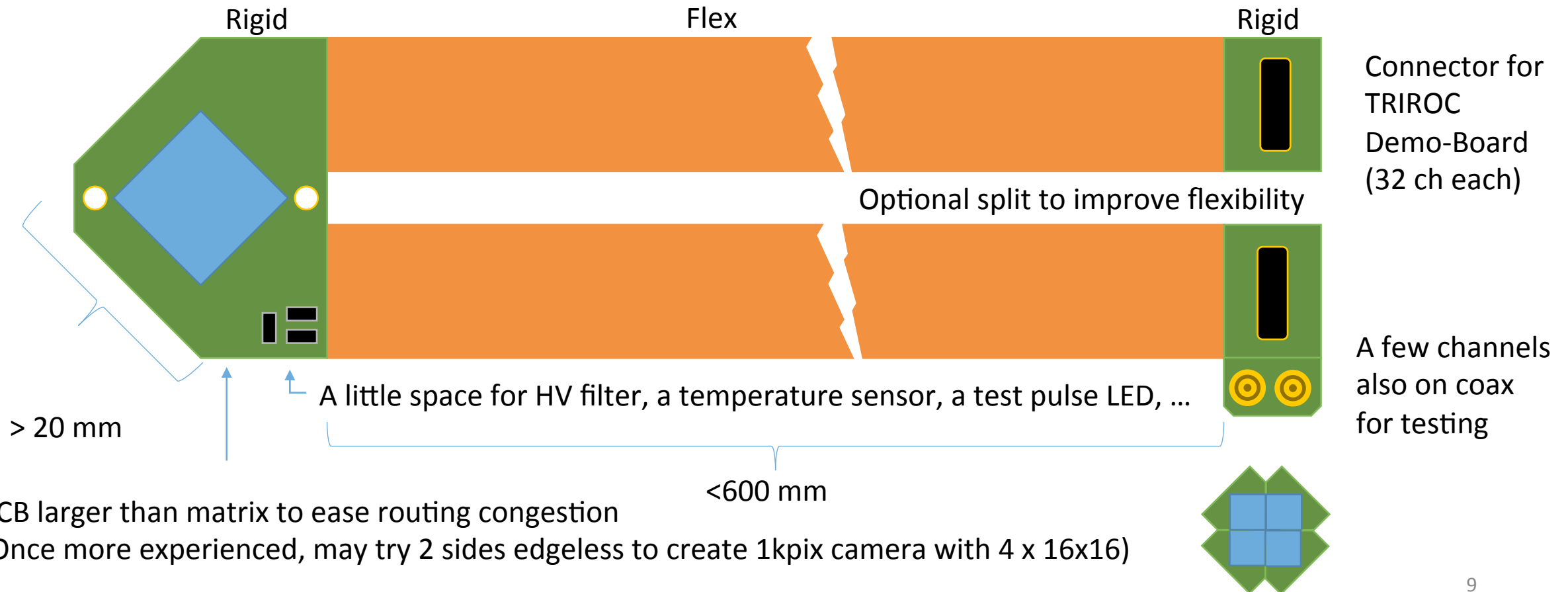
PCB stackup (CERN capabilities)

BGA soldering possible, extra tooling cost

Blind Vias (depth/Ø <= 1)

Bias Plane

Copper 17 or 35 um,
Track/space >= 75 um

Kapton 25 or 50 um

Gnd

Signal

Gnd

FR4

Adding glue here makes it more rigid but improves impedance control

Gnd

Signal

Gnd

Normal Vias (depth/Ø <= 8, Ø >= 150 um)

Max 700 mm

Not shown: flex glue layers >= 25um

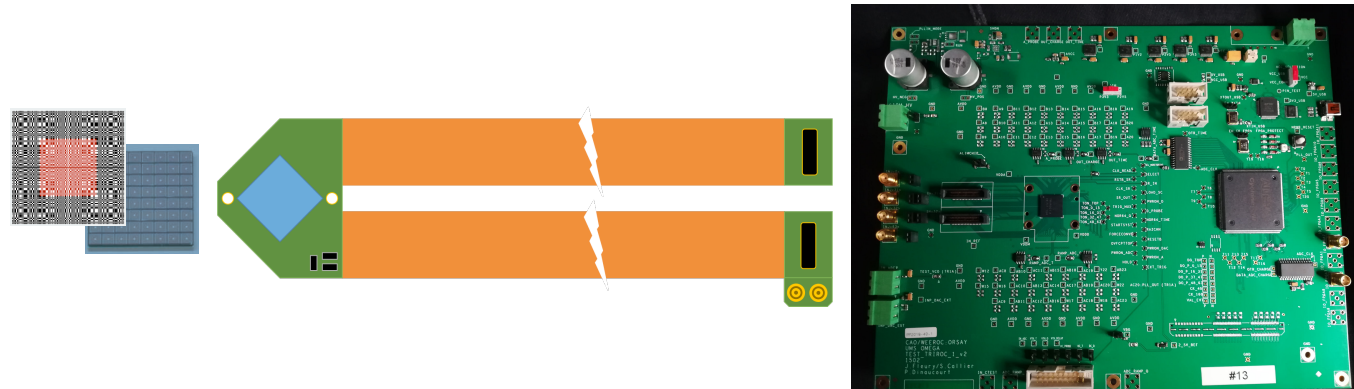Double Gnd layer very useful for RF shielding

Warm demonstrator (1)

IF from simulation we have indication that we can reconstruct some very simple pattern with 8x8 matrix

 Hadamard mask - > SiPM matrix 8x8 - > flex - > TRIROC demo board

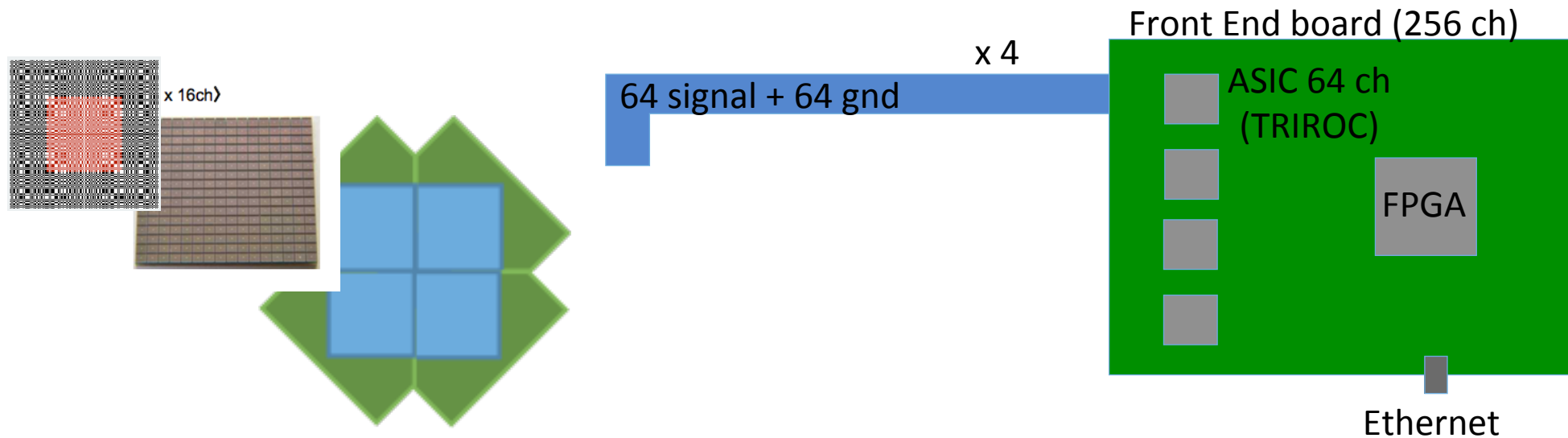Test in a black box the reconstruction of simple light patterns

Anyway it is a mandatory exercise to test the SiPM matrix and the ASIC

Warm demonstrator (2)

ELSEIF from simulation we have indication that we have to use at least 16x16 matrix, we need to build a new FE/DAQ board that can deal with 256 channels:

Hadamard mask - > SiPM matrix 16x16 - > 4 flex - > board 4 TRIROC

Test in a black box

x 16ch⟩

64 signal + 64 gnd

x 4

Front End board (256 ch)
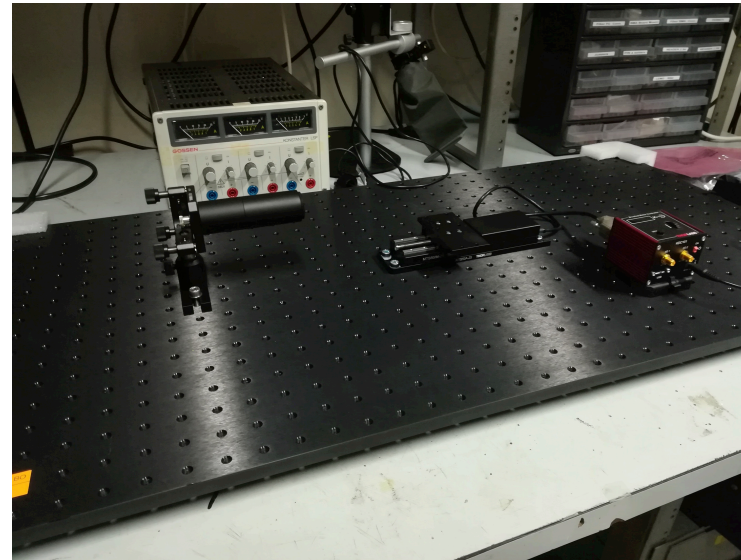
ASIC 64 ch (TRIROC)

FPGA

Ethernet

Black box

- Laser + micrometric 2d stage -> test electronics + SiPM crosstalk
- Led + black panel with grooved patterns -> test reconstruction with mask
- ….

under construction

available

Contact pads Hamamatsu 16x16