The Clock/Sync Distribution & a Streaming Readout TDC

William Gu
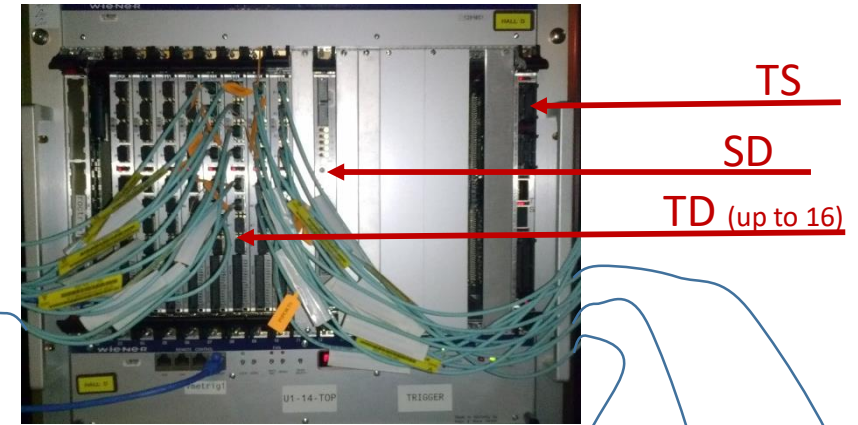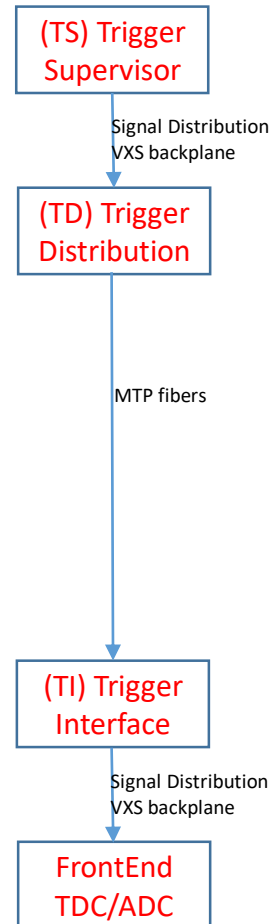
Streaming Readout IV
22-24 May 2019, Camogli

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1. JLAB HallB/D Trg/Clk/Sync/Busy overview

MTP Fiber assignment:

Trigger etc.

Clock

Sync

FiberMeas

FiberMeas

Not_used

Not_used

Acknowledge/Busy

TS/TD → TI (front end)
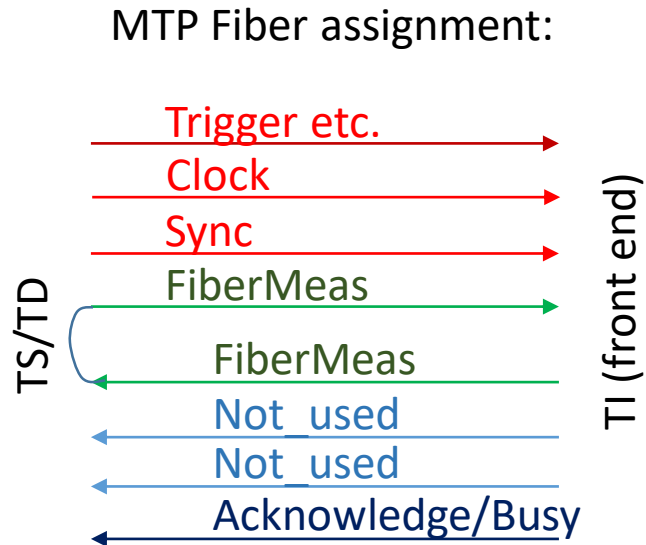
- Same clock for the system;
- Frontend electronics is Synced to one clock period (4 ns);
- Delay adjustment on TI to compensate for the fiber delays;
- Clock jitter: several ps

(TS) Trigger Supervisor

Signal Distribution
VXS backplane

(TD) Trigger Distribution

MTP fibers

(TI) Trigger Interface

Signal Distribution
VXS backplane

FrontEnd TDC/ADC

TS

SD

TD (up to 16)

~60

TI

FronEnd Readout electronics

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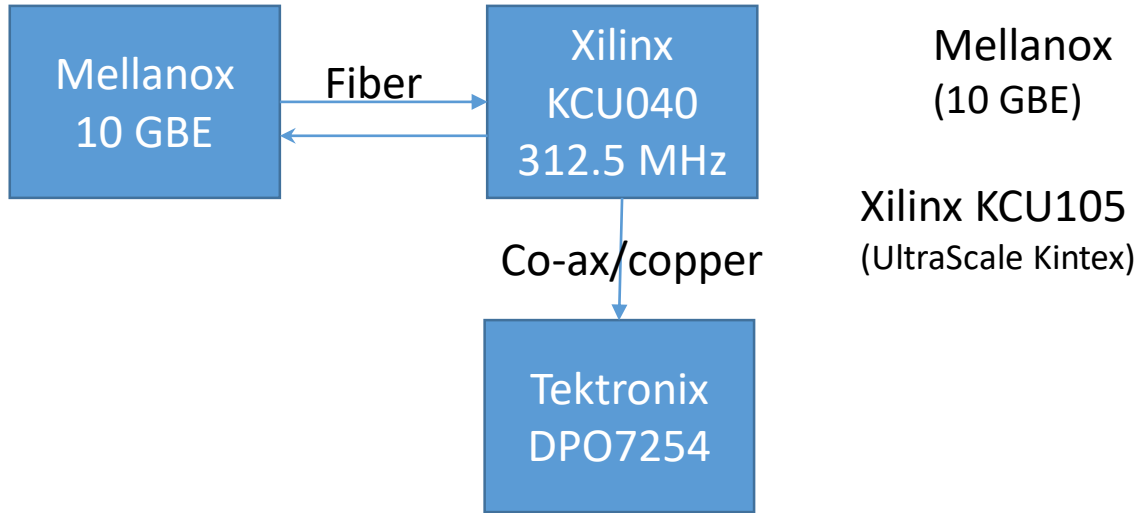
2. Clock Recovery Study

2.1 Low jitter clock can be recovered

Clock result:

Period: 3.2000ns, Frequency: 312.50 MHz

Std Dev: 3.28 ps, 320.2 KHz

P_P: 29.3ps, 2.86 MHz

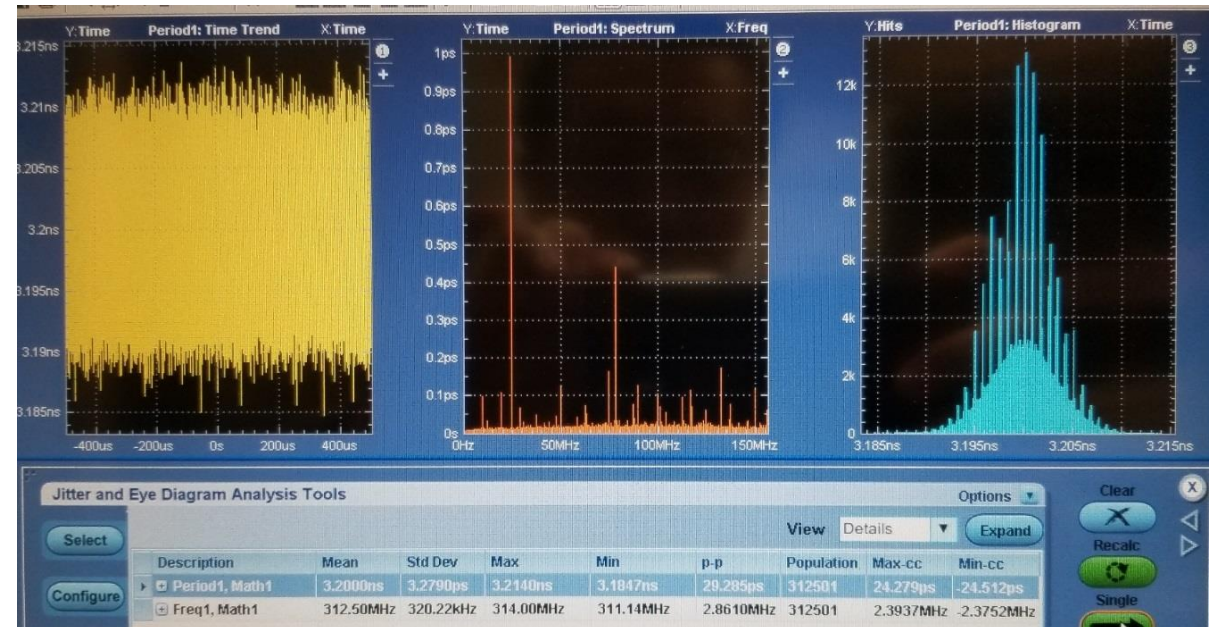Enabling the Mellanox TX, Std Dev → 3.30 ps

Enabling the KCU040 TX, Std Dev → 6.42 ps

Single pulse period measurement: Std Dev: 6~7 ps
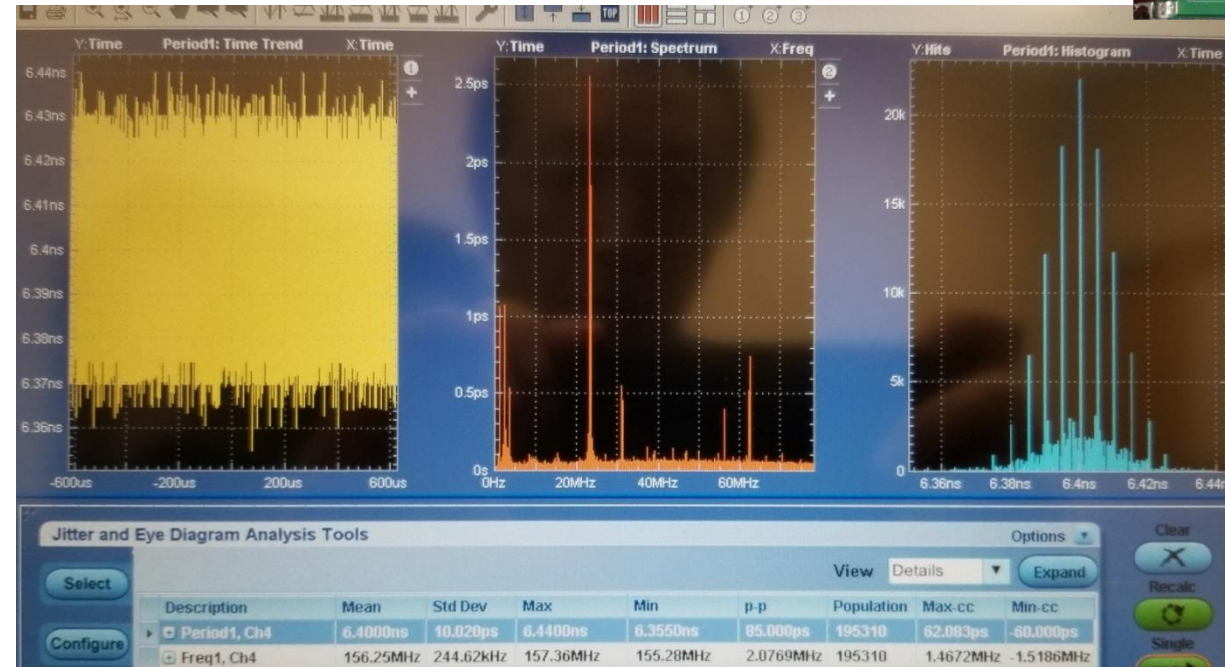
DPX mode (200 GSps): 700~900 fs

Mellanox
(10 GBE)

Xilinx KCU105
(UltraScale Kintex)

Recovered clock to Tektronix DPO7254

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2. Clock Recovery Study

2.2 One→Two clock recovery

| Xilinx KCU1500 6.25 Gbps | → | VETROC Xc7a200 312.5/2 |

QSFP transceivers/Fiber
Xilinx Aurora-64B66B
& Aurora-8b10b

| VETROC Xc7a200 312.5/2 |
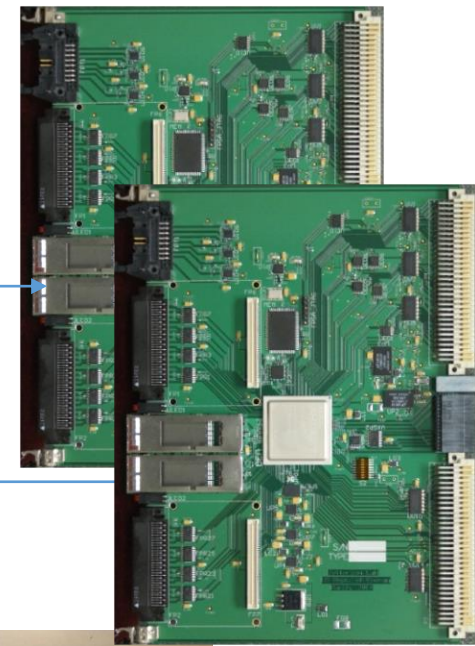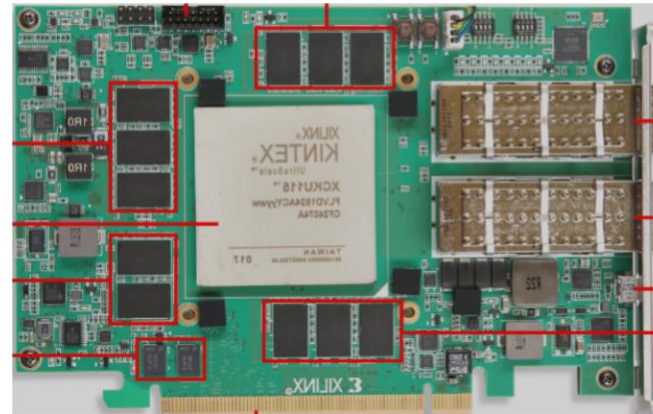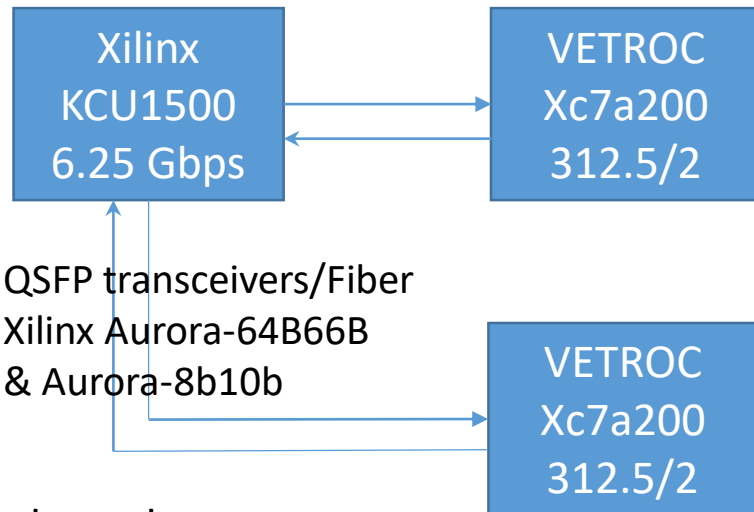
Clock result:
Period: 6.4000ns, Frequency: 156.25 MHz
Std Dev: 10.02 ps, 244.6 KHz
P_P: 85ps, 2.08 MHz

Single pulse period meas.: Std Dev: 7.5 ps
DPX mode (200 GSps): 778 fs

*VETROC FPGA → Scope: long LVCMS, then differential
PCB traces. 312.5 MHz impossible

2. Clock Recovery Study

2.3 Clock wandering probem

Trigger on the VETROC_A recovered clock, the VETROC_B recovered clock width P_P is about 200ps !

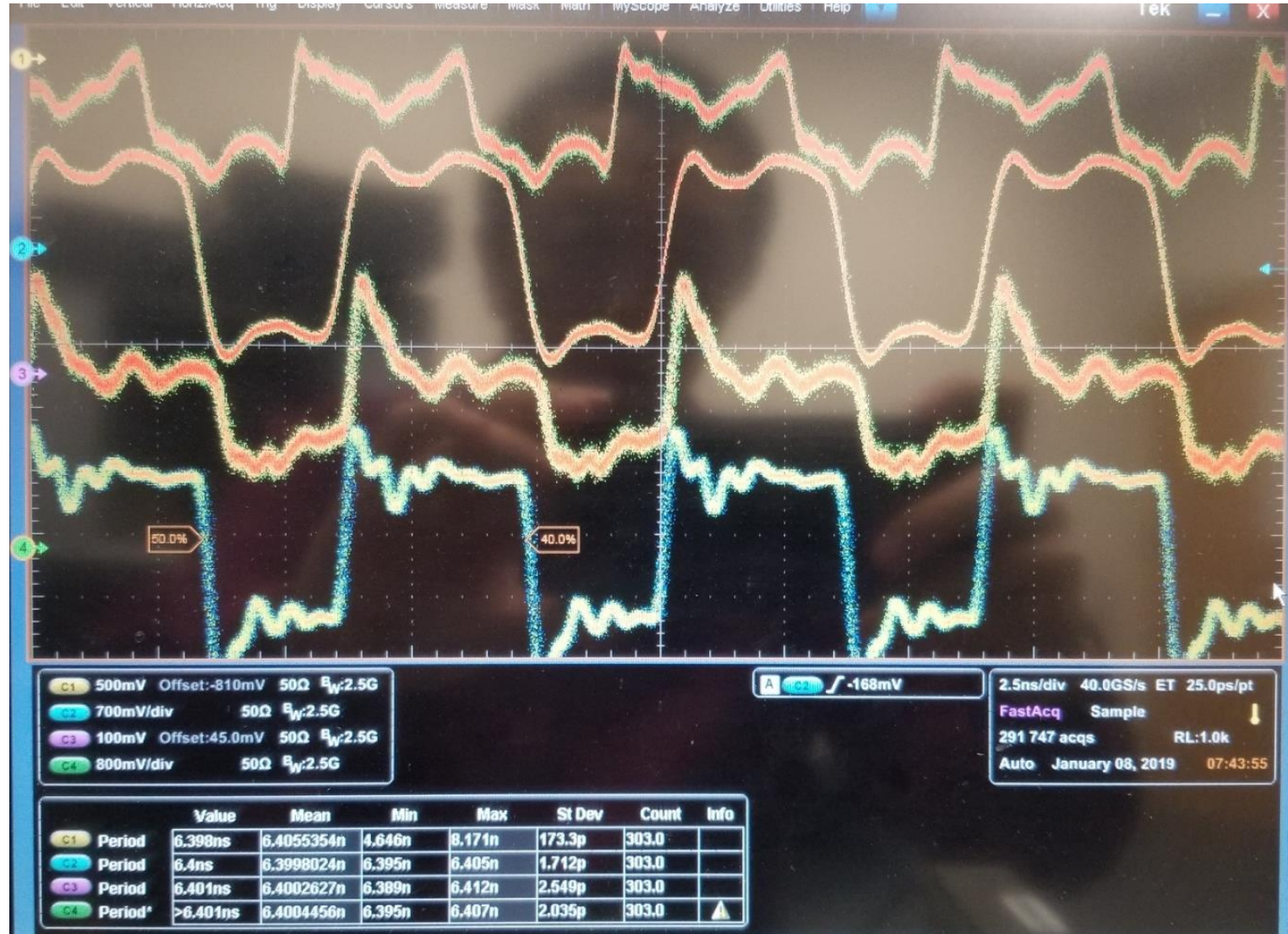- All these four channels are reconstructed KCU1500 clock
- Ch#1 and Ch#2 have narrow spread as ch#2 is the trigger source
- Ch#3 and Ch#4 have wide spread (~200ps)
- Ch#2: Width: 6.4ns, Std Dev: 1.71ps
- Ch#4: Width: 6.4ns, Std Dev: 2.54ps
- The phase between Ch#1/2 and Ch#3/4 are changing (within a clock cycle) when re-link, though the phase is pretty stable. This is caused by the CDR clock devision.

Ch#1: VETROC_A, MGT#2 RxClk, single-ended probe
Ch#2: VETROC_A, MGT#3 RxClk, differential probe
Ch#3: VETROC_B, MGT#2 RxClk, single-ended probe
Ch#4: VETROC_B, MGT#3 RxClk, differential probe

		Value	Mean	Min	Max	St Dev	Count	Info
C1	Period	6.398ns	6.4055354n	4.646n	8.171n	173.3p	303.0	
C2	Period	6.4ns	6.3998024n	6.395n	6.405n	1.712p	303.0	
C3	Period	6.401ns	6.4002627n	6.389n	6.412n	2.549p	303.0	
C4	Period*	>6.401ns	6.4004456n	6.395n	6.407n	2.035p	303.0	⚠

2. Clock Recovery Study

2.3 Clock wandering probem (continued)

The difference between two reconstructed clocks.
The width of the difference of the two reconstructed clocks from the SAME vetroc board is measured to be (one differential probe):

    Width: 336 ps
    Std Dev: 3.75 ps

The width of the difference of the two reconstructed clocks from two VETROC boards is measured (two differential probes with scope math) to be:

    Width: ~472/822 ps (mean 458/781 ps)
    Std Dev: ~35/50 ps (p_p ~210/347 ps)
    (Positive/Negative, not precise meas.)

2. Clock Recovery Study

2.3 Clock wandering probem (continued)

Fundamental problem: TIE (Total Interval Error), not jitter. The TIEs are asynchronous among the recovered clocks.
The recovered clock depends on the data protocol (consecutive number of 1s or 0s in the data stream)

ADC measurement effects:
* Clock Jitter affects the measurement precision;
* The TIE effect is not critical

TDC measurement effects:
* The TIE affects the measurement precision (channel to channel alignment, unless a precision common signal is used as the time reference);
* The jitter effect is not critical as the jitter is much smaller than the TDC measurement precision

Data transmission effects:
* Clock Jitter affects the data transmission;
* The TIE effect is not critical

A typical clock recovery circuit
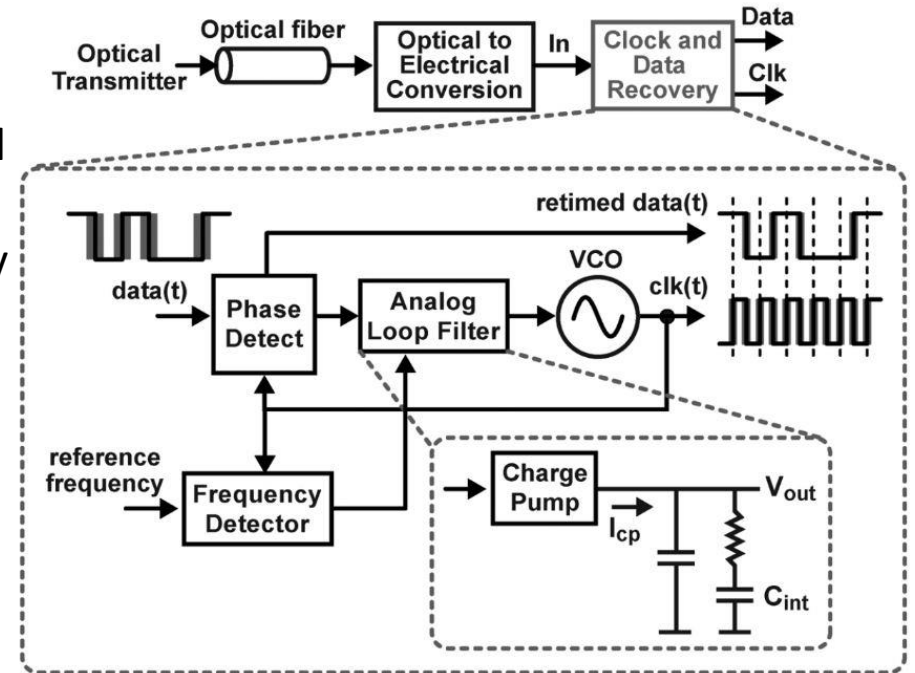
A 2.5-Gb/s Multi-Rate 0.25-μm CMOS Clock and Data Recovery Circuit Utilizing a Hybrid Analog/Digital Loop Filter and All-Digital Referenceless Frequency Acquisition
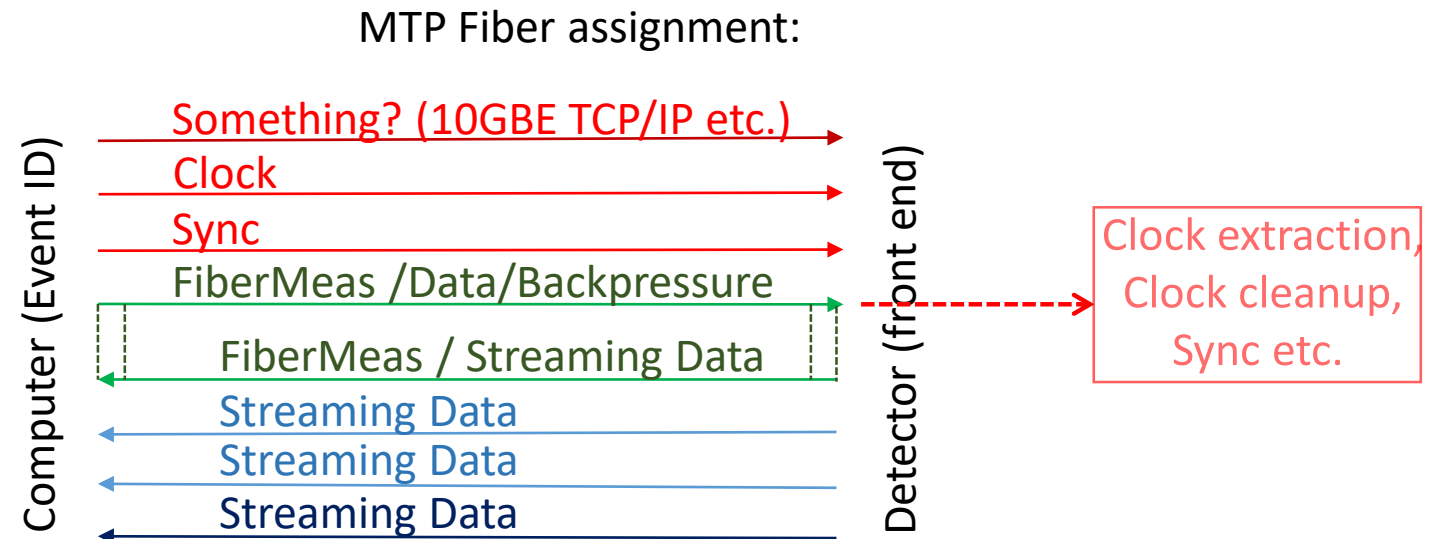
Michael H. Perrott, Yunteng Huang, *Member, IEEE*, Rex T. Baird, Bruno W. Garlepp, *Member, IEEE*, Douglas Pastorello, *Member, IEEE*, Eric T. King, *Member, IEEE*, Qicheng Yu, Dan B. Kasha, Philip Steiner, Ligang Zhang, Jerrell Hein, and Bruce Del Signore

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2. Clock Recovery Study

2.4 Clock/Sync distribution tree

It is not expensive ($50 for a 40 Gbps optic transceiver) to keep QSFP (easy) for Clock/Sync distribution and streaming data readout

Dedicated clock to keep the edge information (low jitter, no wandering), but, we will keep an eye on the LpGBT development at the LHC

MTP Fiber assignment:

Computer (Event ID)

Something? (10GBE TCP/IP etc.)
Clock
Sync
FiberMeas /Data/Backpressure
FiberMeas / Streaming Data
Streaming Data
Streaming Data
Streaming Data

Detector (front end)

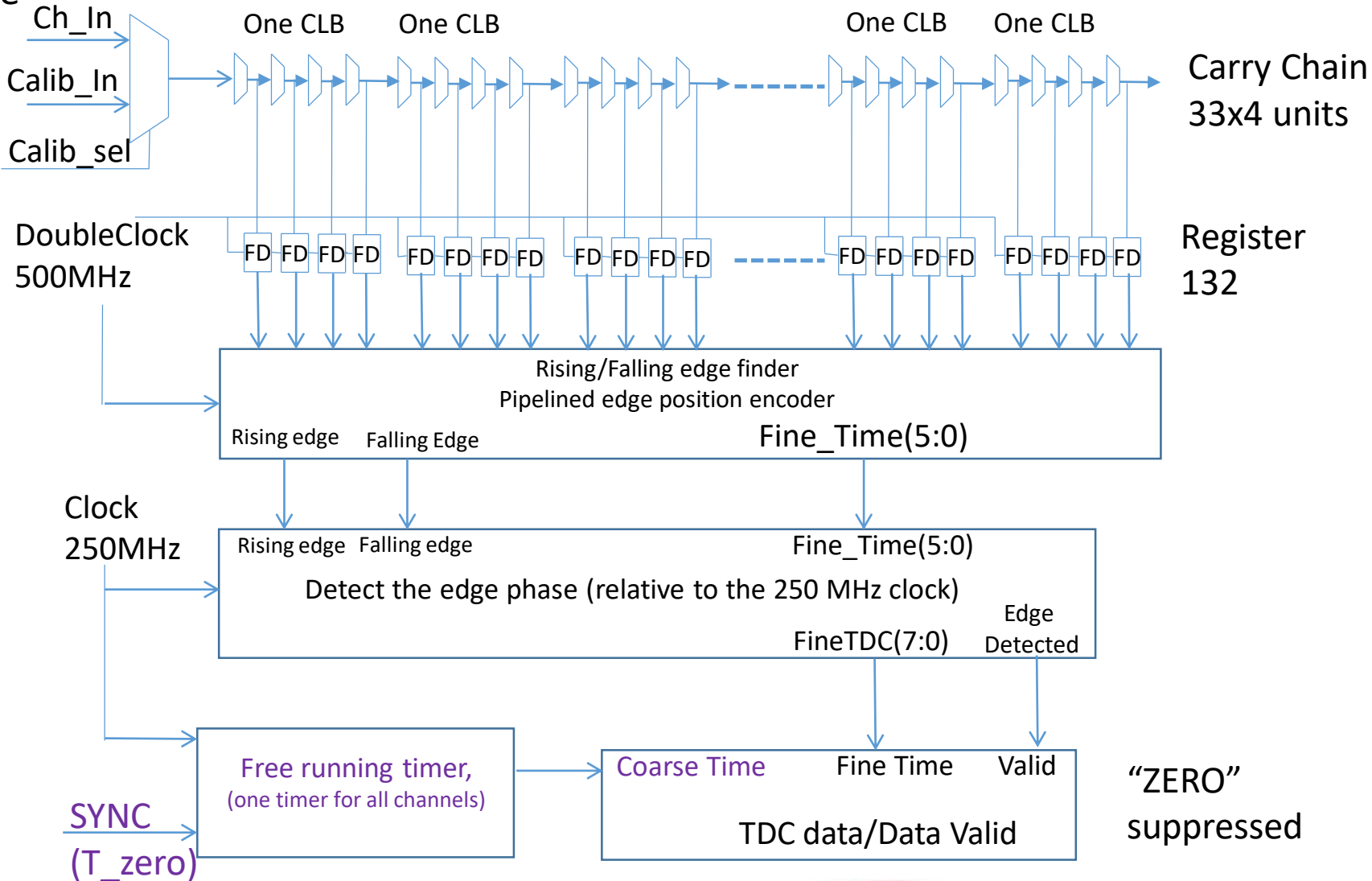Clock extraction, Clock cleanup, Sync etc.

3. VETROC Streaming TDC
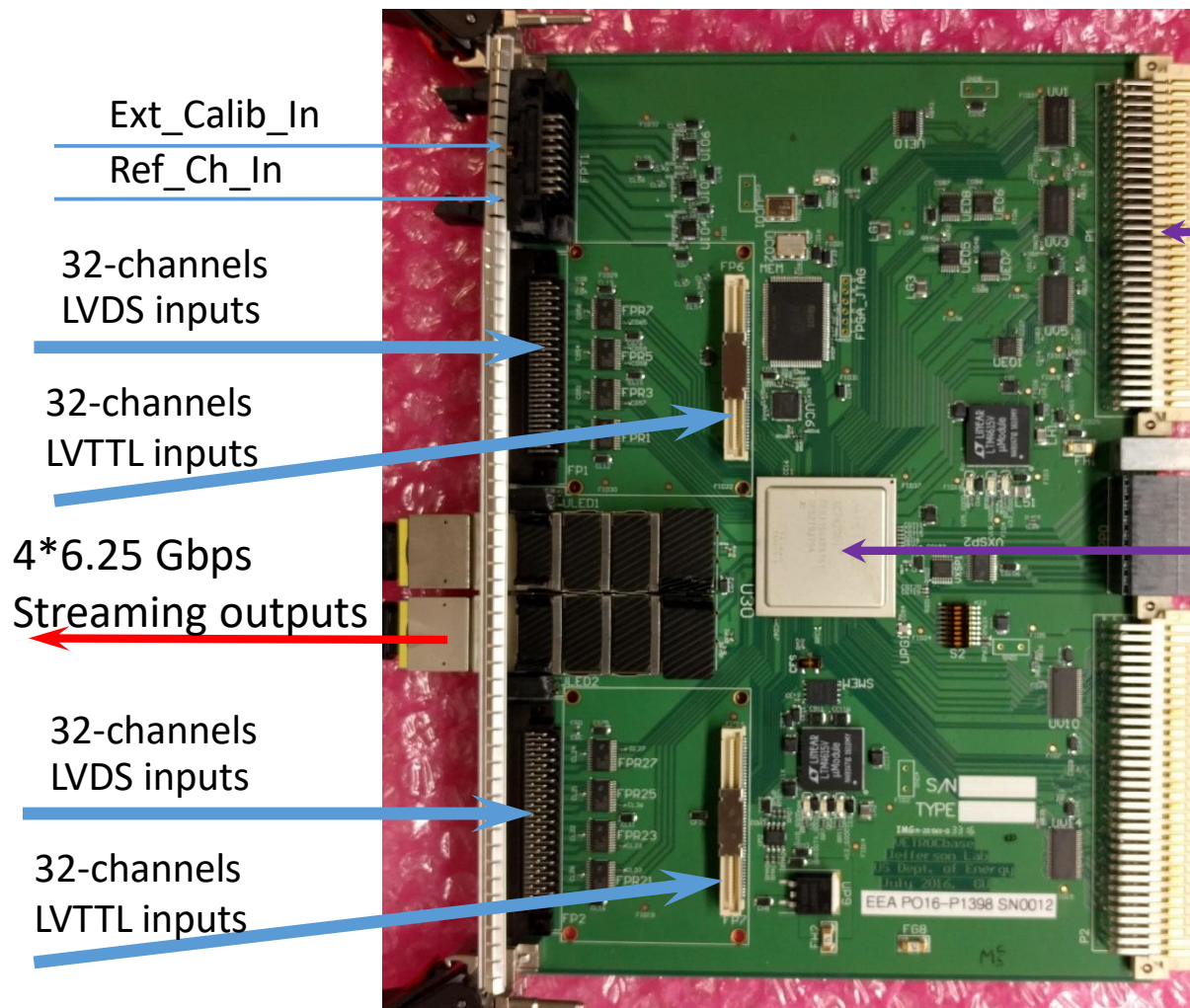
3.1 TDC measurement principle

The edges of the pulse is measured against the system clock:

- precision part: phase in the clock (using Xilinx FPGA carry chain delay and clock registers);
- coarse part: number of clock cycles since system reset (T_zero) (a synchronous counter)

Ch_In

Calib_In

Calib_sel

One CLB   One CLB   One CLB   One CLB

Carry Chain
33x4 units

DoubleClock
500MHz

FD FD FD FD   FD FD FD FD   FD FD FD FD   ------   FD FD FD FD   FD FD FD FD

Register
132

Rising/Falling edge finder
Pipelined edge position encoder

Rising edge   Falling Edge   Fine_Time(5:0)

Clock
250MHz

Rising edge   Falling edge   Fine_Time(5:0)

Detect the edge phase (relative to the 250 MHz clock)

FineTDC(7:0)   Edge Detected

Free running timer,
(one timer for all channels)

Coarse Time   Fine Time   Valid

"ZERO"
suppressed

SYNC
(T_zero)

TDC data/Data Valid

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3. VETROC Streaming TDC

3.2 VETROC Streaming TDC

Ext_Calib_In

Ref_Ch_In

32-channels
LVDS inputs

32-channels
LVTTL inputs

VME 64

4*6.25 Gbps
Streaming outputs

xc7A200 FPGA

32-channels
LVDS inputs

32-channels
LVTTL inputs

EEA PO16-P1398 SN0012

Data Format (128 bits)

Bits (127-124) (123:104) (103:78) (77:52) (51:26) (25:0)
 TYPE   Timer   Ch#A   Ch#B   Ch#C   Ch#D
                Timer(28:9)

(25:20 : 19:8   :   7   :   6 :   5 : 0)
 CH# Coarse_time Clk250 pulse Fine_time
 0-63 Time(11:0)   edge   edge   ~35ps

Bit(127:124) decoding:
- 0x8 for channels 1-32;
- 0x9 for channels 33-64;
- 0xA for channels 65-96;
- 0xB for channels 97-128;
- 0xF for reference channels

For reference channels, the full 48-bit timer is included, which keeps the unique time for about 290 hours after SYNC.

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3. VETROC Streaming TDC (backup slide)

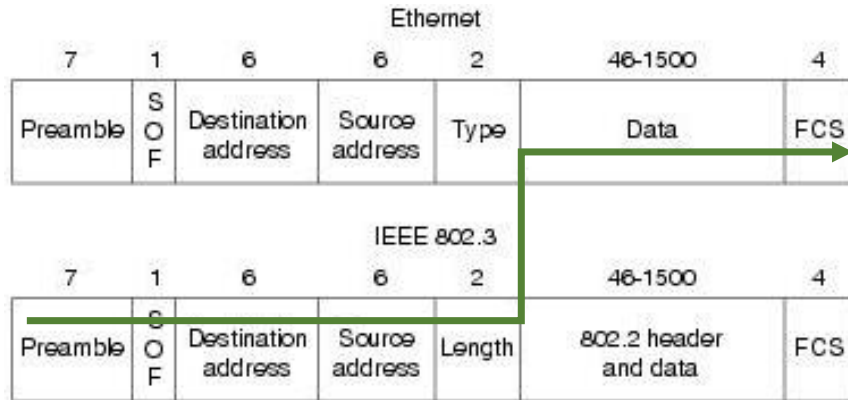## 3.2 VETROC Streaming TDC – 128 TDC channels with extra reference channels

Edge separation: <2.5ns;
LSB: ~35ps;
TimeStamp: ~10 days;
Streaming rate: ~2.5 Gbyte/s
Channel count: 128

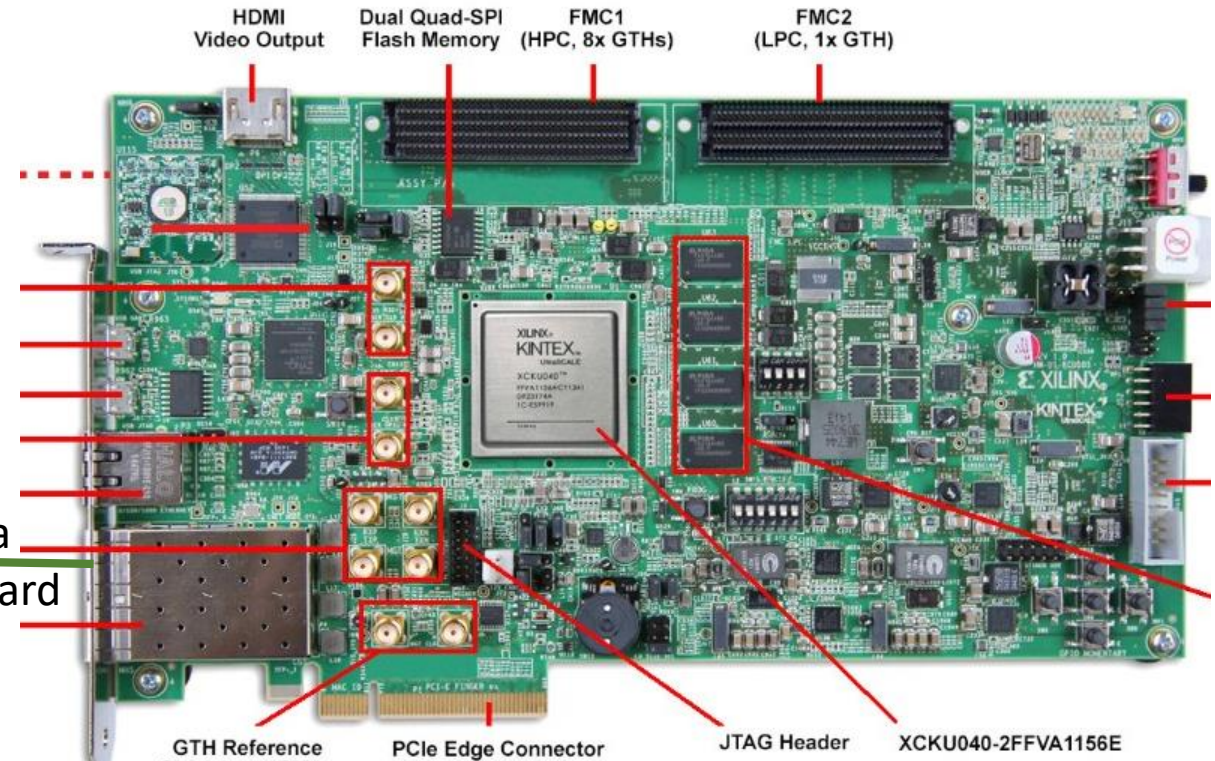Computers do not recognize the AURORA data stream
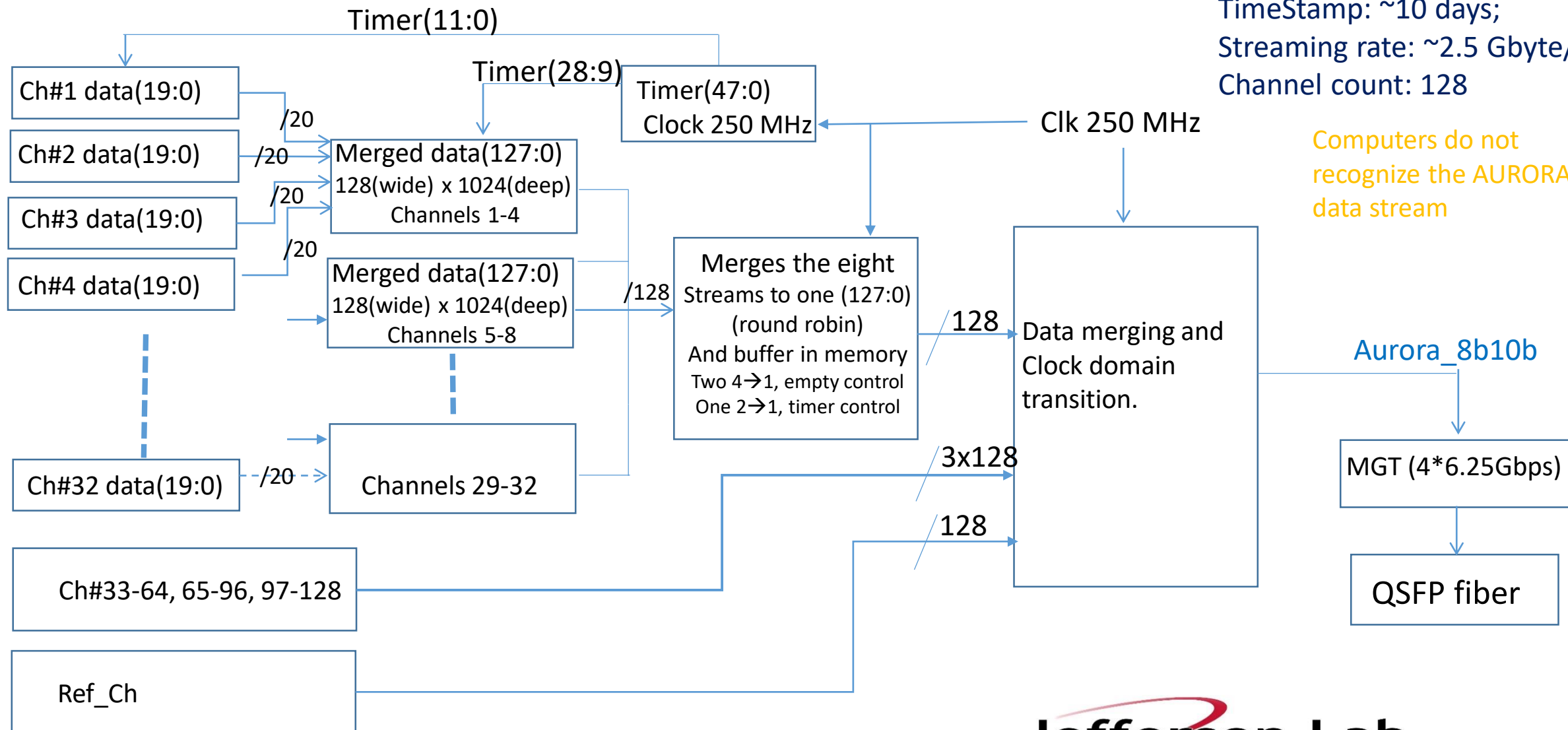
4. Streaming Readout:

4.1 10-GBE test using KCU105 eval board

SOF = Start-of-frame delimiter
FCS = Frame check sequence

(UDP) and skip the 802.2 header:
Reached: ~1.1 GByte/s (sustained)
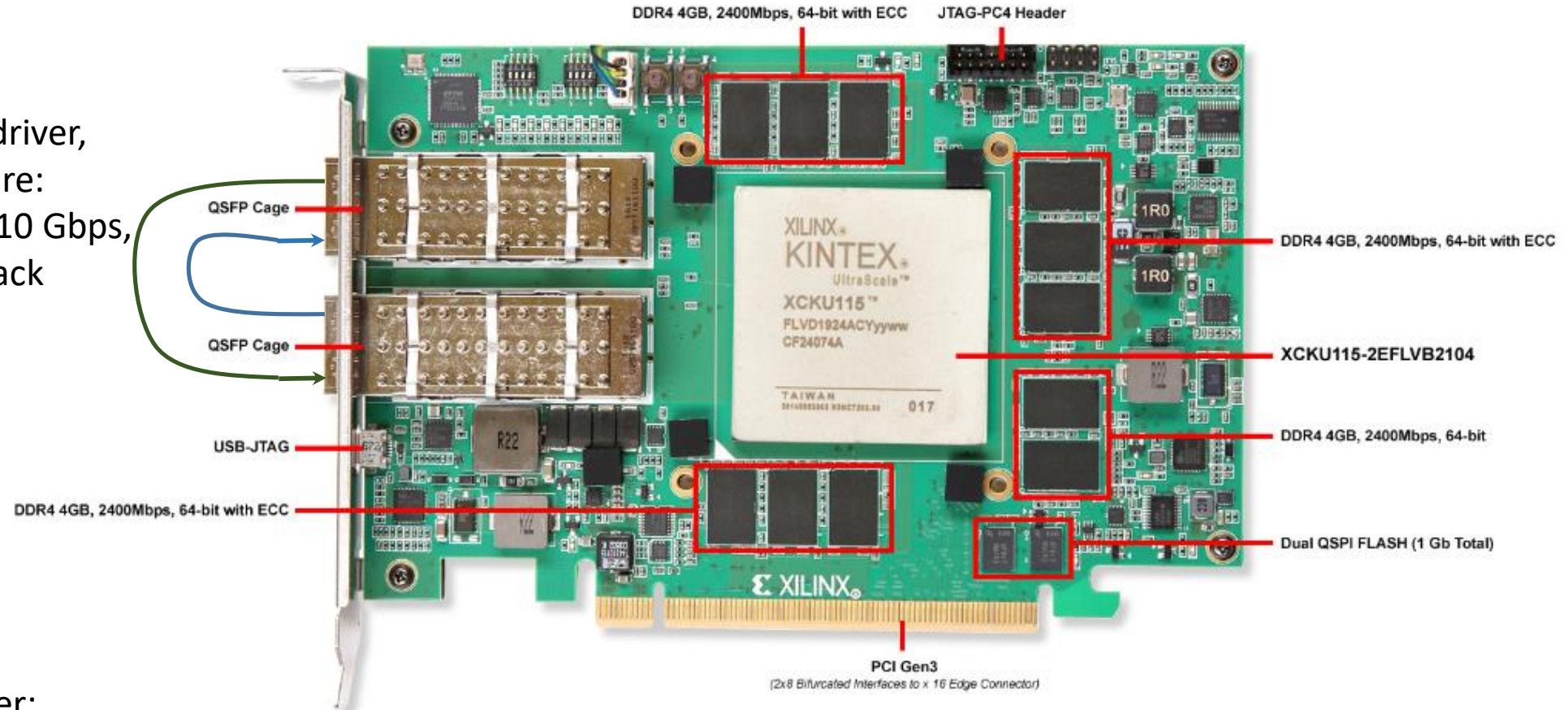 (from ifconfig ?trusted?)

10 GbE to a Mellanox card

4. Streaming Readout:

4.2 xDMA PCIe3x8 test using KCU1500 accelerator card

Using Xilinx's PCIe DMA driver, and modified test software:
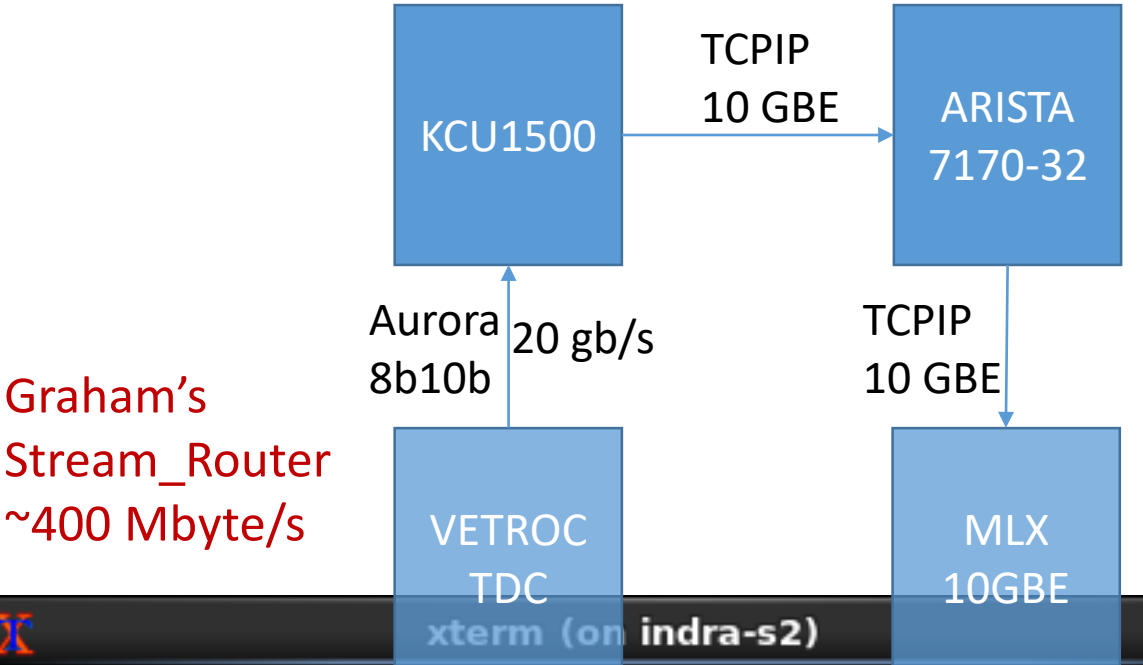QSFPs: Aurora 8-lane, 8x10 Gbps, 64b66b encoding, loopback through fiber

Achieved on the computer:
- Computer (memory) → KCU1500: 5600 MB/s
- AND KCU1500 → Computer (memory): 5200 MB/s.

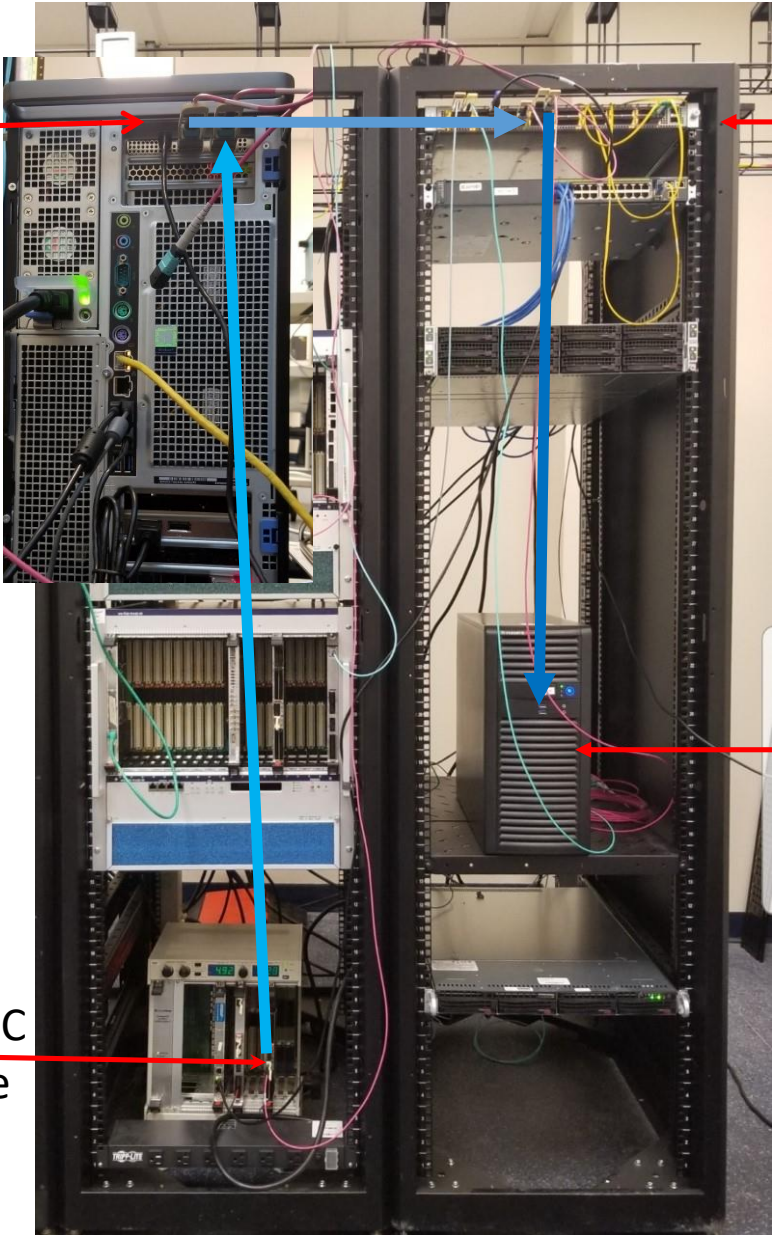# 4. Streaming Readout:

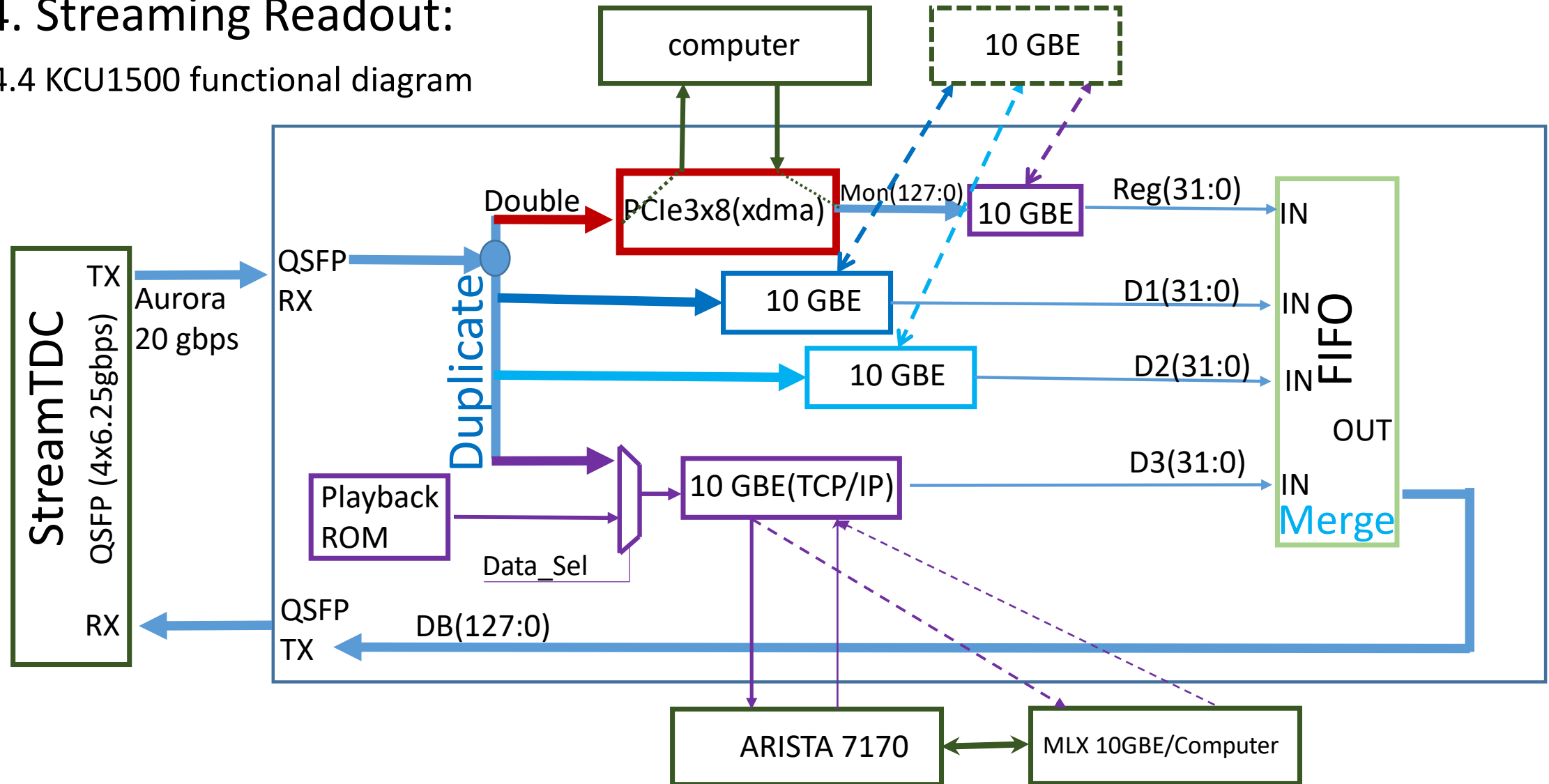## 4.3 TCP/IP readout (INDRA lab setup)

KCU1500 In ALKAID

ARISTA 7170-32C

MLX 10_GBE in INDRA-S2

VETROC TDC In VXS crate

Graph's Stream_Router ~400 Mbyte/s

```
KCU1500  --TCPIP 10 GBE-->  ARISTA 7170-32
   ^                              |
 Aurora 8b10b  20 gb/s       TCPIP 10 GBE
   |                              v
VETROC TDC                     MLX 10GBE
```

xterm (on indra-s2)

```
ID CODA0048 - buffer rate 379895.25 Hz, data rate 0.407248 GByte/s
ID CODA0048 - buffer rate 391878.30 Hz, data rate 0.420094 GByte/s
ID CODA0048 - buffer rate 381900.90 Hz, data rate 0.409398 GByte/s
ID CODA0048 - buffer rate 389568.43 Hz, data rate 0.417617 GByte/s
ID CODA0048 - buffer rate 382177.78 Hz, data rate 0.409695 GByte/s
ID CODA0048 - buffer rate 386047.66 Hz, data rate 0.413843 GByte/s
ID CODA0048 - buffer rate 369711.18 Hz, data rate 0.396330 GByte/s
ID CODA0048 - buffer rate 357362.87 Hz, data rate 0.383093 GByte/s
ID CODA0048 - buffer rate 376956.18 Hz, data rate 0.404097 GByte/s
ID CODA0048 - buffer rate 366132.41 Hz, data rate 0.392494 GByte/s
ID CODA0048 - buffer rate 398968.96 Hz, data rate 0.427695 GByte/s
ID CODA0048 - buffer rate 390347.00 Hz, data rate 0.418452 GByte/s
ID CODA0048 - buffer rate 393121.97 Hz, data rate 0.421427 GByte/s
ID CODA0048 - buffer rate 359522.01 Hz, data rate 0.385408 GByte/s
```

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4. Streaming Readout:

4.4 KCU1500 functional diagram

* The Data flows are in parallel

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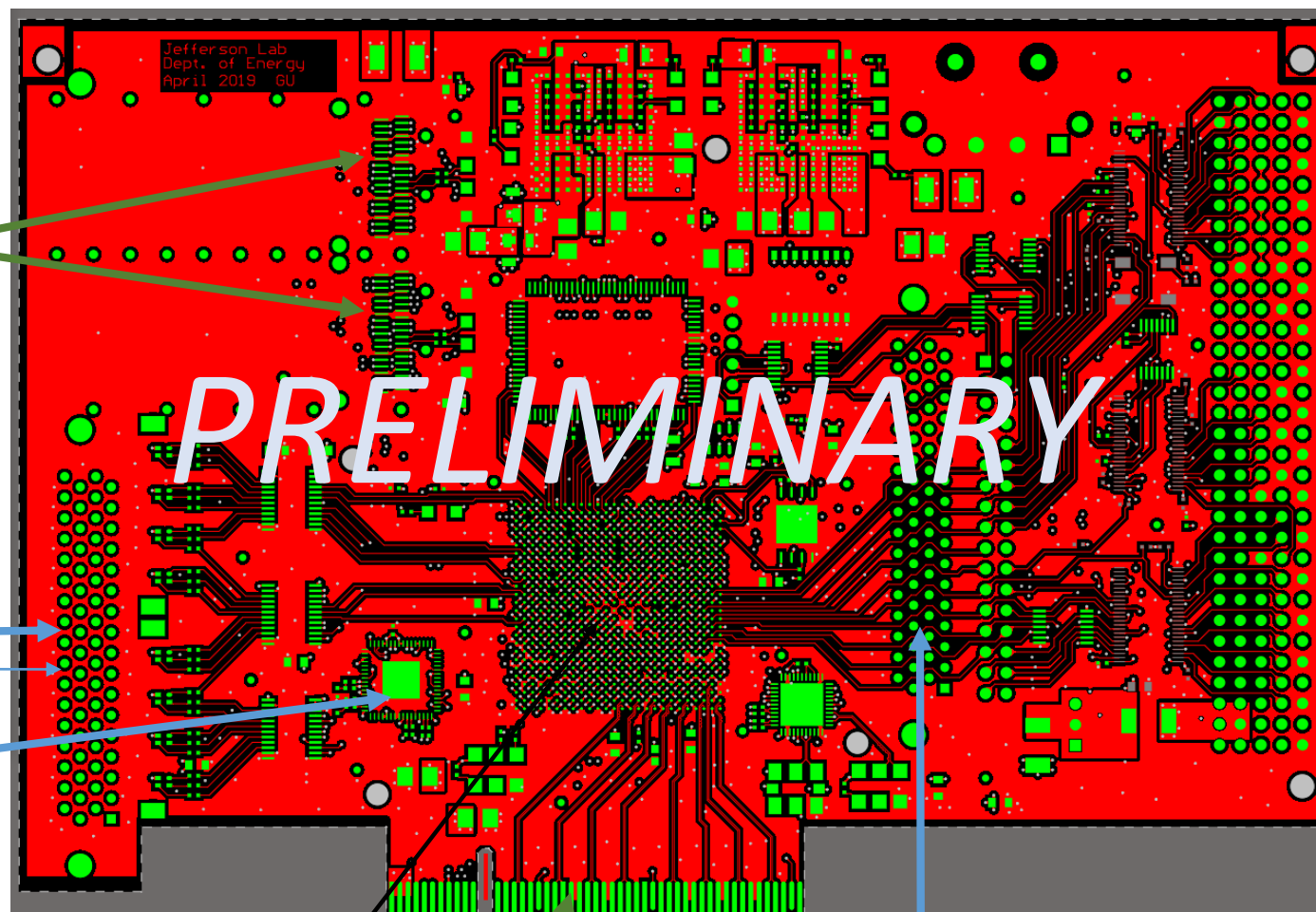Thomas Jefferson National Accelerator Facility

5. Prototype board:

5.1 STDCpcie

Two QSFPs
(2x4x10 GbE
Or 2x40 GbE
Or others)

32 LVDS inputs
+ 10MHz clock

Clock, Sync

Combining the VETROC
streaming readout TDC
and the KCU105 into one:
64-CH Streaming TDC with
standard interfaces
(PCIexpress_Gen3 and
Ethernet_10GBE)

XCKU040-2

PCIe3x8 (64 Gb/s)

32 LVDS inputs
+ SYNC

12-layer, PCIe x8 or VME (~3U)

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5. Prototyping board:

5.2 STDCpcie Status

This board will be able to test:

- Standalone 64-channel streaming TDC (~20ps) with up to eight 10 GBE interfaces;

- 64-channel TDC → PCIe Gen3 x8 interface;

- Sync/clock/Readout test of many boards (system) with the proposed fiber assignment (sec. 2.4);

- 8x MGT (1 Gbps ~ 16 Gbps) ←→ PCIe3 x8;

- 4x MGT (1 Gbps ~ 16 Gbps) ←→ 4x 10 GbE;

- Serial link beyond 10 Gbps (PCIe GEN4, 25_GBE/100_GBE) with more advanced FPGAs;

The board is ready to be manufactured: the PCB is fully routed and DRC checked; budget secured.

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6. Summary:

The CLOCK/SYNC distribution is feasible

- The dedicated clock distribution tree is better and easier, and cost manageable;

- The SYNC can be accomplished with the fiber length measurement, and delay compensation;

- We will keep an eye on the CLOCK/SYNC developments (LpGBT etc.);

The STREAMING READOUT is feasible

- A 128-ch Streaming TDC is tested;

- Some readout interfaces are tested;

Several (prototype) boards will be manufactured for CLOCK/SYNC/StreamingTDC test

Thank You

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