BDX Digitizer's Streaming Readout architecture

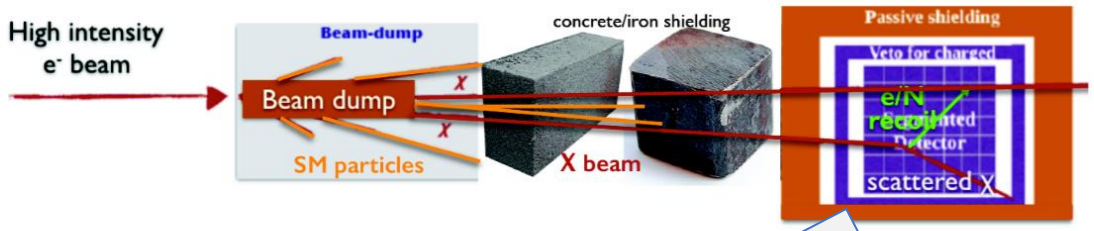
Fabrizio Ameli

INFN - ROMA

Outline

- BDX experiment requirements
- Streaming Readout DAQ
  - The Digitizer Board
    - Description
    - Characterization
  - Trigger architecture
- Conclusions
  - Trigger-less benefits

The Beam Dump eXperiment



The experiment is designed wit ls:

Producing and detecting LDM

- High-intensity e^- beam, $\simeq 10^{22}$ electrons-on-target (EOT)
- Medium-high energ
- $\simeq 1\ m^3$ (1-5
- EM-sh pability

Re ound

- shielding between beam-dump and ector to filter beam-related backgrounds (except νs)
- Passive shielding and active vetos surrounding the active volume to reduce and identify cosmogenic backgrounds
- Segmented detector for background discrimination based on event topology
- Good time resolution to perform detector-veto coincidence

Remember L. Marsicano talk

- High light yield of searched events
  - ~5 phe threshold
  - SiPM noise is under threshold
  - hit amplitude is O(100 mV)
- Hit timing properties:
  - duration: O(10 μs)
  - bandwidth: O(10 MHz)
  - rate @ 5 phe threshold: O(10 Hz)

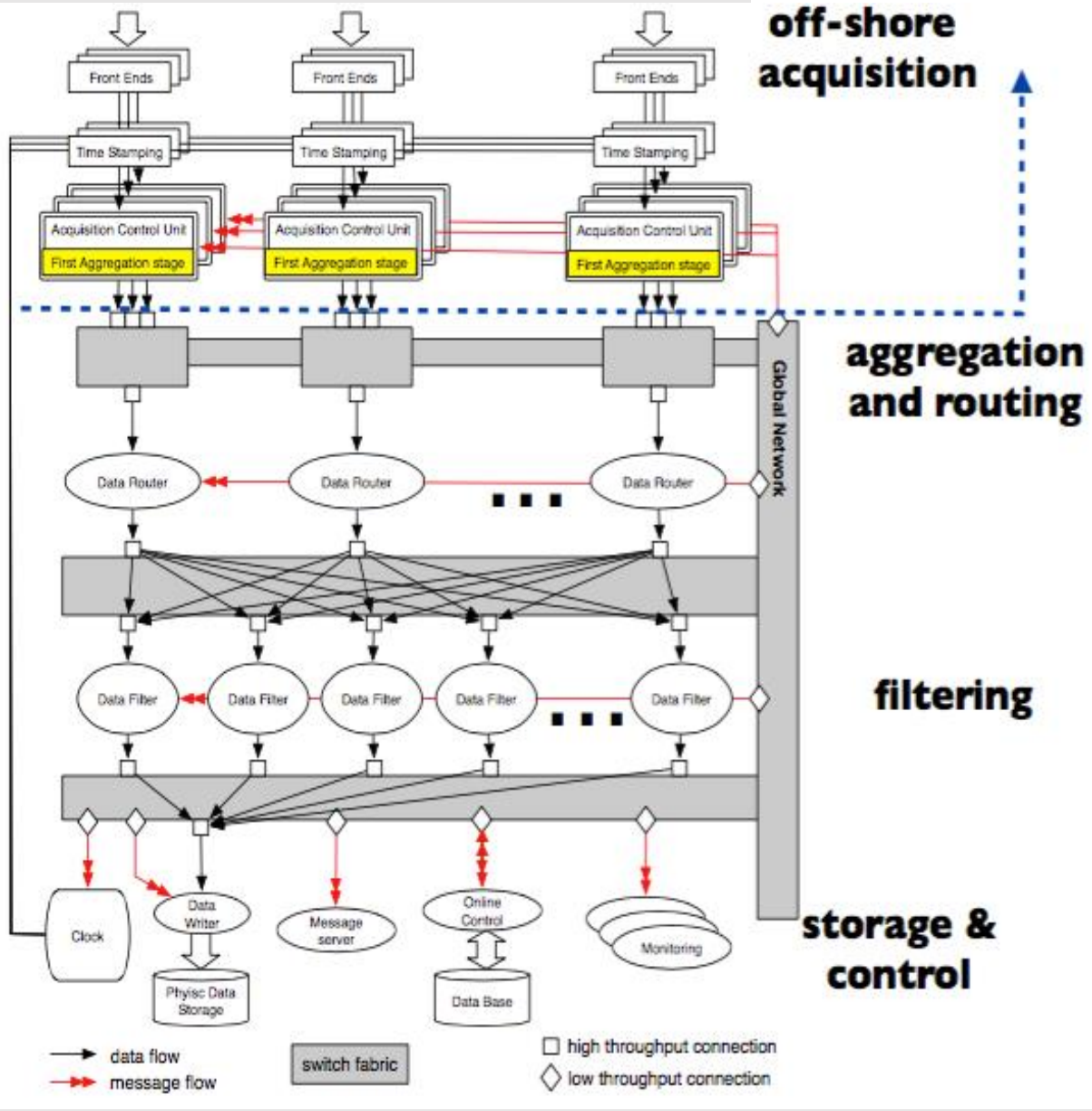
From front-end to DAQ

- DAQ architecture and front-end inherited from **KM3NeT** experiment:
  - **Trigger-less front-end** system:
    - ADC sampling (14 bit, 200MHz → 250MHz)
    - **zero-suppression** (L0 trigger) @ 0.3 p.e. threshold
    - sampling window is **time-variable**
    - all non-zero data forwarded (**all data to shore**)
  - **Trigger-less Data Acquisition System** (TriDAS)
    - **Scalable** Event Building architecture
    - DAQ scalability relies on **network** scalability

From front-end to DAQ

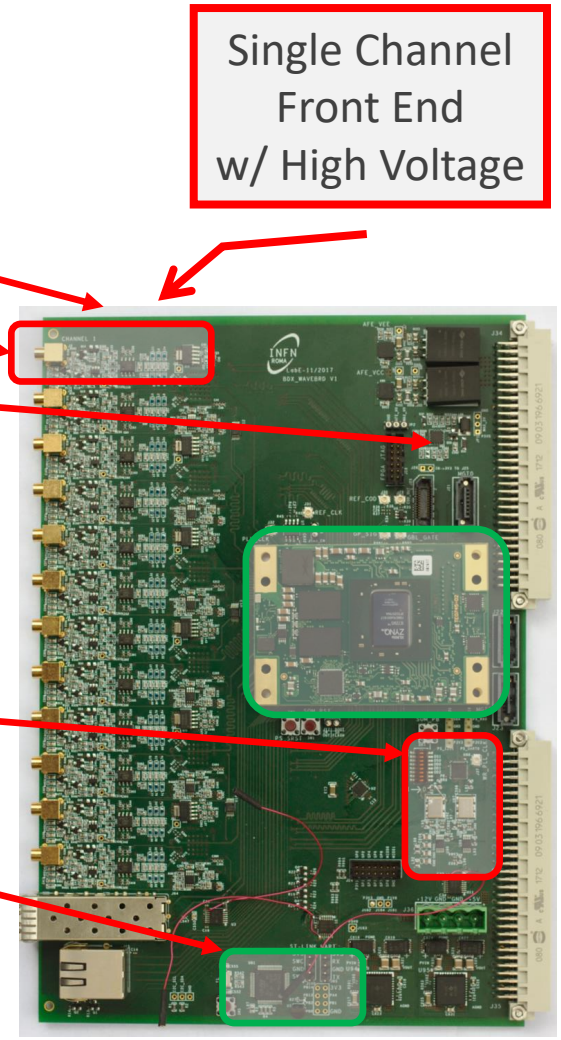
- DAQ architecture and front-en
  - **Trigger-less front-end** system:
    - ADC sampling (14 bit, 200MHz →
    - **zero-suppression** (L0 trigger) @ C
    - sampling window is **time-variable**
    - all non-zero data forwarded (**stre**
  - **Trigger-less Data Acquisition Sy**
    - **Scalable** Event Building architectu
    - DAQ scalability relies on **network**

See T. Chiarusi talk



The *WaveBoard* digitizer board

- The board is based on a Commercial-Off-The-Shelf (COTS) System On Module (SOM) mezzanine card hosting a **Zynq-7030**
- There are 12 analog front end channels
  - 6 dual-channel ultra low-power ADCs (**12/14** bit up to **250MHz**)
  - Pre-amplifier on board: **selectable gain** (either 2 or 50)
  - **HV** provided and monitored on-board
  - pedestal set by DAC
- Timing interfaces:
  - PLL to clean, generate, and distribute clocks
  - External clock and reference signals
  - White Rabbit enabled board
- ARM-M4 controls on-board peripherals (ADCs, DACs, PLL, …)
- On board peripherals:
  - High speed: GbE, SFP, USB OTG
  - Low Speed: serial, I2C, temperature monitor

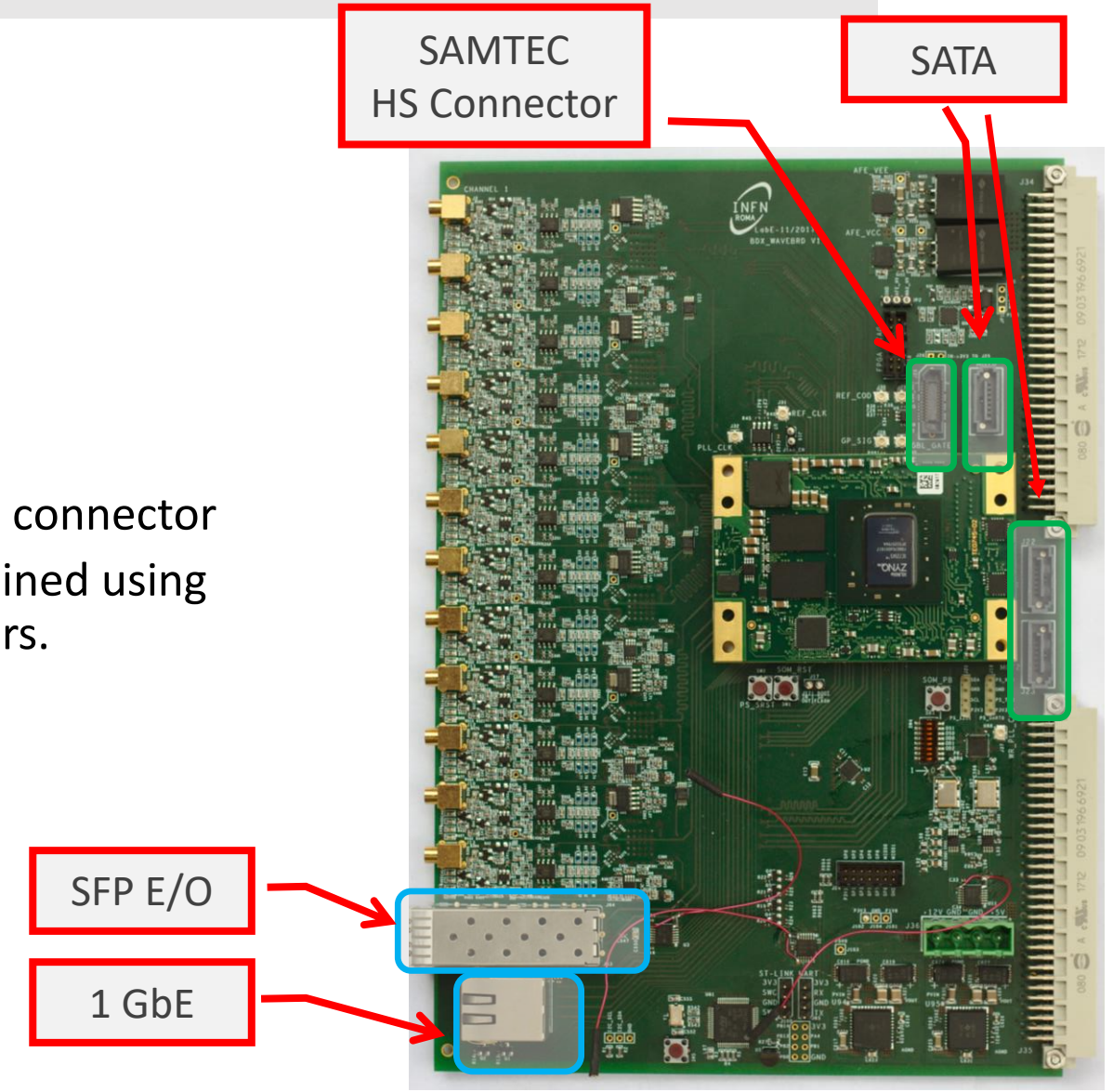


Trenz Electronics - TE0745 – Pluggable SOM

- K7-Based Zynq
- Zynq-7030/7035/7045
- DC/DC onboard
- 1GB DDR3
- 32 MB SPI Flash
- 1 Gb Ethernet PHY
- USB 2.0 PHY
- I2C, RTC, EEPROM (MAC)
- 250 I/O pins + 6 MIO
- I/O banks power from connector

Board features: Interfaces

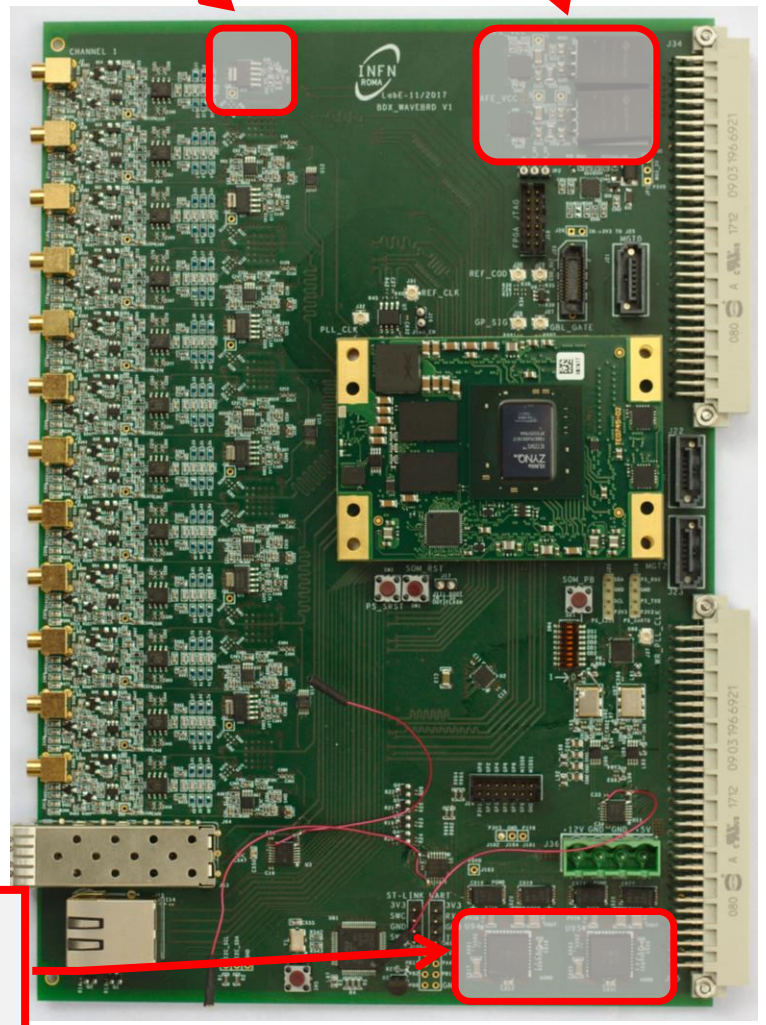
- High Speed interfaces:
  - 1 x GbE connector (PS driven)
  - 1 x SFP connector (PL driven)
  - 3 SATA connectors
  - 1 x USB On The Go
  - High Speed Samtec expansion connector
  - Boards can be easily daisy chained using FPGA MGTs on SATA connectors.
- Low speed interfaces:
  - 2 serial ports
  - 1 I2C bus
  - 1 USB
  - 1 daisy chainable temperature sensor



Board features: Power

- Linear regulators dedicated to analog front-end supplies (+5V and -5V)
- Dedicated 1.8V linear regulator per FastADC
- VME connectors only for power and mechanical support
- SiPM High Voltage up to 90V provided on-board
- Power consumption:
  - 2.3A @5V
  - 0.5A @ 12V

Total power ~17.5 W



Board Cost

- Board cost is adjustable according to project requirements:
  - Use the right ADC: price ranges from 9 to 65 €/channel
  - Choose the right SOM: 500€ to 780€

Total cost ranges from 1.3k€ to 2.1k€ per board

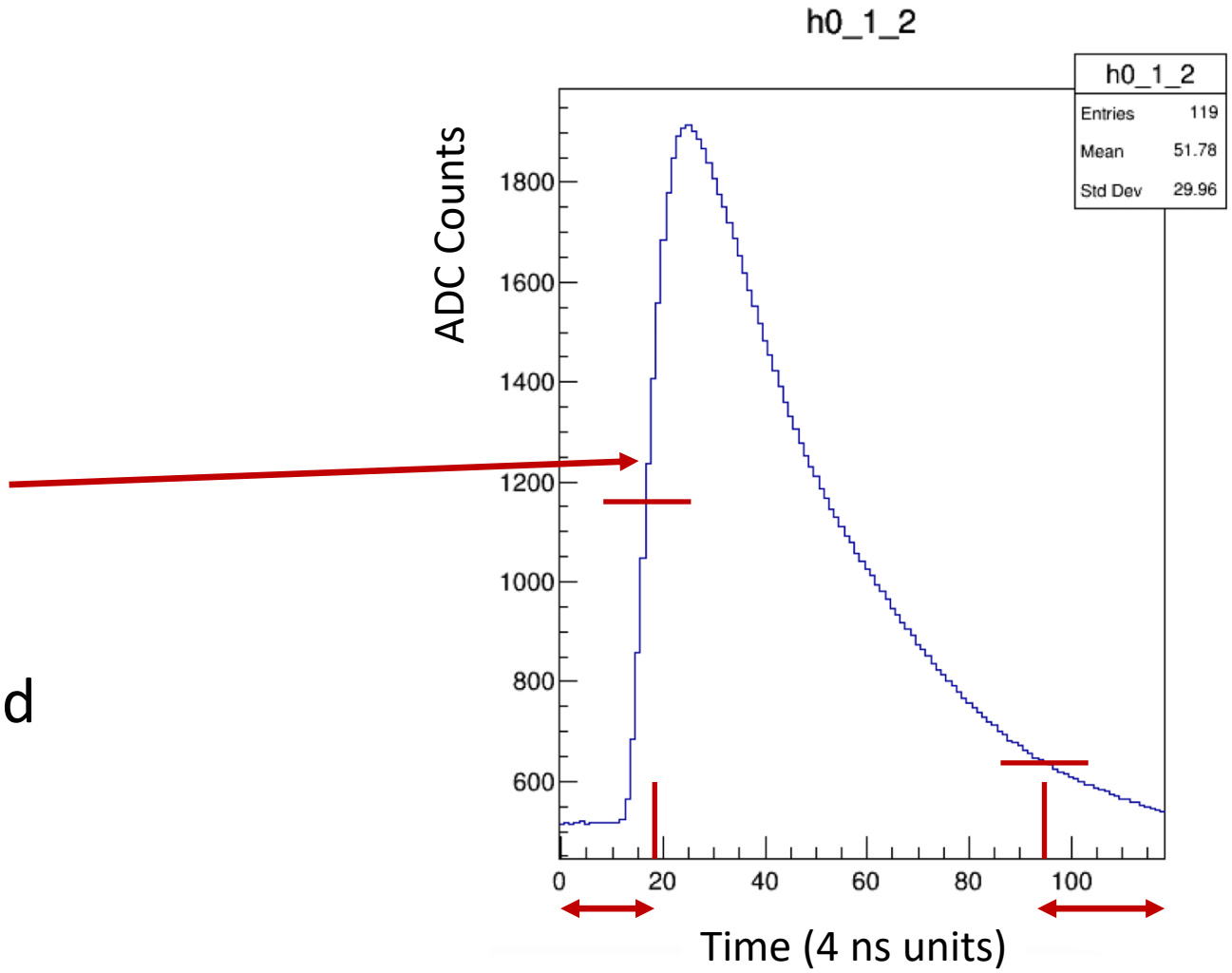
Digitization example: BDX crystal read by SiPM

DAQ Setup Procedure

- Set over and under thresholds
- Set Leading samples number
- Set Trailing samples number

Acquisition Process

- Time stamp is set on first over threshold sample
- A packet with channel ID, charge, time stamp and samples is pushed through Ethernet interface
- Dead time happens when output link speed is too low wrt hit rate

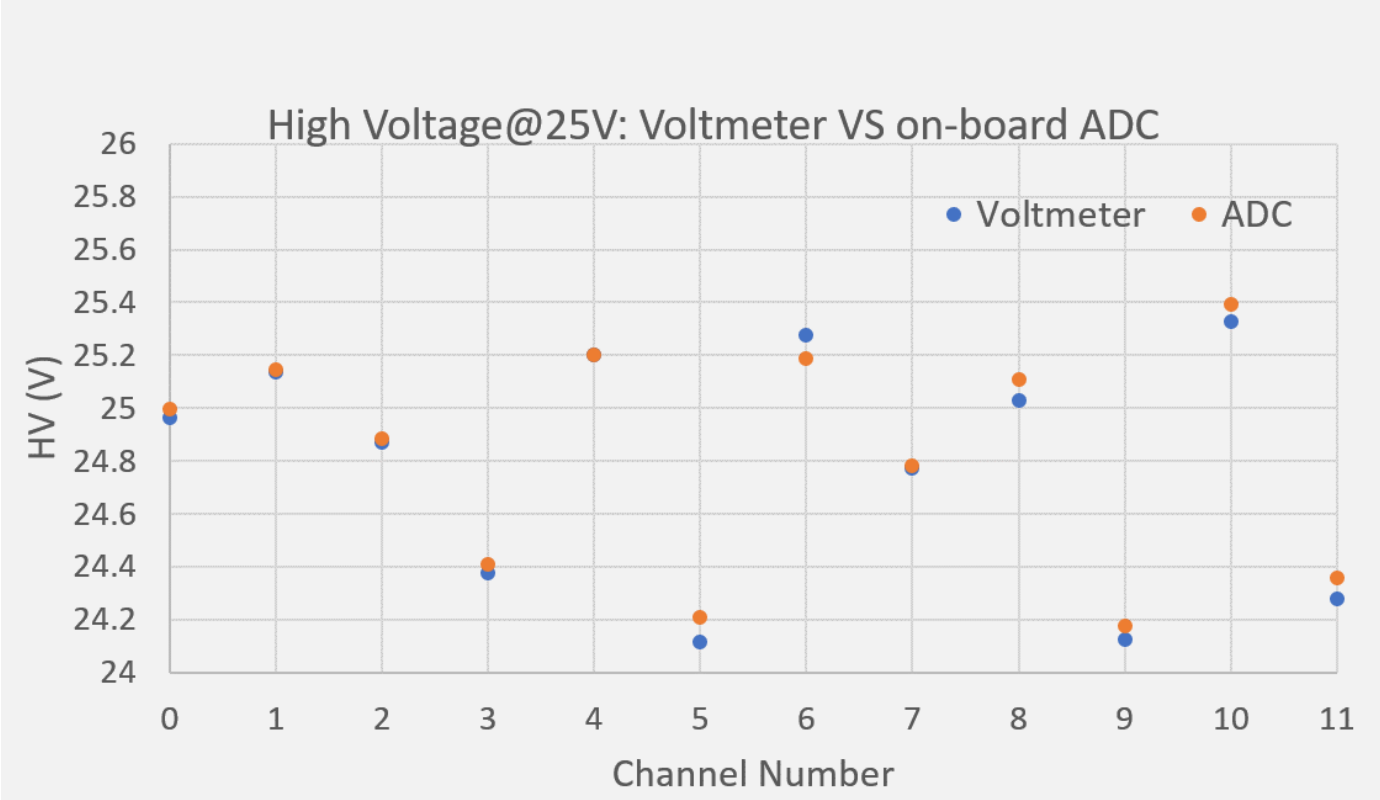


High Voltage set and measurement

- The board can provide High Voltage to power sensors (typically SiPM)
  - HV is AC-coupled to sensor signal
  - up to 90V on-board generation
  - HV is linearly regulated (accepted input up to 100V)
  - Range is from 25 to 75V, DAC selectable
- Changing HW configuration, the same circuit can control a HV generator (e.g. PMT HV base can be set by a control voltage ranging from 0 to 2V)

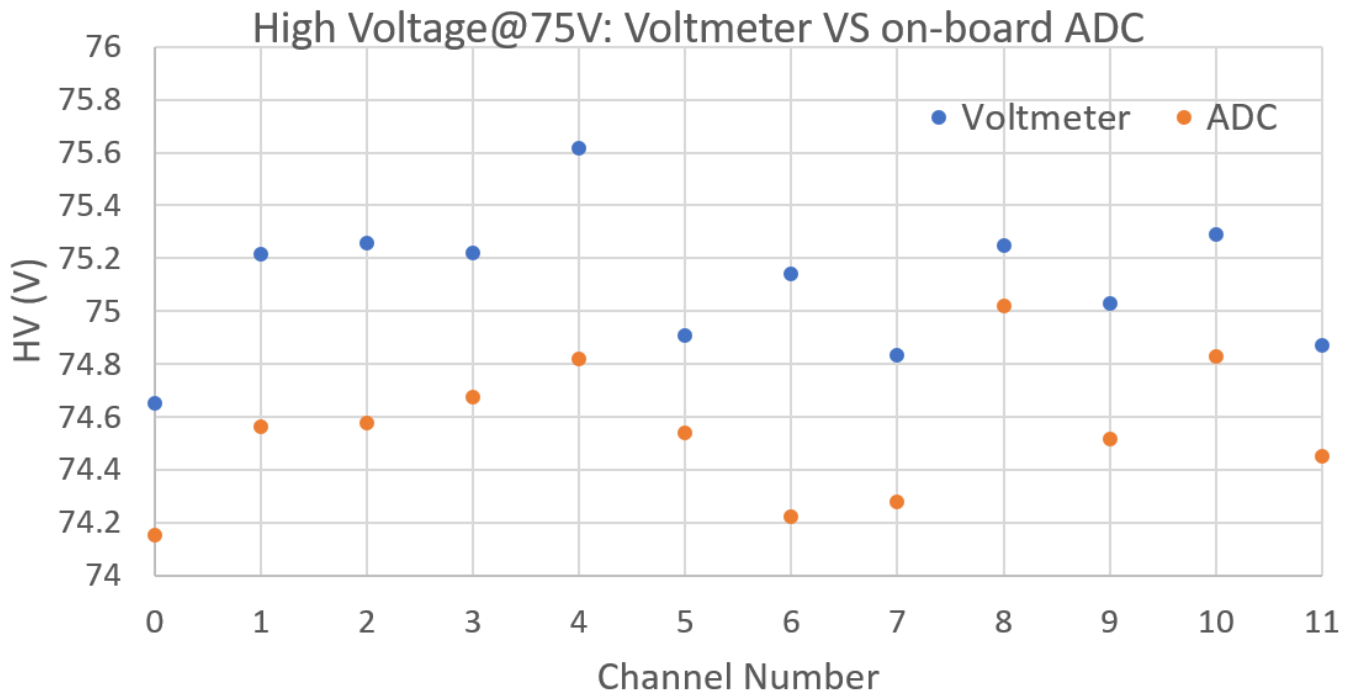
High Voltage set and measurement

- High Voltage set to 25V:
  - Values read by Voltmeter and on-board ADC
  - Channel average error: 0.2%



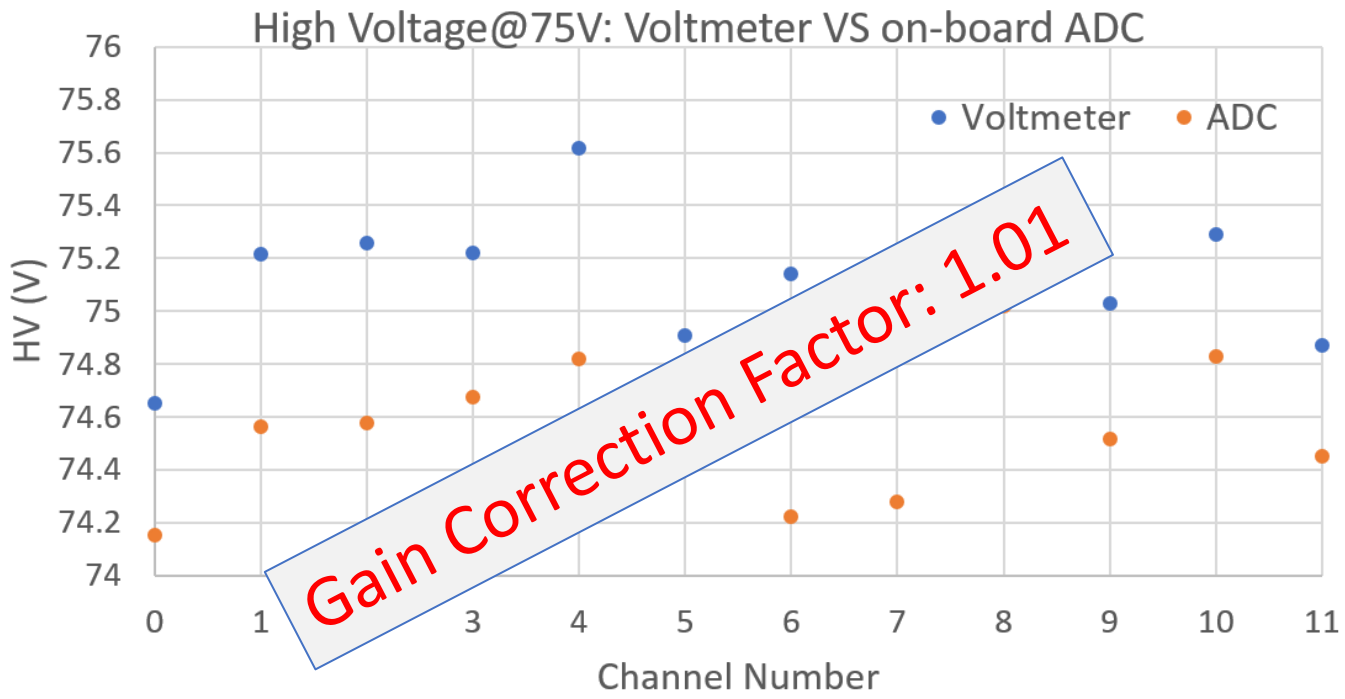
High Voltage set and measurement

- High Voltage set to 75V:
  - Values read by Voltmeter and on-board ADC
  - Channel average error: 0.7%



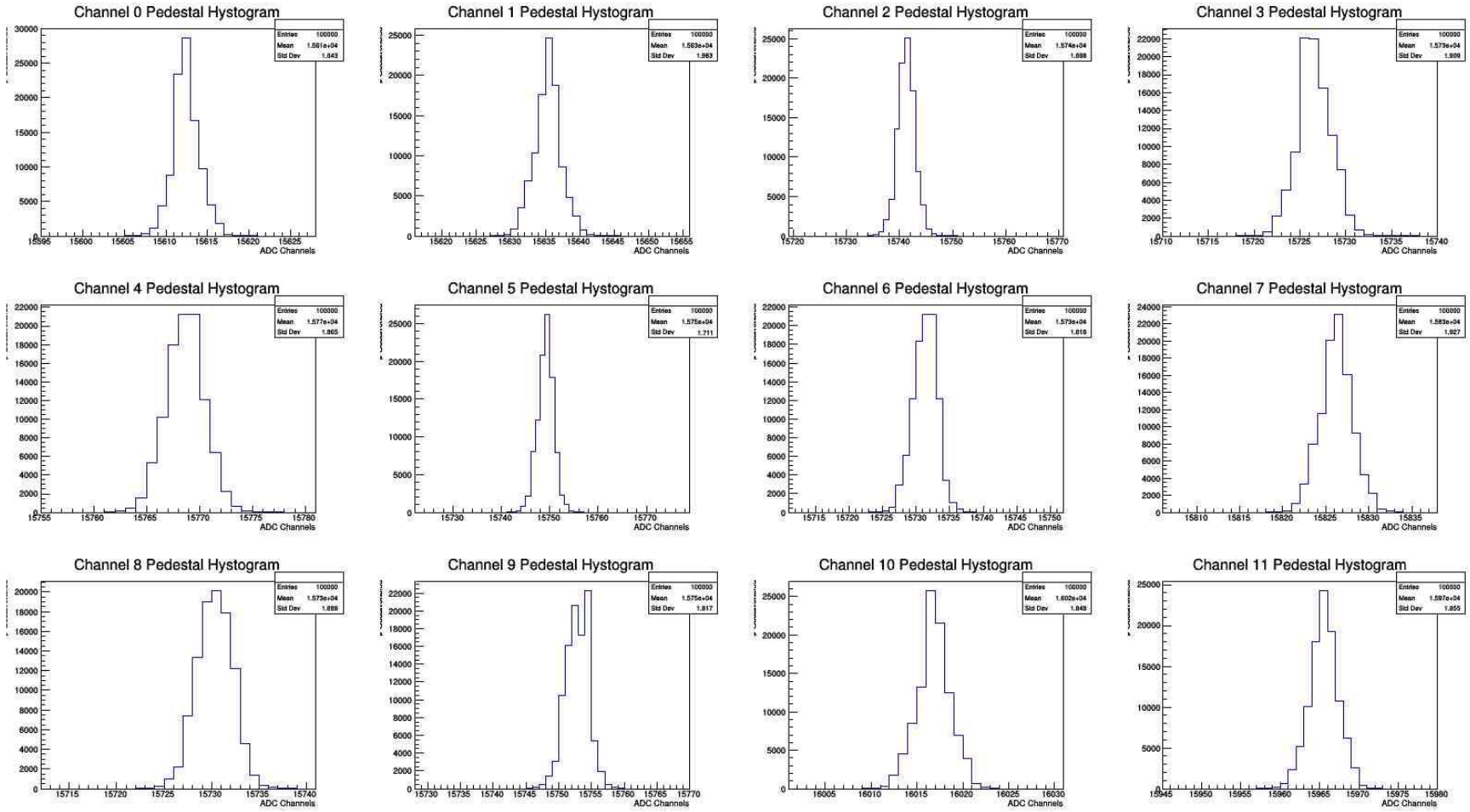
High Voltage set and measurement

- High Voltage set to 75V:
  - Values read by Voltmeter and on-board ADC
  - Channel average error: 0.7%



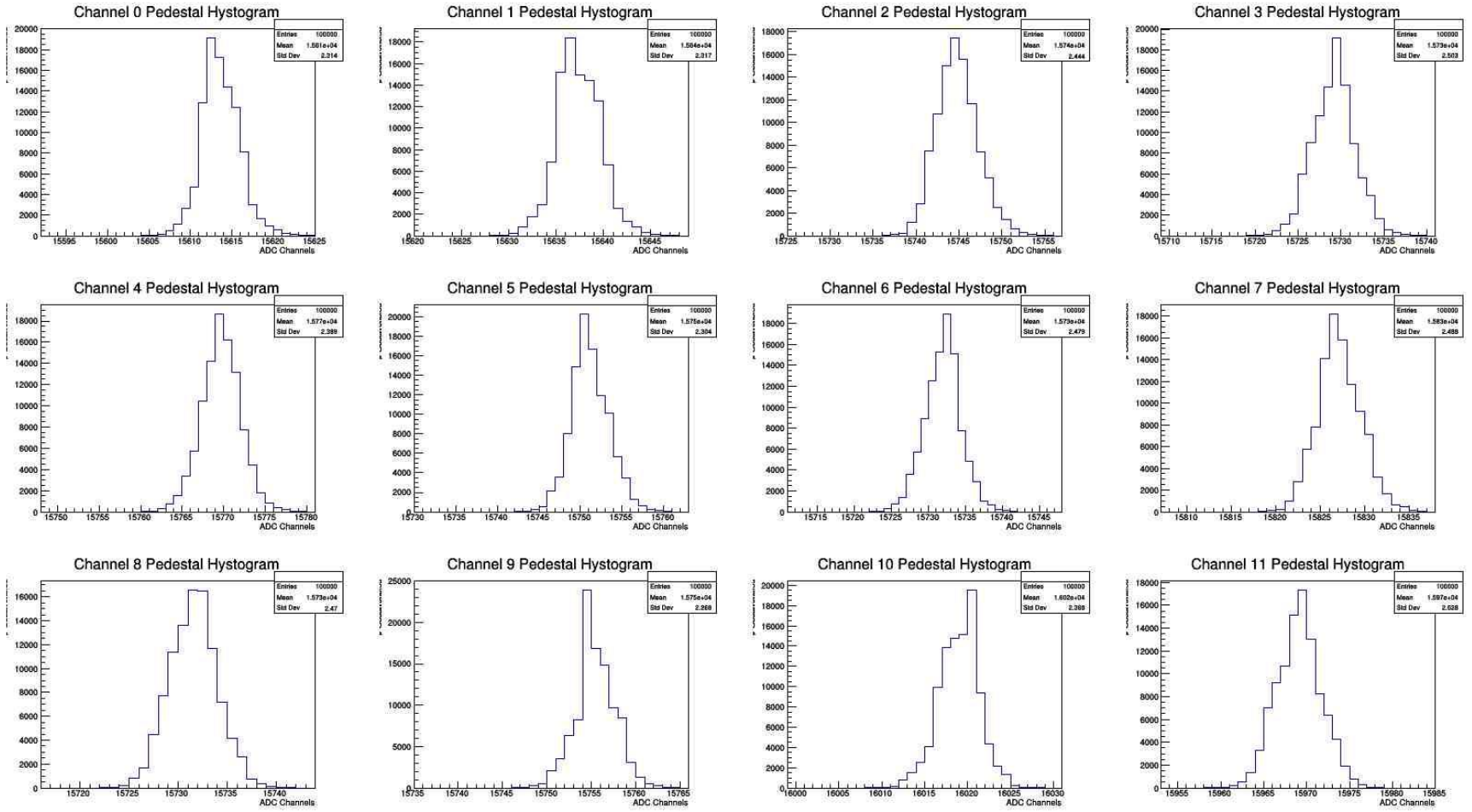
Pedestal estimation and Noise

- Channel Pedestal estimate: 1.6-1.9 ADC count (rms)
  - Calculated on 10^5 samples
  - Input is Open
  - **No HV generated**



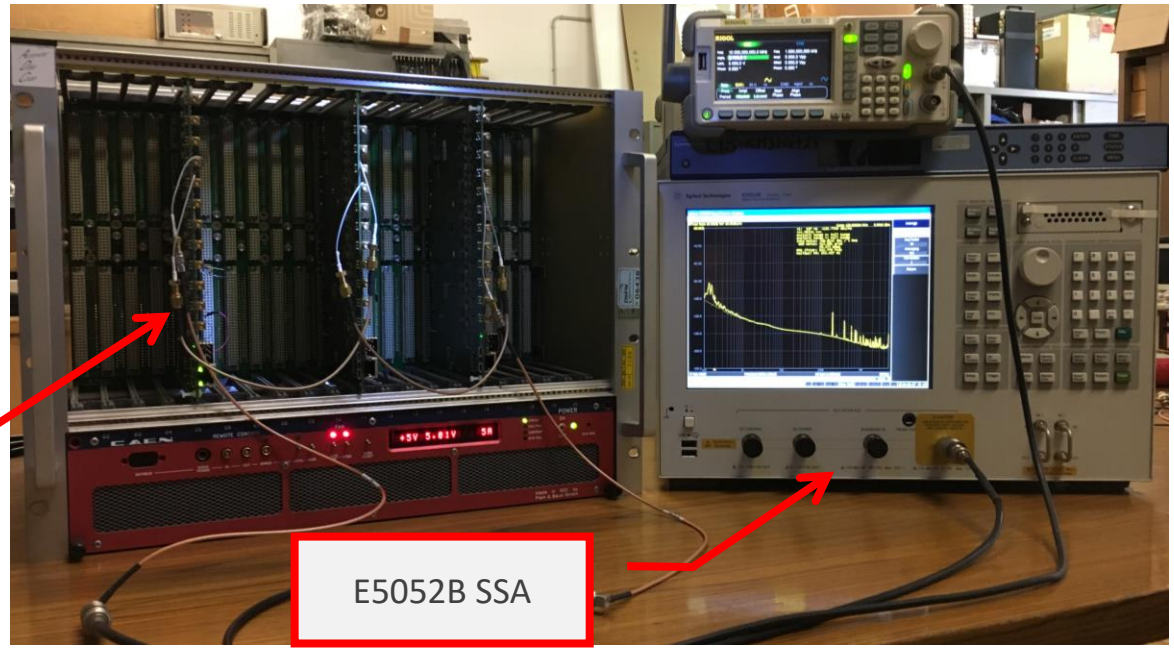
Pedestal estimation and Noise

- Channel Pedestal estimate: 2.2-2.6 ADC count (rms)
  - Calculated on 10^5 samples
  - Input is Open
  - **HV generated**



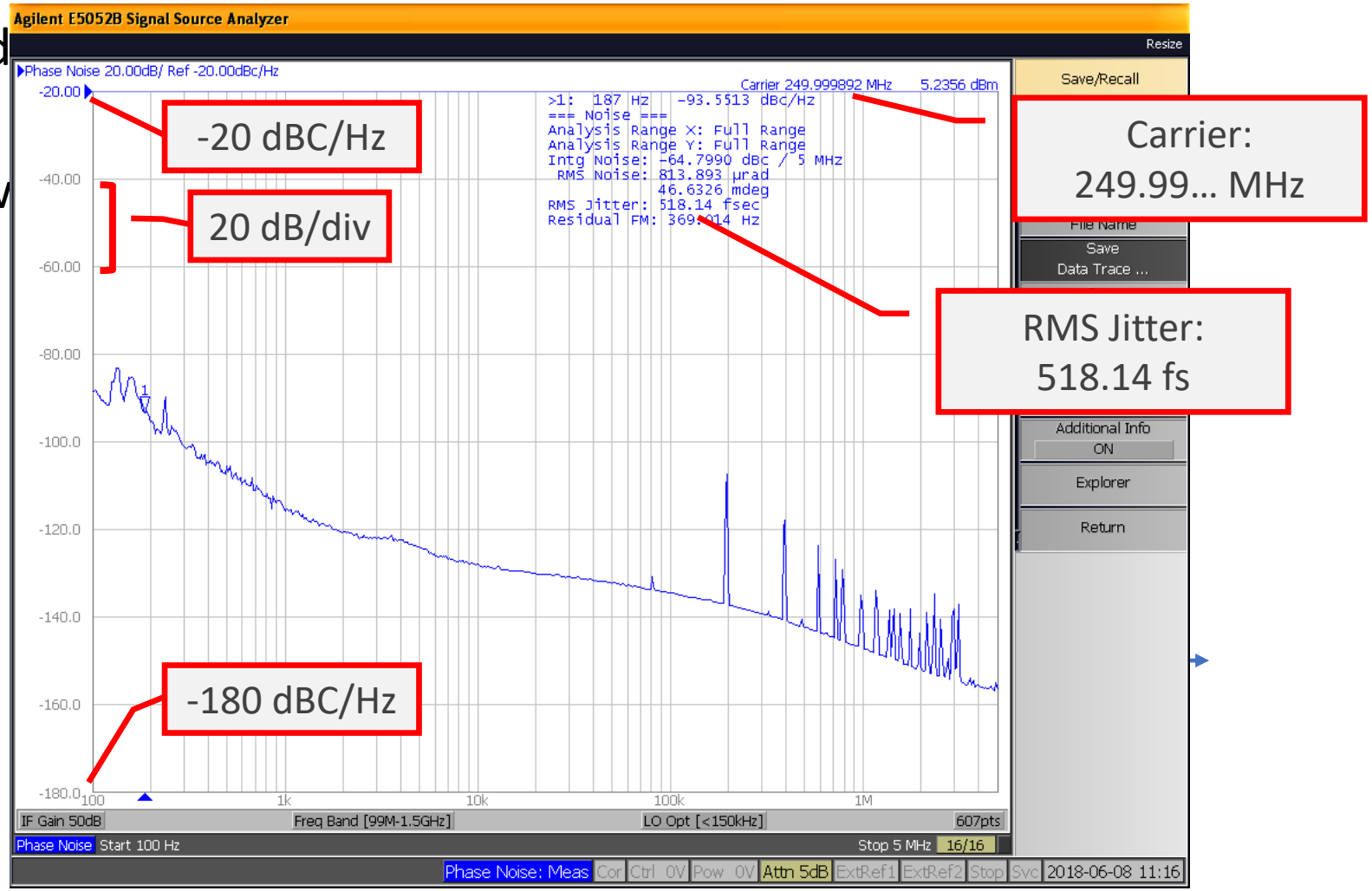
Timing test bench setup: clock quality

- Input clock from generator: 10 MHz
- Input clock is jitter-cleaned and multiplied by a factor 25 by on-board PLL
- Jitter performance measured with E5052B-Signal Source Analyzer



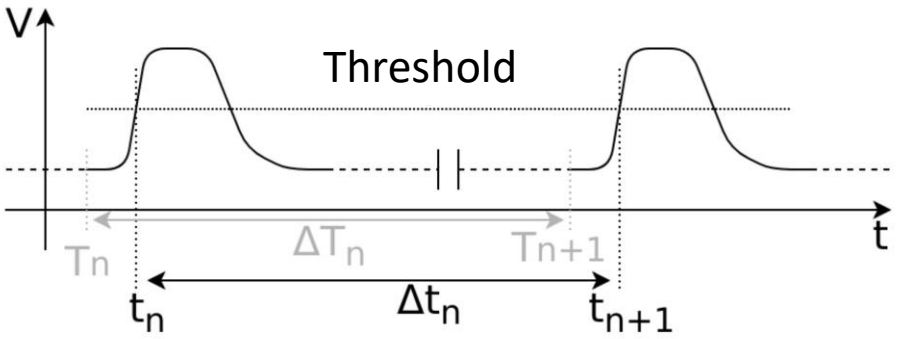
Timing test bench setup: clock quality

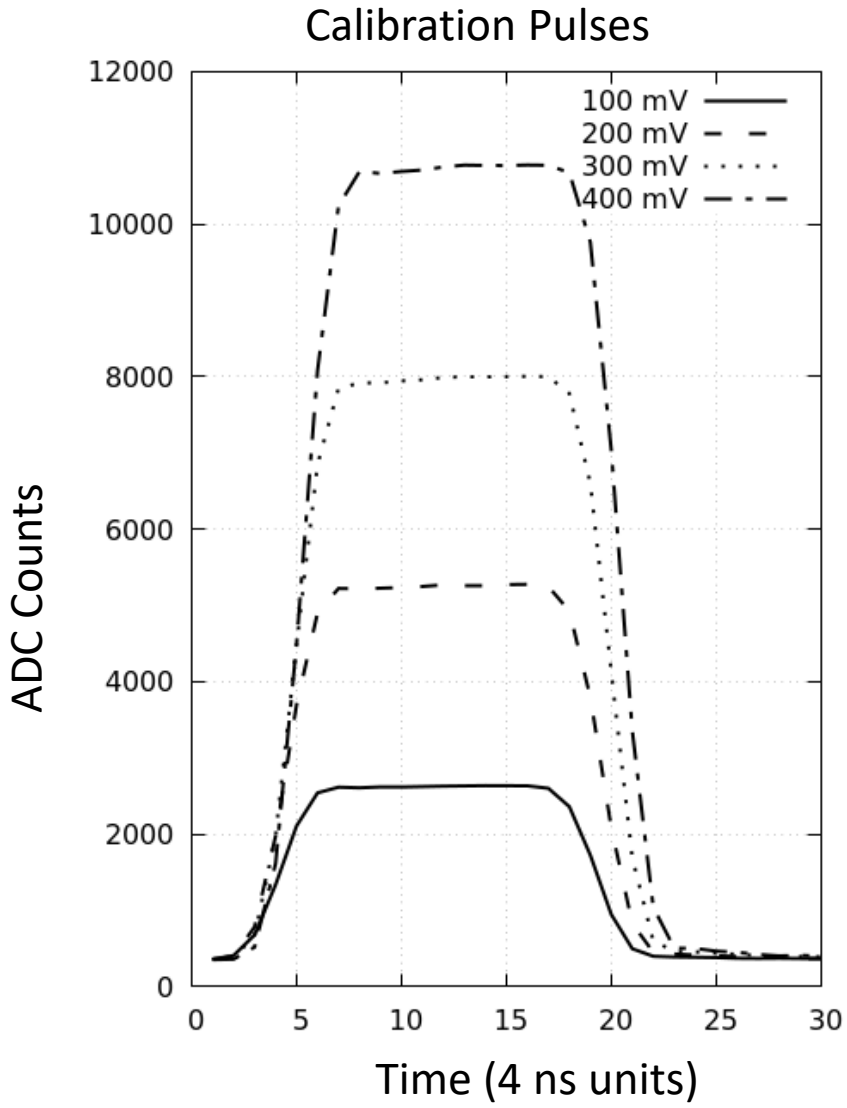
- Input clock from generator: 10 MHz
- Input clock is jitter-cleaned and
  by a factor 25 by on-board PLL
- Jitter performance measured w
  E5052B-Signal Source Analyzer



Timing test bench setup: resolution

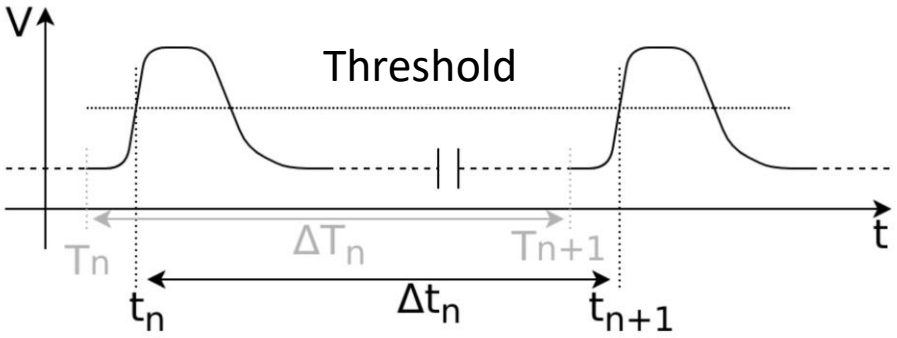
- Input is driven by a pulse generator (DTG5334)
  - Pulses period: 50 kHz
- Histogram of time differences between consecutive pulses
  - Linear interpolation of waveforms
  - The higher the amplitude, the better
  - Spline interpolation enhances resolution

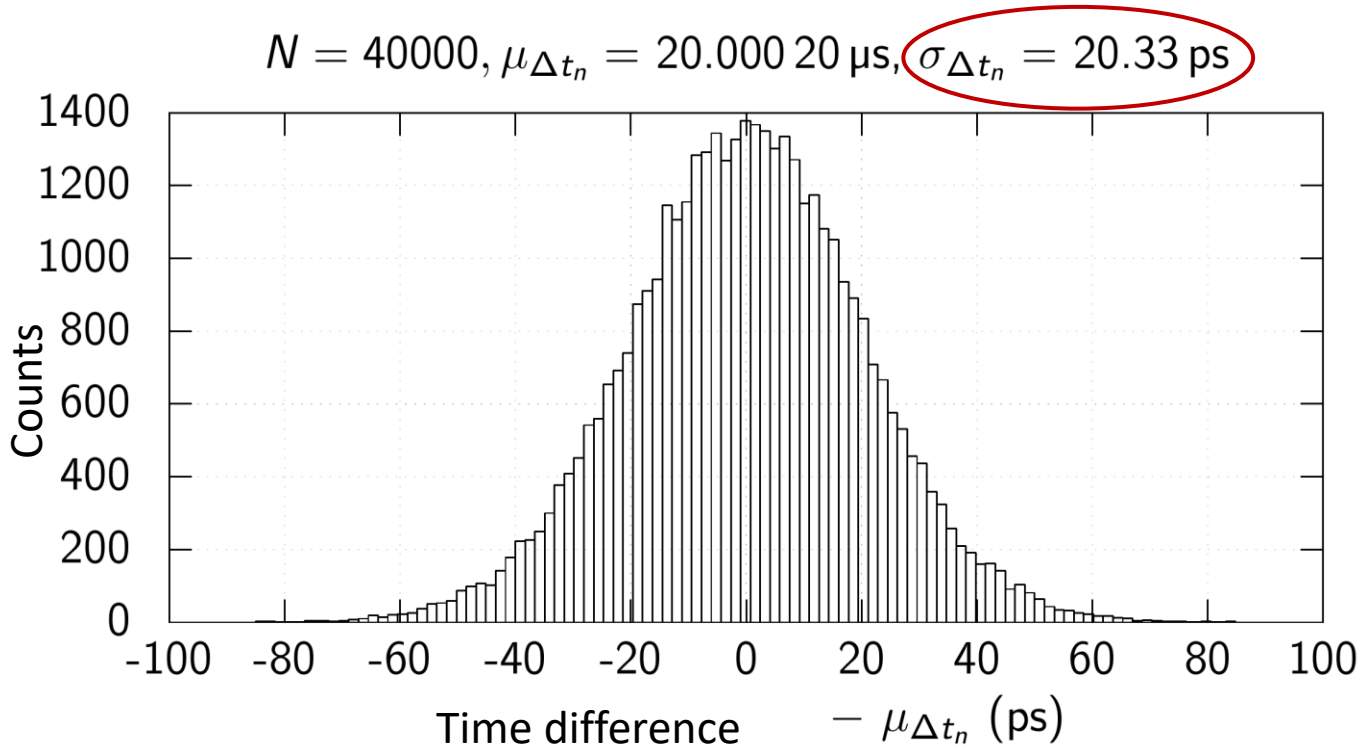




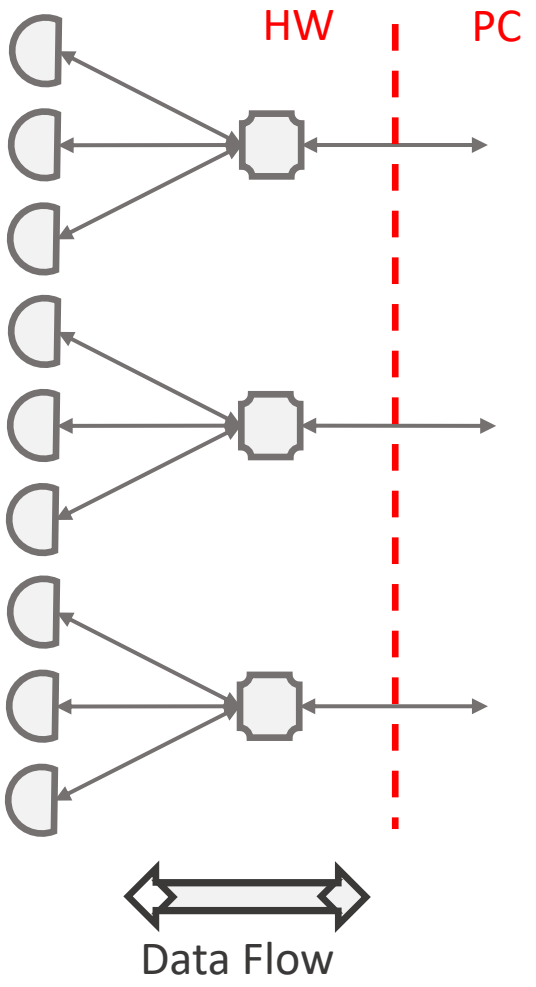
Timing test bench setup: resolution

- Input is driven by a pulse generator (DTG5334)
  - Pulses period: 50 kHz
- Histogram of time differences between consecutive pulses
  - Linear interpolation of waveforms
  - The higher the amplitude, the better
  - Spline interpolation enhances resolution



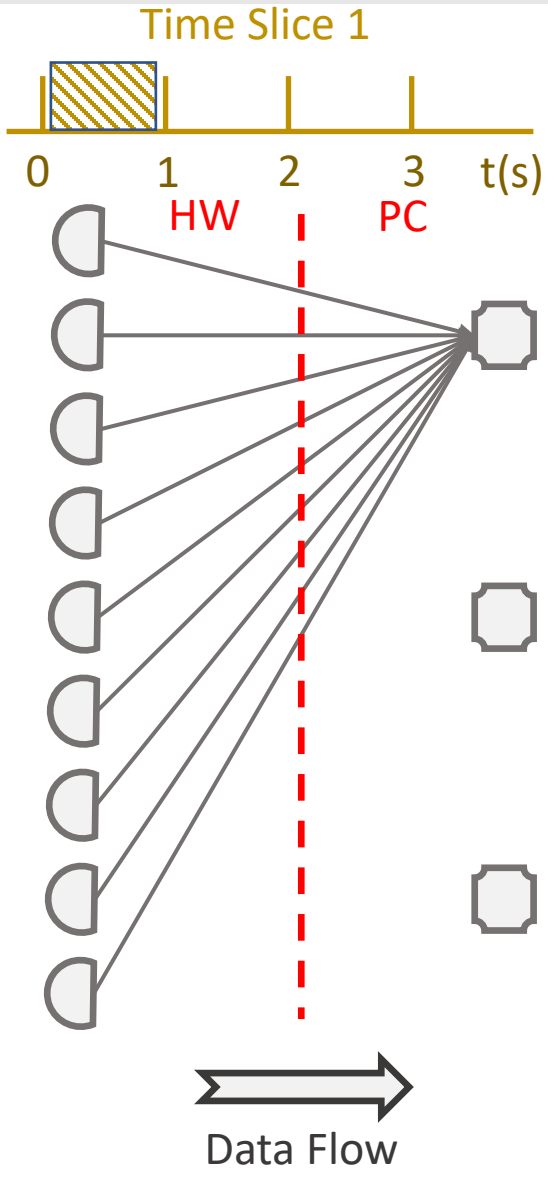


Triggered architecture



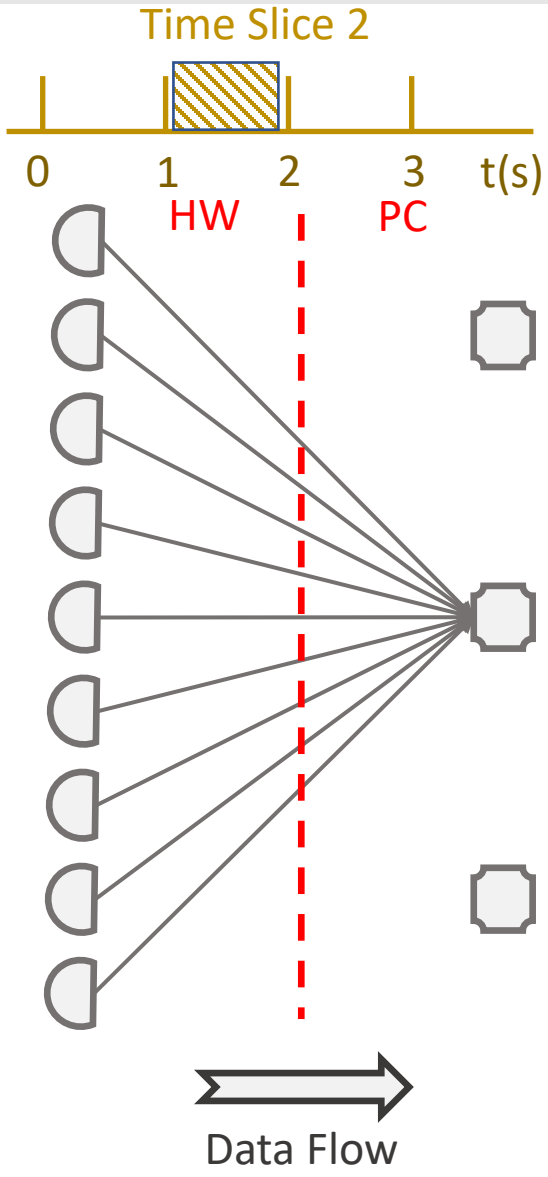
- **HW Trigger**:
  - Signal feature extraction
  - Stream **few** data forward
  - If level2 triggers: send all data forward
- **Buffering**:
  - Enough to cope with trigger latency
- **Detector sectioning**:
  - Needed to implement local triggers
- **Event Selection**:
  - Higher trigger levels

Streaming Readout architecture



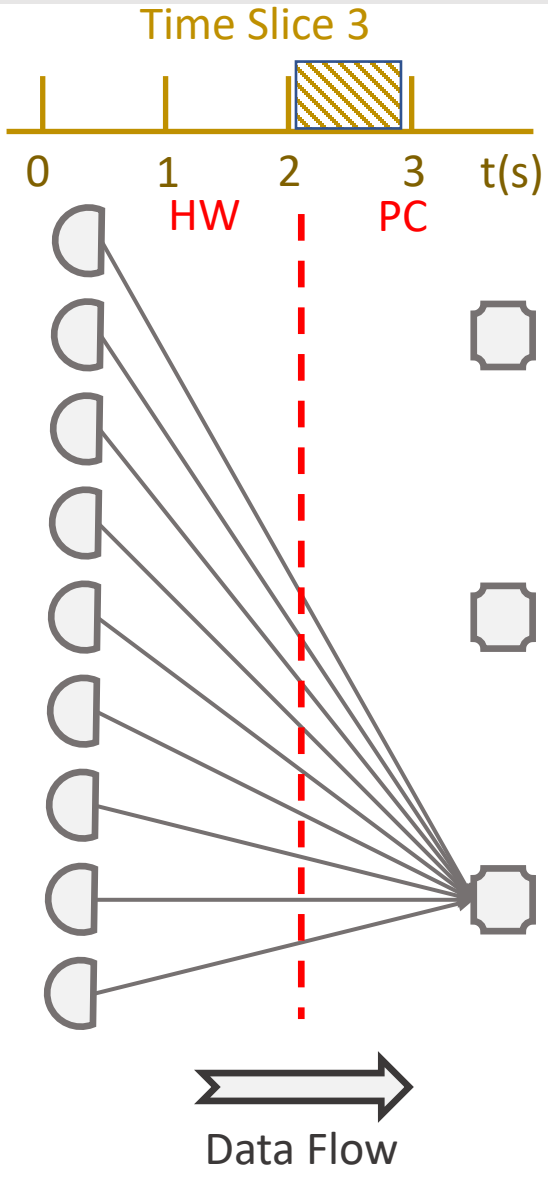
- **HW DAQ**:
  - L0 trigger (Zero Skipping)
  - Stream **all** data forward
- **Buffering**:
  - Enough to cope with transmission link
- **Detector sectioning**:
  - Not needed
- **Event Selection**:
  - Time is divided into time slices
  - Hits in the same time slice are forwarded to same trigger PC

Streaming Readout architecture



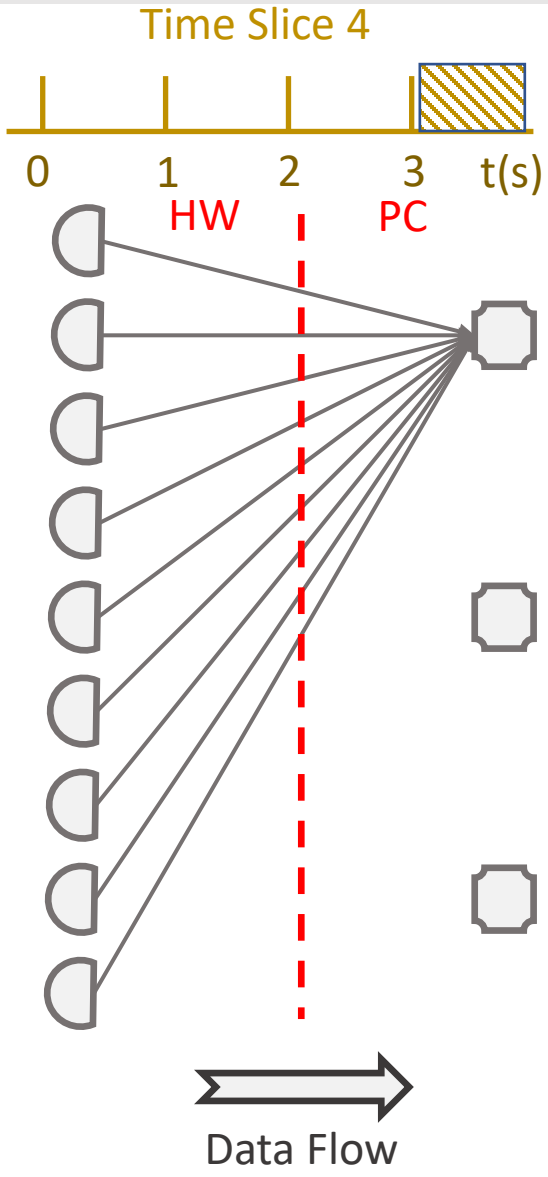
- **HW DAQ**:
  - L0 trigger (Zero Skipping)
  - Stream **all** data forward
- **Buffering**:
  - Enough to cope with transmission link
- **Detector sectioning**:
  - Not needed
- **Event Selection**:
  - Time is divided into time slices
  - Hits in the same time slice are forwarded to same trigger PC

Streaming Readout architecture



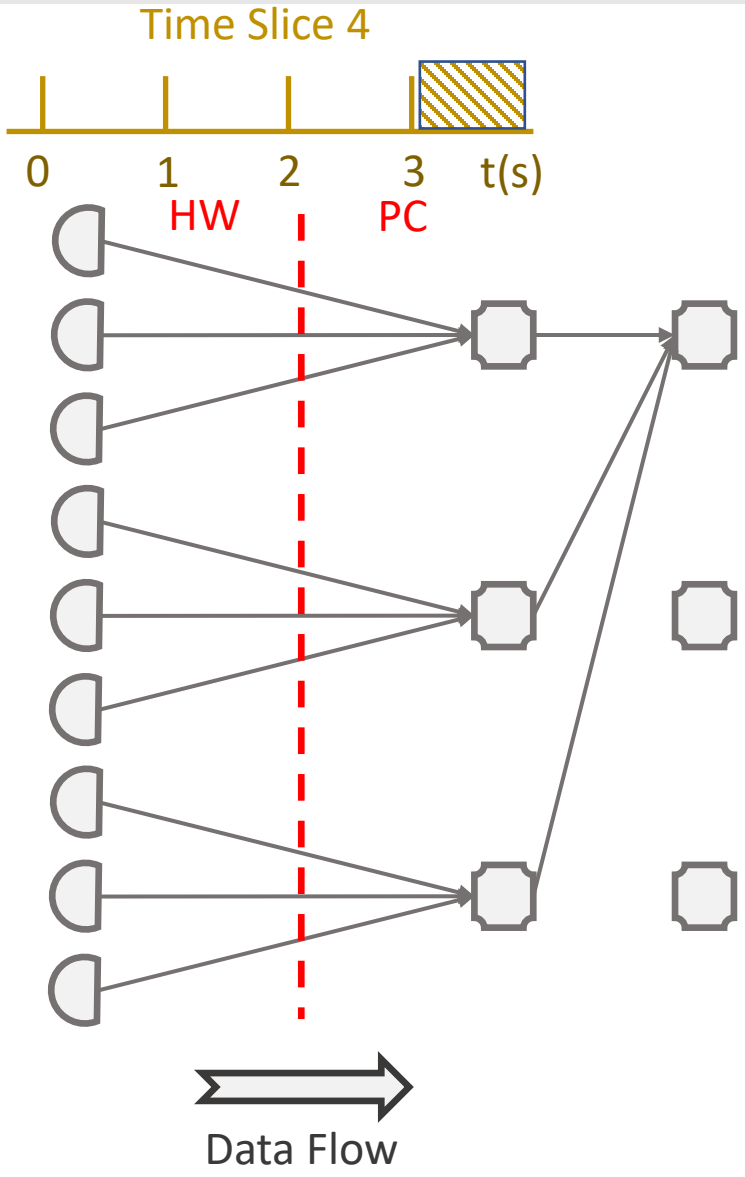
- **HW DAQ**:
  - L0 trigger (Zero Skipping)
  - Stream **all** data forward
- **Buffering**:
  - Enough to cope with transmission link
- **Detector sectioning**:
  - Not needed
- **Event Selection**:
  - Time is divided into time slices
  - Hits in the same time slice are forwarded to same trigger PC

Streaming Readout architecture



- **HW DAQ**:
  - L0 trigger (Zero Skipping)
  - Stream **all** data forward
- **Buffering**:
  - Enough to cope with transmission link
- **Detector sectioning**:
  - Not needed
- **Event Selection**:
  - Time is divided into time slices
  - Hits in the same time slice are forwarded to same trigger PC

Streaming Readout architecture



- **HW DAQ**:
  - L0 trigger (Zero Skipping)
  - Stream **all** data forward
- **Buffering**:
  - Enough to cope with transmission link
- **Detector sectioning**:
  - Not needed
- **Event Selection**:
  - Time is divided into time slices
  - Hits in the same time slice are forwarded to same trigger PC

Streaming readout: cons

- Less efficient in terms of total data rates
  - HW could be more demanding
- In some cases, data rates are so high that pushing all data is not feasible
- If L0 discards data (ie hit is under threshold), data are lost!
  - If triggered systems apply L0, both approaches are equivalent

Streaming readout: HW benefits

- Flat Front End nodes hierarchy
  - FE nodes are **independent** from each other
  - Same **minimal HW programming** required for all nodes (no trigger, no feature extraction, no strict latency)
  - **Unidirectional** data flow
- Changing trigger doesn't change HW
- Connecting network should be based on commercial protocols/HW:
  - Ethernet network: low cost, wide availability, FPGA IP core support
  - Ethernet switches can be used as data concentrator

Streaming readout: DAQ benefits

- Trigger algorithm complexity moves into SW domain
- Trigger algorithms can be applied to the whole detector
- The architecture is scalable as long as the network is:
  - If trigger algorithm gets more and more complex, just add PCs
  - If FE rate gets higher (eg using lower thresholds), just add PCs
  - If FE nodes grow, just add more PCs

Farnesina
Ministero degli Affari Esteri
e della Cooperazione Internazionale

INFN

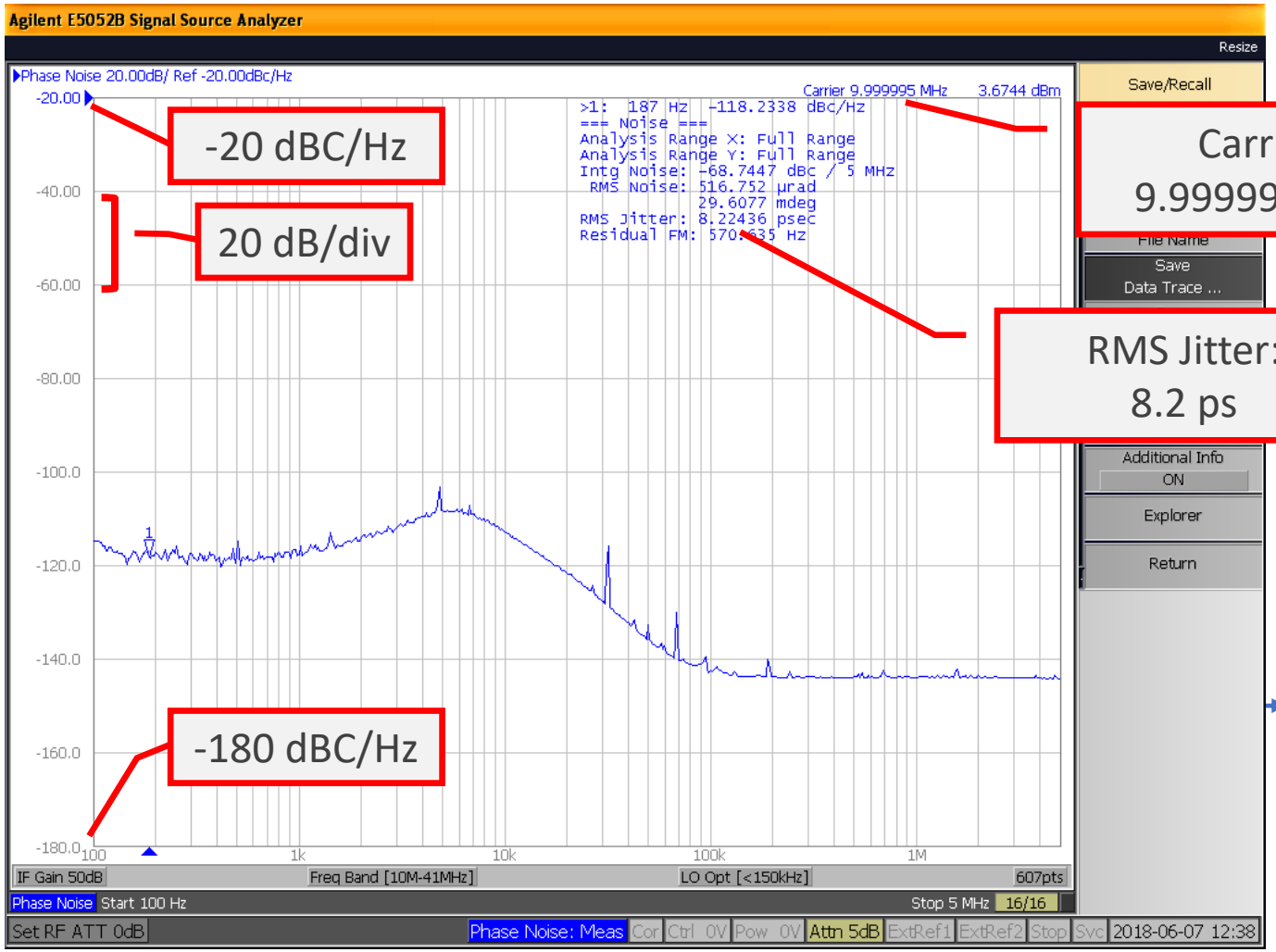
Thank you

BDX status

- **Beam Dump eXperiment** at JLab:
  search for Dark sector particles
  in the 1 ÷ 1000 MeV mass range.
  - High intensity ($\simeq 10^{22}$ EOT/year), high energy (11GeV) e- beam
  - Detector: ~800 CsI(Tl) calorimeter + 2-layers active veto + shielding.
    Reuse BaBar crystals with improved SiPM readout.
- BDX can be ready to run within ~2 years
- Current experiment status:
  - Full proposal submitted to JLab PAC 44: **conditionally approved**
  - After PAC45 update, on-site background measurements and detector optimization studies
  - Presented update to PAC46 for approval

Timing: test bench setup

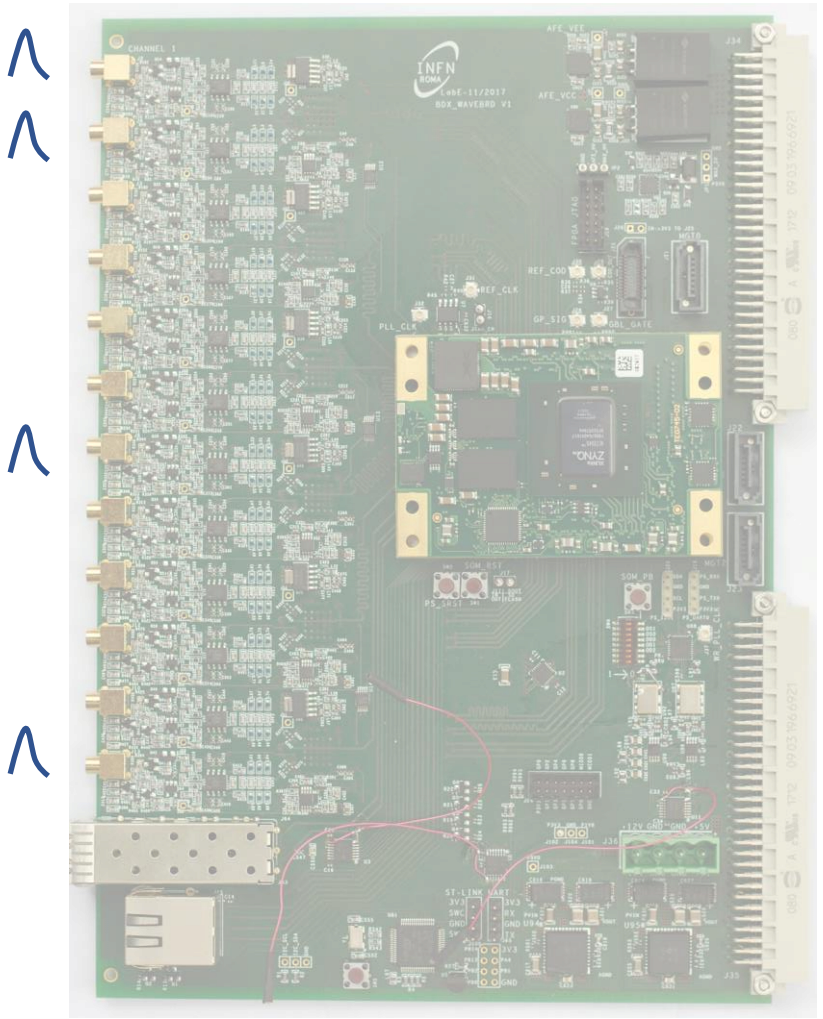
- Ref 10 MHz clock path:
  Generator Clock JItter

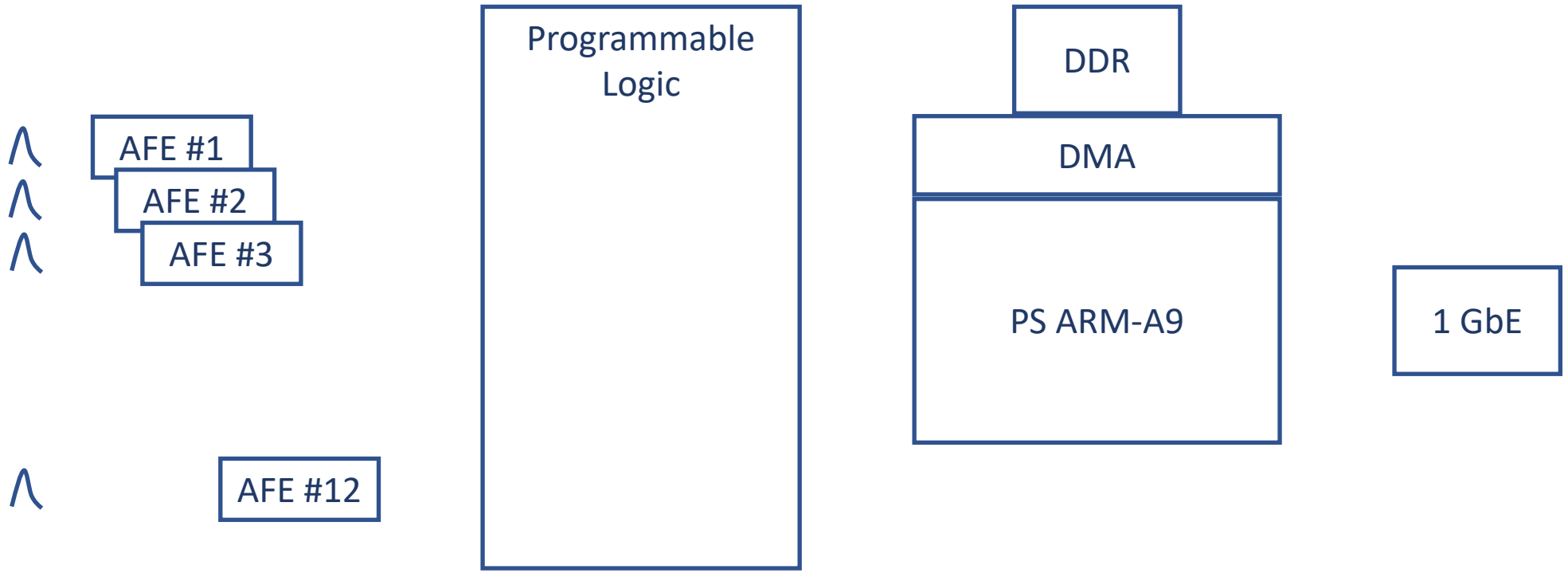


Board features: Power

- Linear regulators dedicated to analog front-end supplies (+5V and -5V)
- Dedicated 1.8V linear regulator per FastADC
- VME connectors only for power and mechanical support
- SiPM High Voltage up to 90V provided on-board
- Power consumption:
  - 2.3A @5V
  - 0.5A @ 12V

Total power ~17.5 W




AFE #1
AFE #2
AFE #3
AFE #12
Programmable Logic
DDR
DMA
PS ARM-A9
1 GbE