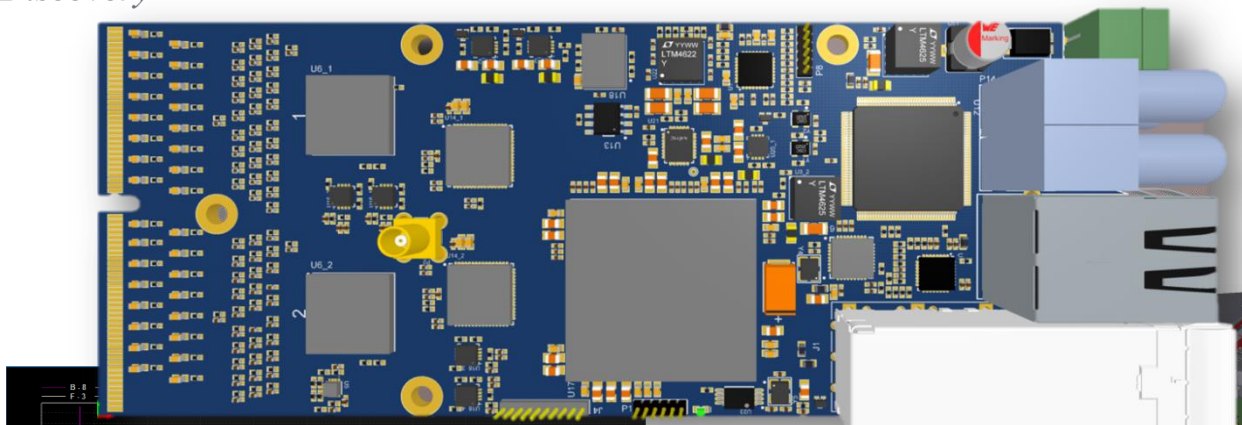
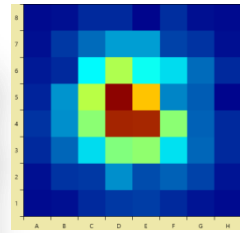
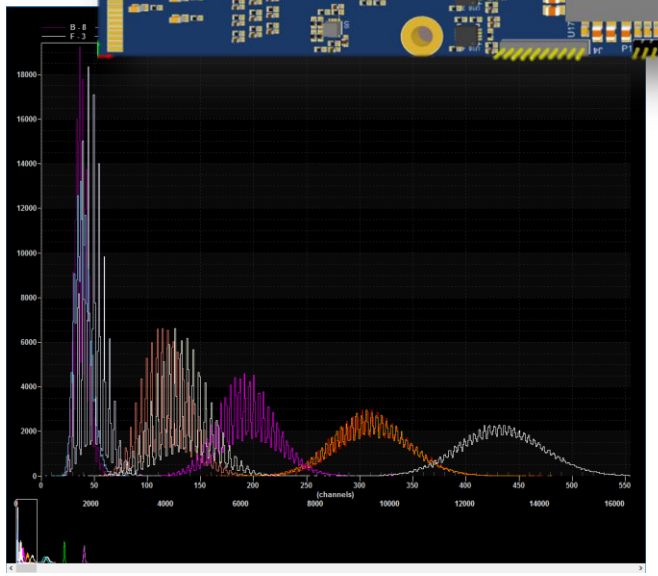
CAEN Electronic Instrumentation

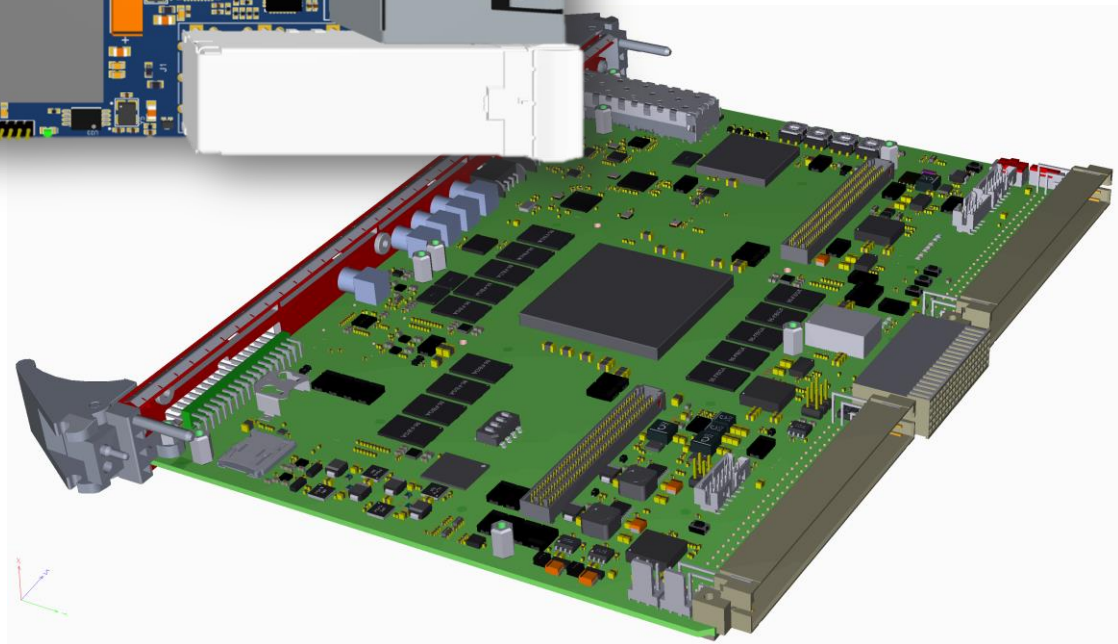
Tools for Discovery

40 YEARS OF INNOVATION 1979-2019









Readout electronics for large experiments

Carlo Tintori

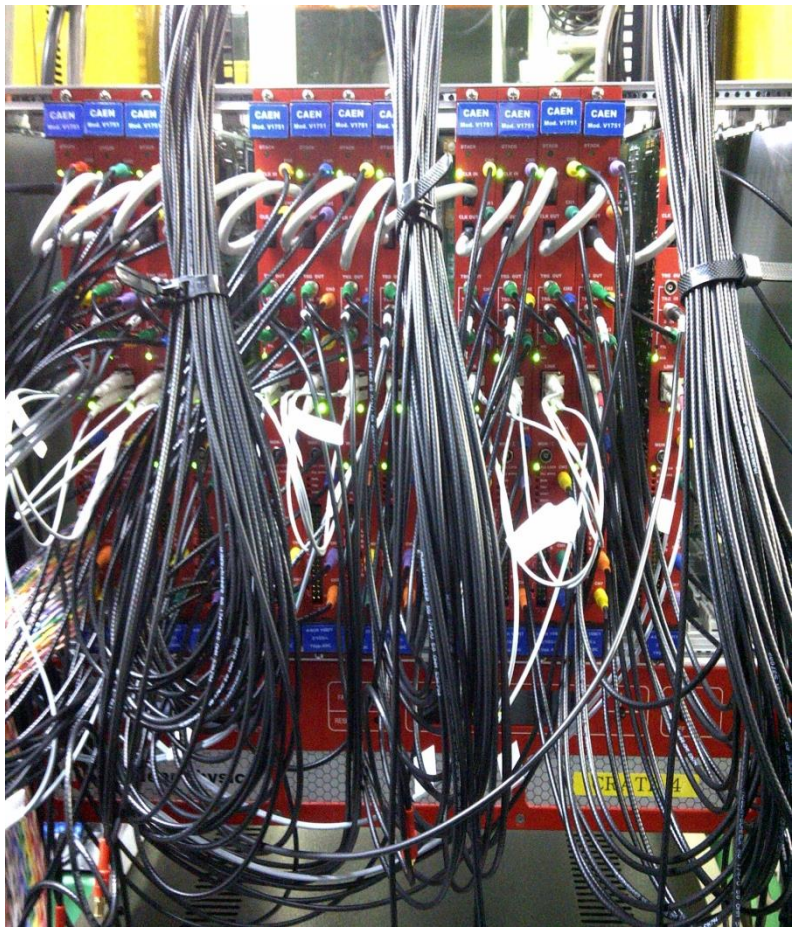
EIC Streaming Readout Conference - Camogli - May 23rd, 2019

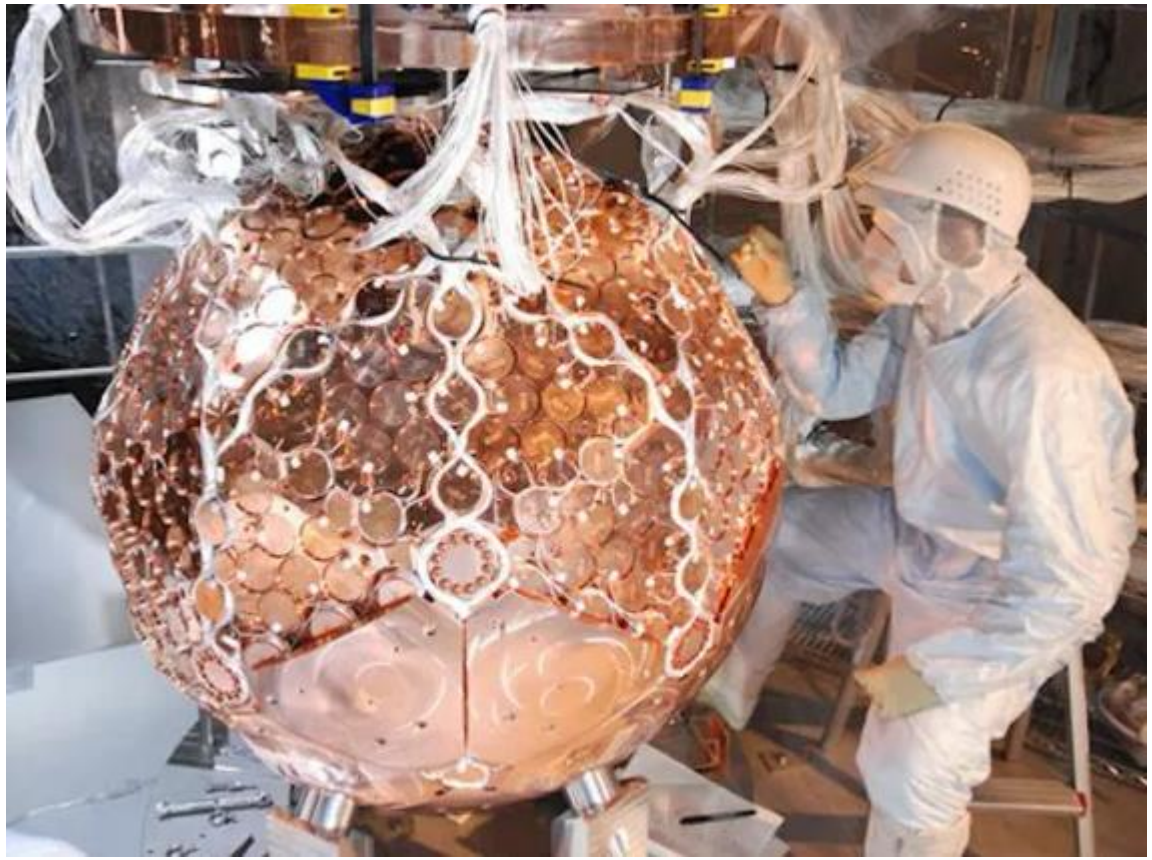
Outline

- **CAEN Digitizers:** 12 years side by side with the physicists
- **Digitizer 2.0:** the new generation of waveform digitizers and DPP algorithms
- **FERS-5200**: a distributed Front End Readout System, an alternative to rack electronics

Digitizers 1.0: 12 years of success

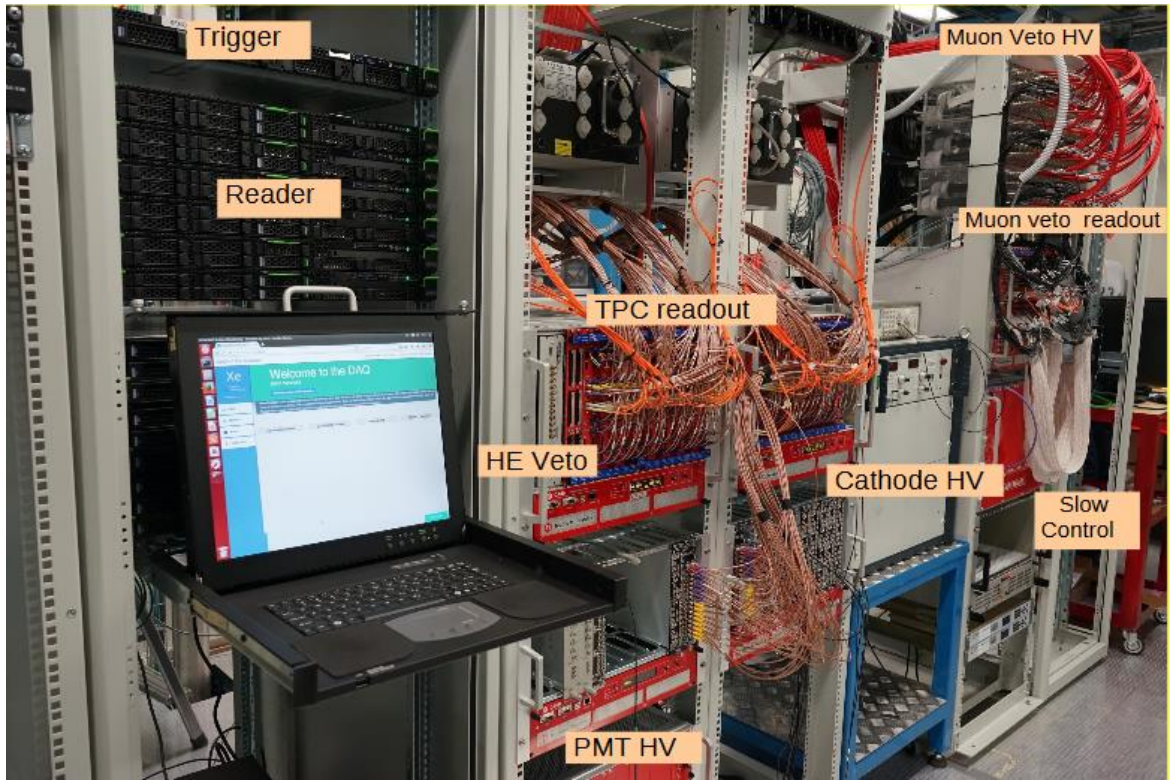
- **Xmass** @ Kamioka (Japan): Dark Matter
- **672** channels = 84 V1751s (1 GS/s, 10 bit) with custom FW (**ZLE**)





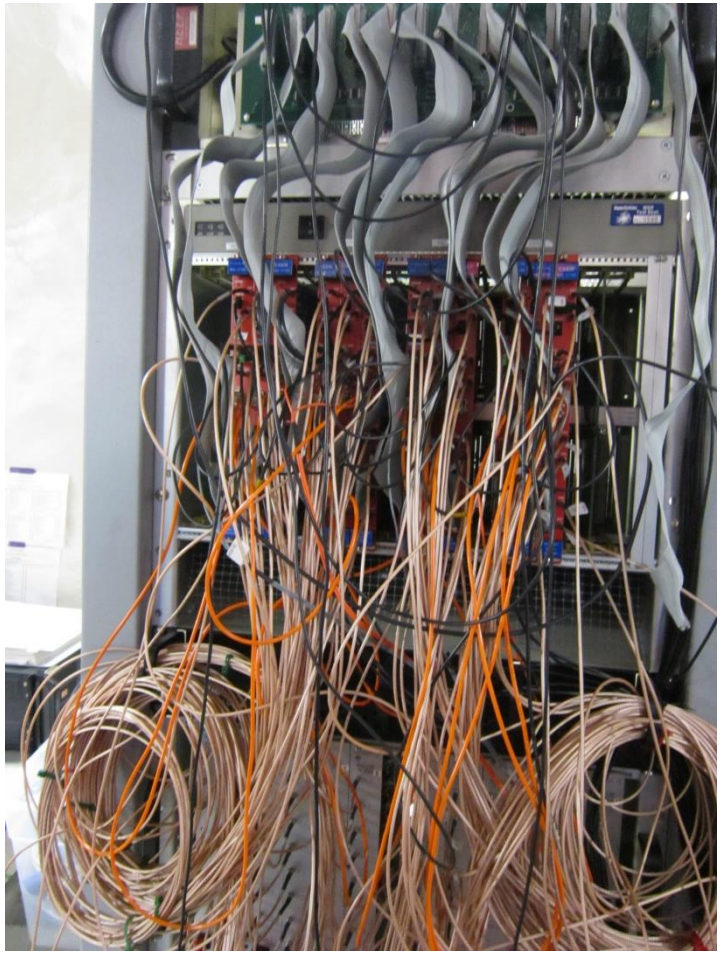
Digitizers 1.0: 12 years of success

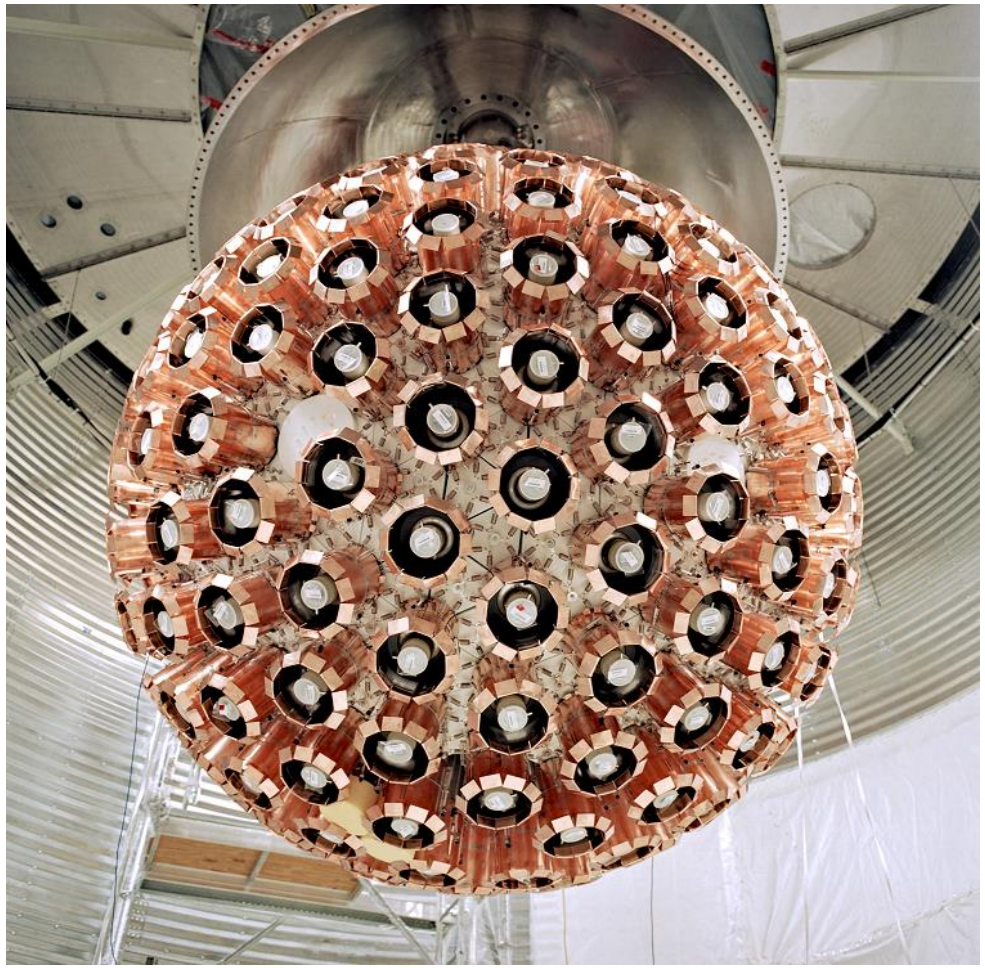
- **XENON1T** @ LNGS (Italy): Dark Matter
- **248** PMTs = 32 V1724s (100 MS/s, 14 bit). **Trigger-less** DAQ with custom FW (**DAW**)



Digitizers 1.0: 12 years of success

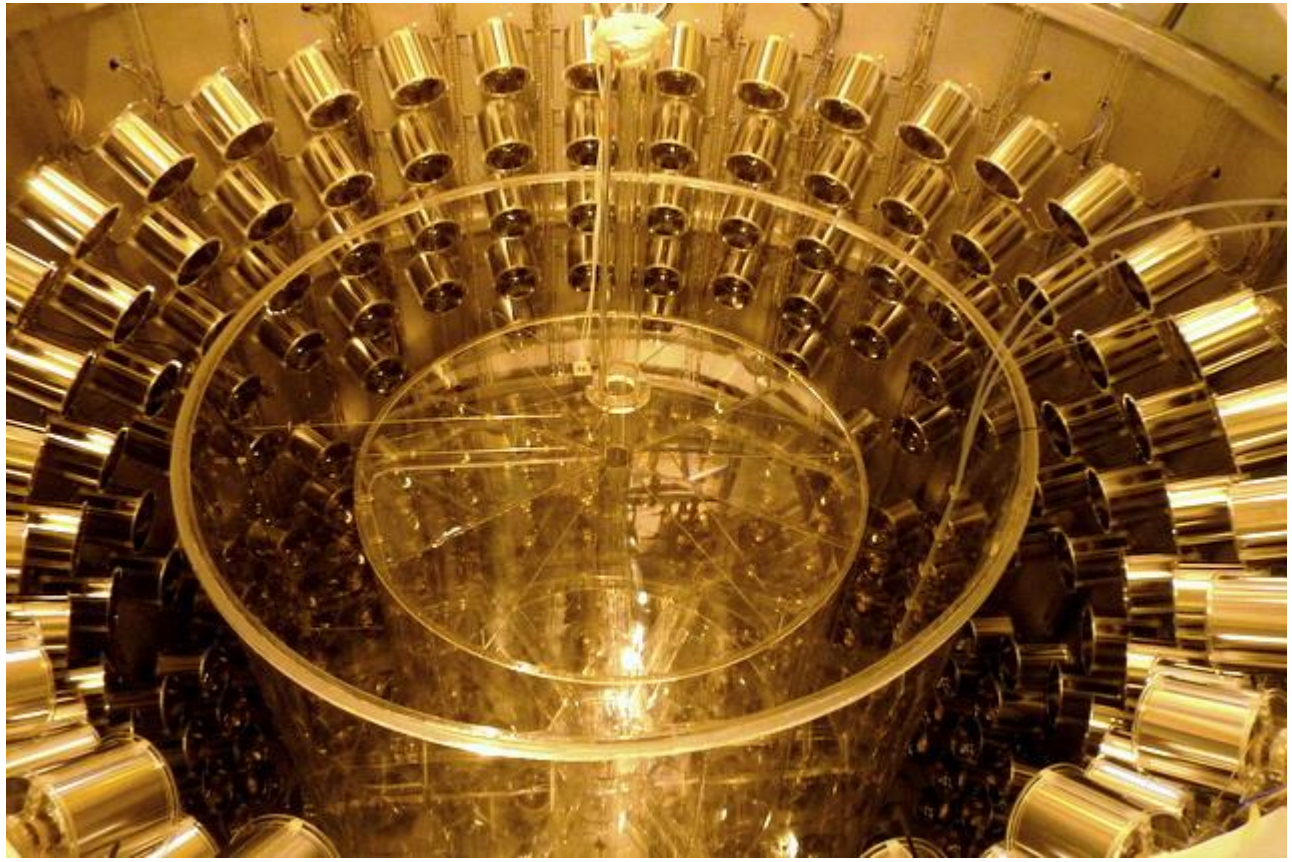
- **DEAP-3600** @ Snolab (Canada): Dark Matter
- **255** PMTs = 32 V1720s (250 MS/s, 12 bit) + 5 V1740 (62.5 MS/s, 12 bit). Tot: **576** readout channels





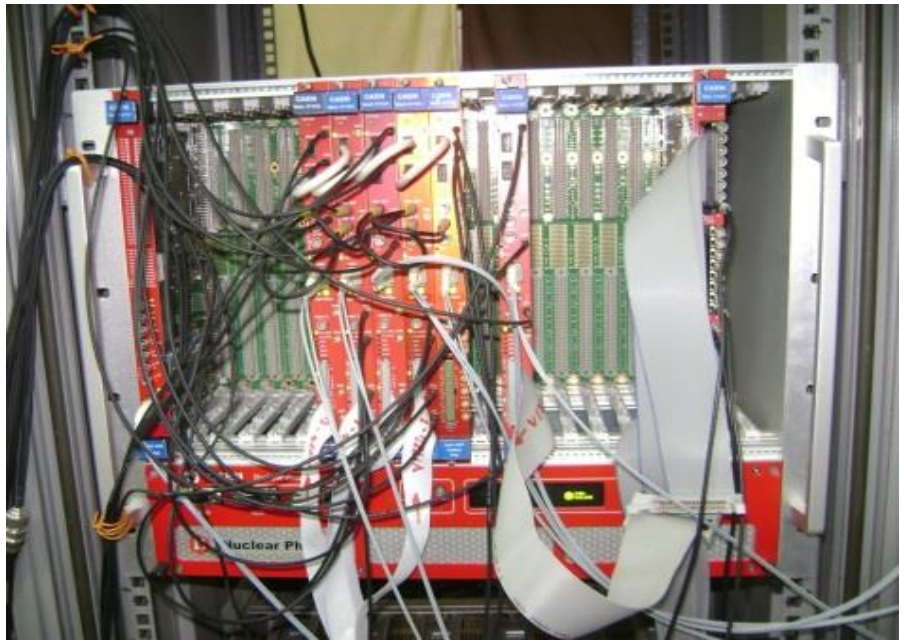
Digitizers 1.0: 12 years of success

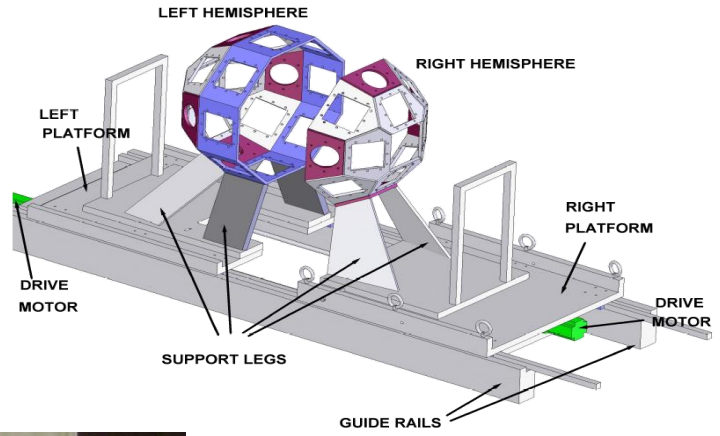
- **Double-Chooz** @ Chooze Power Plant (Ardenne, France): neutrino oscillation
- **368** PMTs = 46 V1721s (500 MS/s, 8 bit)



Digitizers 1.0: 12 years of success

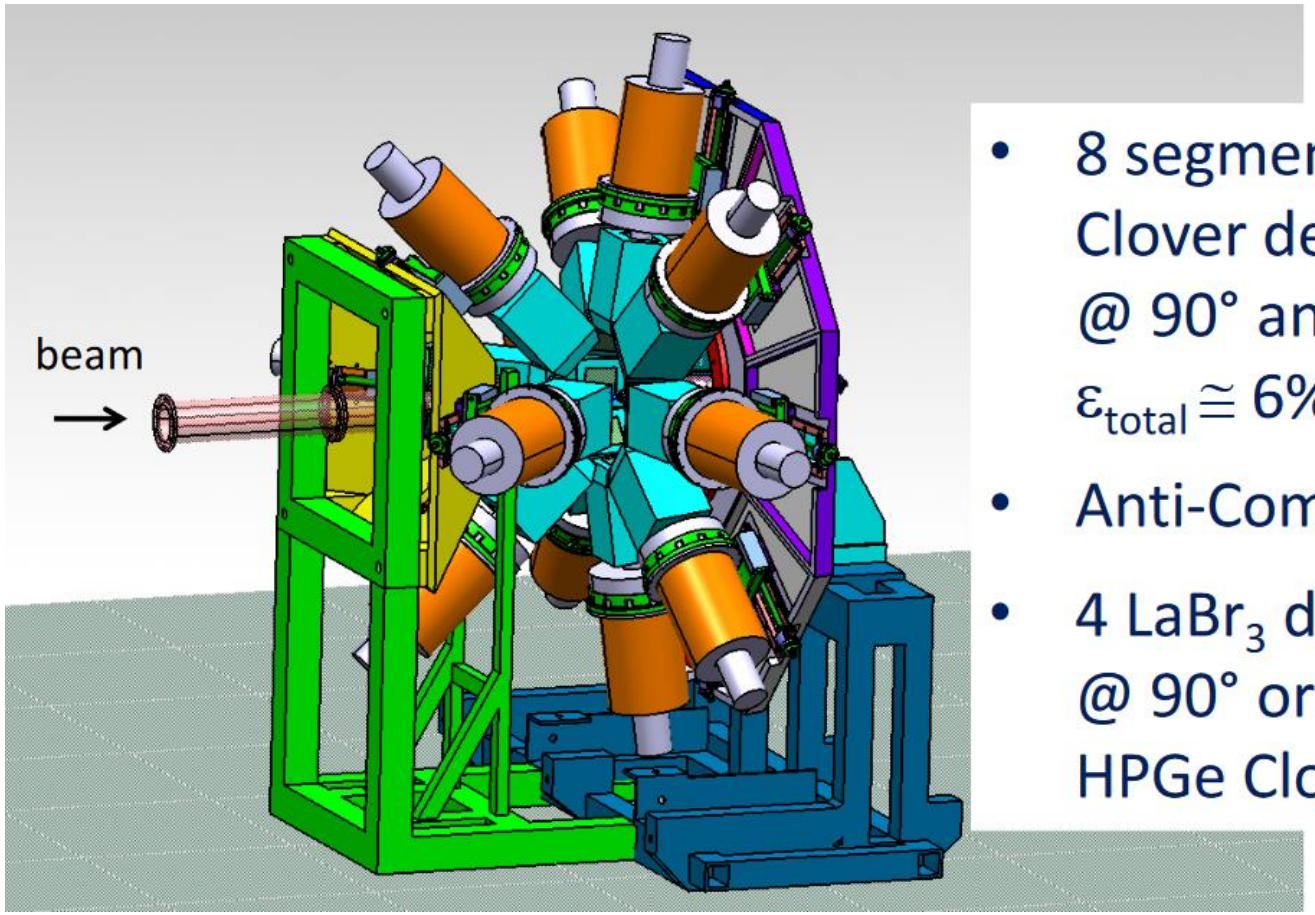
- **Dhruva** @ BARC (India): gamma-ray spectroscopy of fission fragment nuclei
- **Multi-detector** readout: 8 **Clover** detectors with **ACS** + 16 **$LaBr_3$** => 4 V1724s (100 MS/s, 14 bit, **PHA**) + 1 V1720 (250 MS/s, 12 bit) + 1 V1730 (500 MS/s, 14 bit, **QDC-PSD**)





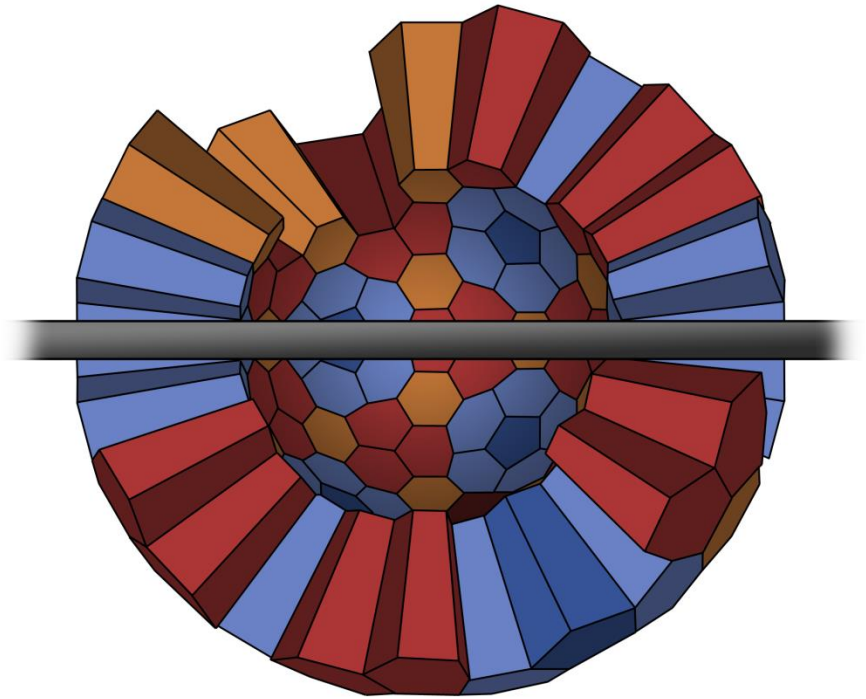
Digitizers 1.0: 12 years of success

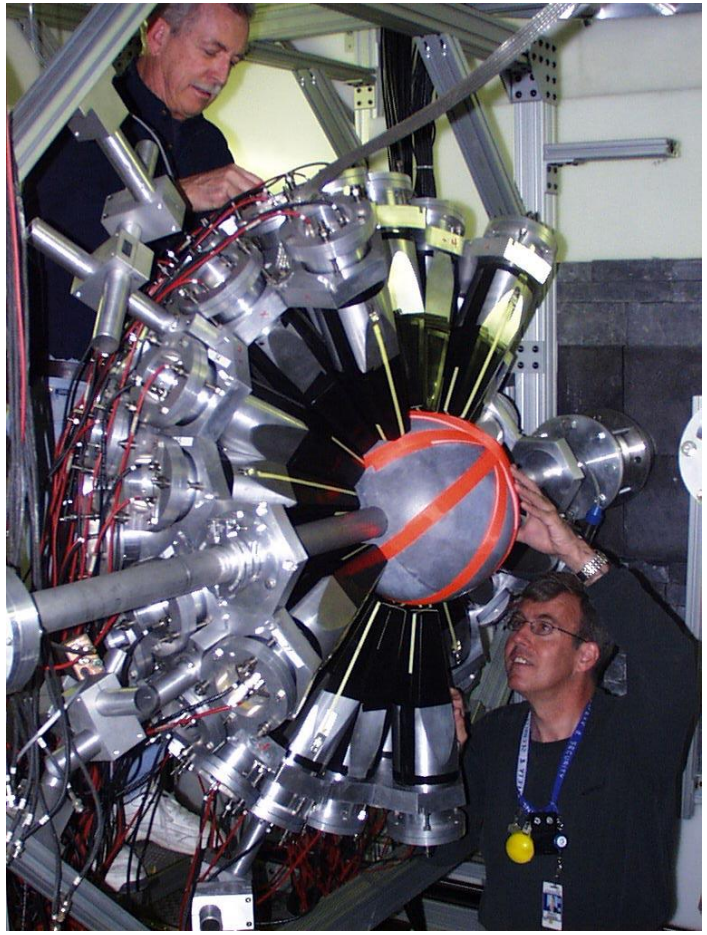
- **Eliade** @ ELI-NP (Romania): photonuclear reactions at Extreme Light Infrastructure
- **Clover** detectors: 36 V1725 (250 MS/s, 14 bit + PHA) + **$LaBr_3$**: 2 V1730 (500 MS/s, 14 bit + QDC-PSD)



Digitizers 1.0: 12 years of success

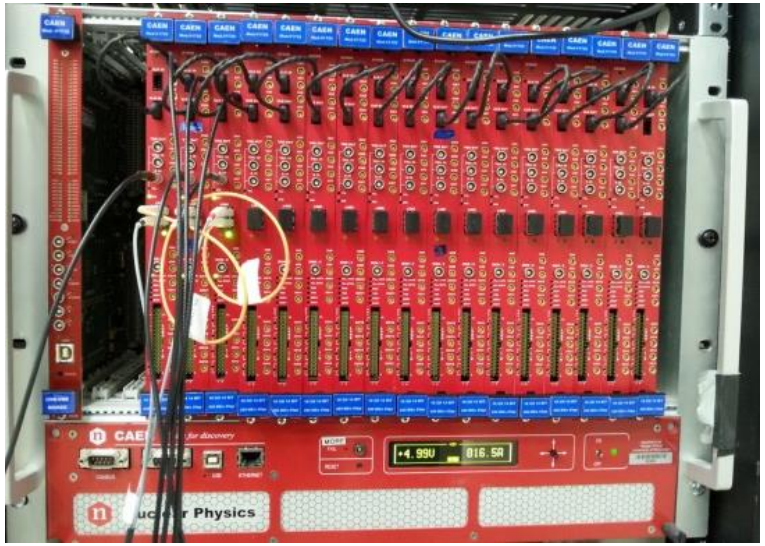
- **Dance** @ Los Alamos (USA): neutron capture
- **162** segments (BaF_2 crystals): 12 V1730s (500 MS/s, 14 bit) with **DPP-PSD**





Digitizers 1.0: 12 years of success

- **Prospect** @ Yale/ORNL (USA): oscillation signature of sterile neutrinos
- **360** PMTs = 22 x V1725s (250 MS/s, 14 bit) with **ZLE**



Digitizers 1.0: 12 years of success

- **Fast Neutron Collar** @ IAEA: non destructive assay of NPP's Fresh Fuel Rods
- 4 V1730s (500 MS/s, 14 bit) **with fast waveform readout (300 MB/s) and PSD**

Digitizers 1.0: 12 years of success

- **Exill** @ ILL (lifetimes of low-lying excited states): HPGe => 10 V1724s (100 MS/s, 14 bit + PHA) + $LaBr_3$ => V1751s (1 GS/s, 10 bit)
- **Mini Clean** @ Snolab (dark matter): 8 V1720s (250 MS/s, 12 bit, Raw Waveforms)
- **Dark Side** @ LNGS (dark matter): currently using V1720s => candidate new digitizer 2.0 (64 ch, 125 MS/s, 14 bit)
- **SPECT**: Single Photon Emission Computed Tomography (Liverpool): 4 V1724s + PHA
- **Samorad**: airborn gamma spectrometer for geological and soil mapping: 1 DT5740 + QDC
- **C-BORD**: Tagged Neutron Inspection System: PSD and ToF with V1730
- **Whole Body Counter** @ JRC (Italy): HPGe and NaI readout with V1725 (250 MS/s, 14 bit)
- **Tawara**: Tap Water Monitoring
- AND MANY OTHERS

Digitizers 1.0: 12 years of success

Model	# channels	MS/s	# bit	Wave	PHA	PSD	CFD	QDC	DAW	ZLE	Notes
V1730 / DT5730	16 / 8	500	14	√	√	√	√	√	√	√	Waveform recorder + Pulse Processor
V1725 / DT5725	16 / 8	250	14	√	√	√	√	√	√	√	Waveform recorder + Pulse Processor
V1751 / DT5751	8 / 4	1000	10	√		√	√	√		√	Waveform recorder + Pulse Processor
V1724 / DT5724	8 / 4	100	14	√	√				√	√	Waveform recorder + Pulse Processor
V1720 / DT5720	8 / 4	250	12	√		√		√		√	Waveform recorder + Pulse Processor
V1740 / DT5740	64 / 32	62.5	12	√				√			Waveform recorder + Pulse Processor
V1742 / DT5742	32 / 16	5000(1)	12	√							Waveform recorder (Switch. Cap. Array)
V1743 / DT5743	16 / 8	3200(1)	12	√							Waveform recorder (Switch. Cap. Array)
V1781 / DT5781	8 / 4	100	14	√	√						MCA
DT5781	2	100	14	√	√						MCA
DT5790	2	250	12	√		√		√			Pulse Processor

(1) switched capacitor ADC: fast sampling, slower A/D conversion (=> dead time)

Motivation

- More density, faster sampling rate, higher resolution => improved performance
- Increase readout bandwidth: from 1 to 10 Gbit/s
- Communication through standard Interfaces: 1/10 Gb Ethernet, USB 3.0 (yet keeping proprietary CONET)
- Make the synchronization easier (clock and timing distribution)
- Increase memory size: from SSRAM to DDR4 (=> from MBs to GBs)
- Renovating obsolete components
- Single FPGA (Zync US+) architecture => more resources for DPP algorithms and support for "Open FPGA"
- Embedded quad-core ARM (Linux) => middleware, web interface. Possibility to run user Data Processing SW
- Support of JESD204B, fast and flexible readout interface => new generation of A/D converters

Digitizers 2.0: Models

V2751: 16 ch, 1 GS/s, 14 bit

- Replace V1751
- Ultra fast detectors (diamonds, MCPs, SiPMs) with ps timing applications

V2725/V2730: 16 ch, 250/500 MS/s, 14 bit

- Replace V1725/V1730/V1720
- Optimal trade-off between cost and performances
- Covers most applications with medium-fast detectors
- Sub ns timing combined with high energy resolution

V2724: 32 ch, 125 MS/s, 16 bit

- Replace V1724 (mainly for spectroscopy & MCA)
- Advanced Front-End (programmable gain, shaping, AC or DC coupling, etc…)
- Best suited for semiconductor detectors (HPGe, Clover, SDD…)
- Typically connected to Charge Sensitive Preamplifiers

V2740: 64 ch, 125 MS/s, 14 bit

- Replace V1740
- Possibility to implement 64 MCAs (PHA firmware) for high channel density spectroscopy solutions
- Good fit for Neutrino and Dark Matter experiments (Candidate for Dark Side)

SCA models

- No plans to replace V1742/V1743 so far
- New ASICs (Sampic, DRS5, …) will be considered

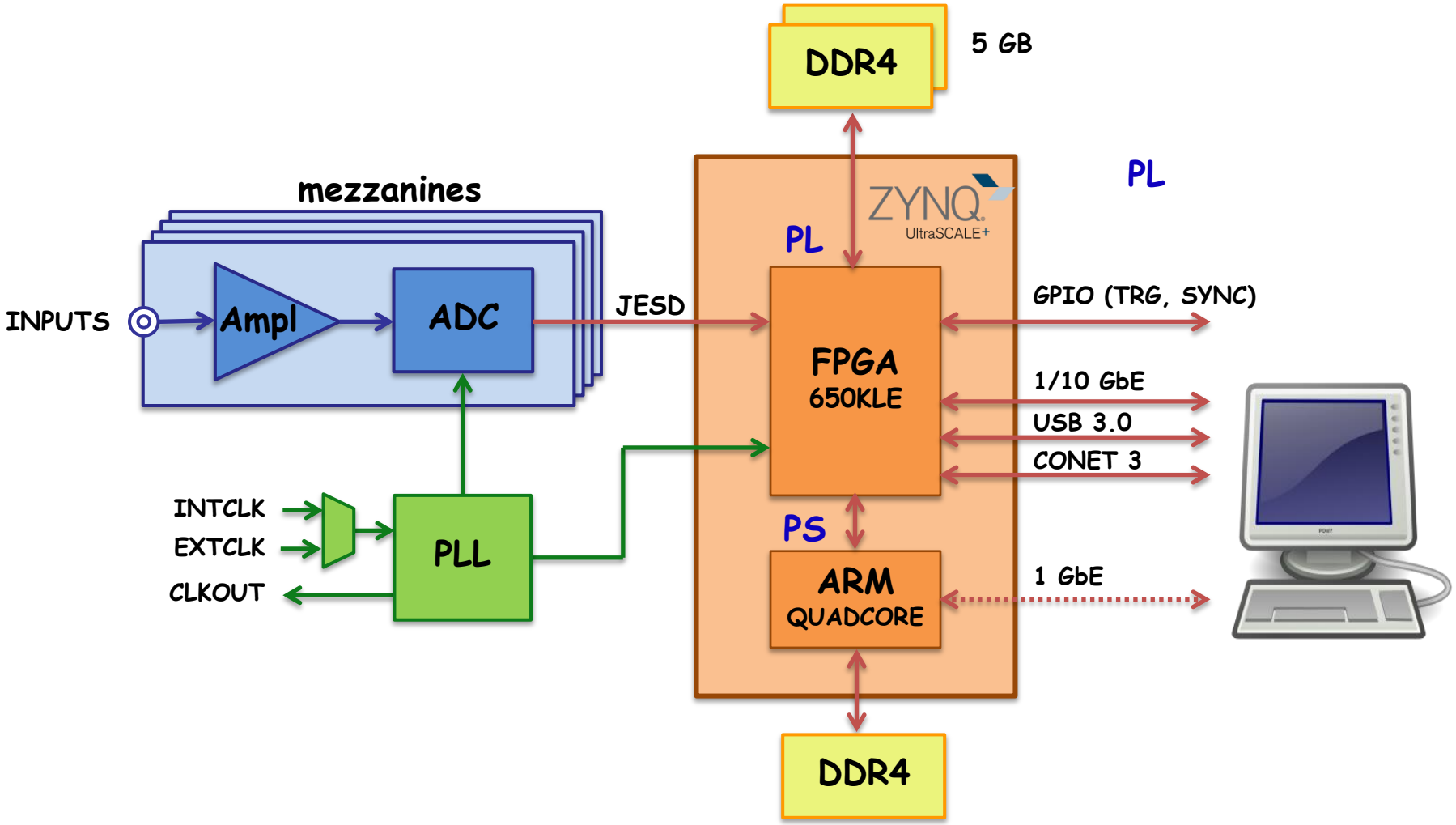
Digitizers 2.0: Communication

- **Ethernet**
  - Front Panel SFP+ with RJ-45 (copper) or LC connectors (fiber)
  - Ethernet port connected to Programmable Logic of the FPGA (PL)
  - TCP-IP stack implemented in embedded ARM (PS).
  - **1 GbE:** tested up to 100 MB/s (TCP-IP)
  - **10 GbE**: fiber only. Preliminary tests up to ~200 MB/s. Optimization still on going
- **USB 3.1**
  - Front Panel Type-C connector
  - Tested up to 300 MB/s
- **CONET (Daisy Chainable Optical Link)**
  - CAEN proprietary protocol
  - Current version (CONET 2.0): 1 Gb/s => ~90 MB/s, up to 8 boards in daisy chain
  - A3818 PCIe collector board (up to 4 links = 32 digitizers)
  - USB 3.1 to CONET adapter being designed in 2019
  - Potential upgrades: 10 Gb/s, synchronization over CONET
- **VME**
  - Legacy of the old digitizers. Keep for retro compatibility.
  - VME64X compliant. MBLT64, 2eSST
  - Not implemented yet. Low priority. Pursuing bus-free readout systems!!!

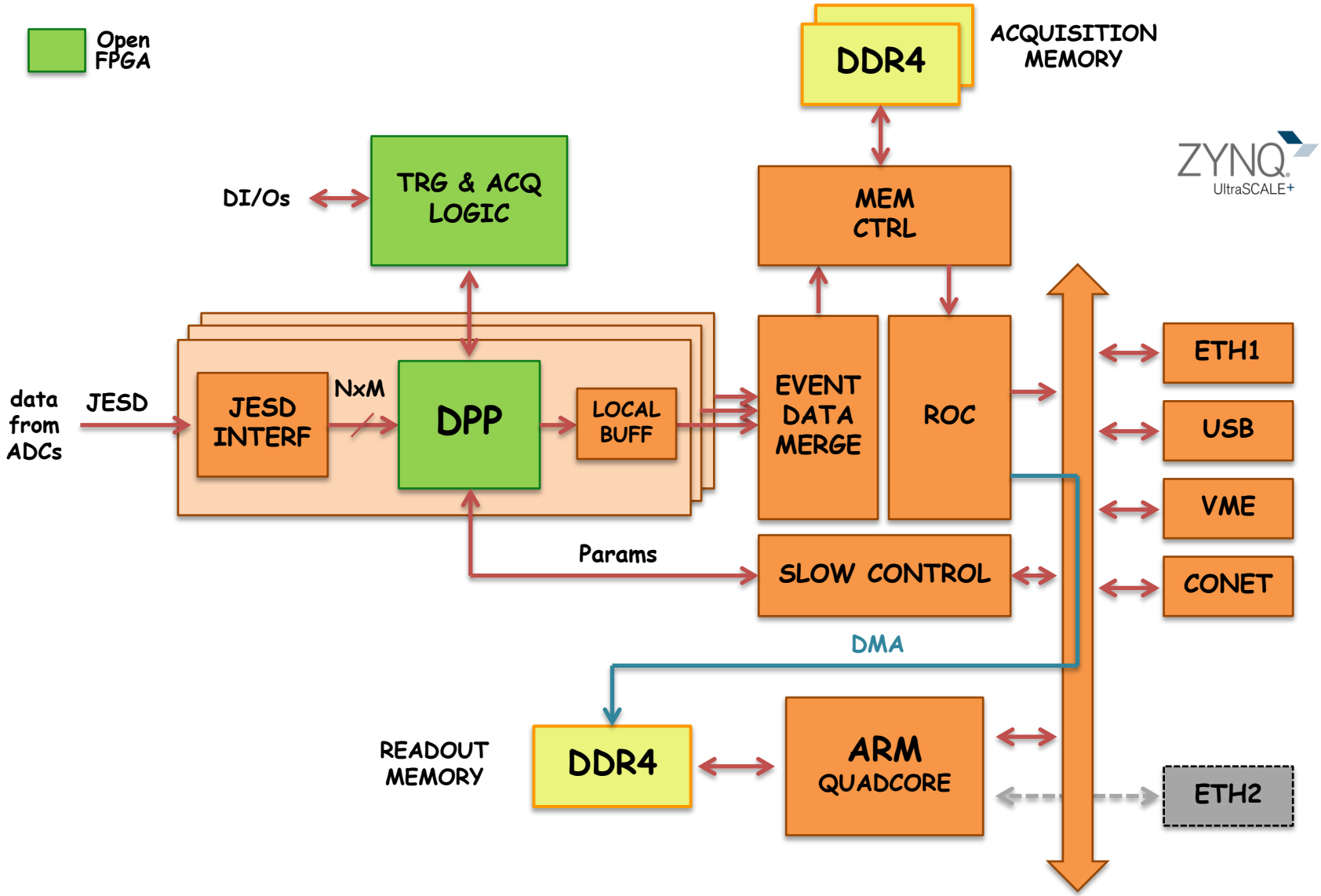
Digitizers 2.0: Synchronization

- **Front Panel Sync Connector**
  - Two 4-pin AMP Modu-II connectors (input + output)
  - Brings Reference Clock (typ. 62.5 MHz) + Sync (T0) signals
  - Daisy Chain (1st digitizer = master) or Star distribution from external fan-out
  - On board, high performance PLL for ADC clock synthesis and phase adjust
  - Sync signal defines Acquisition Start-Stop and/or the zero of the time stamp
- **Backplane Synchronization**
  - Reference Clock and Sync signals routed to J0 connector
  - Requires additional backplane (plugged on back side of P0 connectors on VME64X backplane)
  - Signals from a master digitizer (self-synching) or external source via P0
- **Synchronization from readout link (future upgrades)**
  - Clock recovery from the Front Panel link (optical or copper)
  - Potential support for White Rabbit
  - Potential evolution of CONET to a synch + readout link
- **Other I/Os**
  - 4 LEMO connectors: TrgIn, TrgOut, GPI, GPO (Typ. Start/Stop, Busy, Veto, etc…)
  - 16 LVDS In/Out: individual self-trigger outputs, trigger validations, Veto, Busy, Start, Stop, Pattern Input, etc…

Digitizers 2.0: Architecture



Digitizers 2.0: FPGA Block Diagram



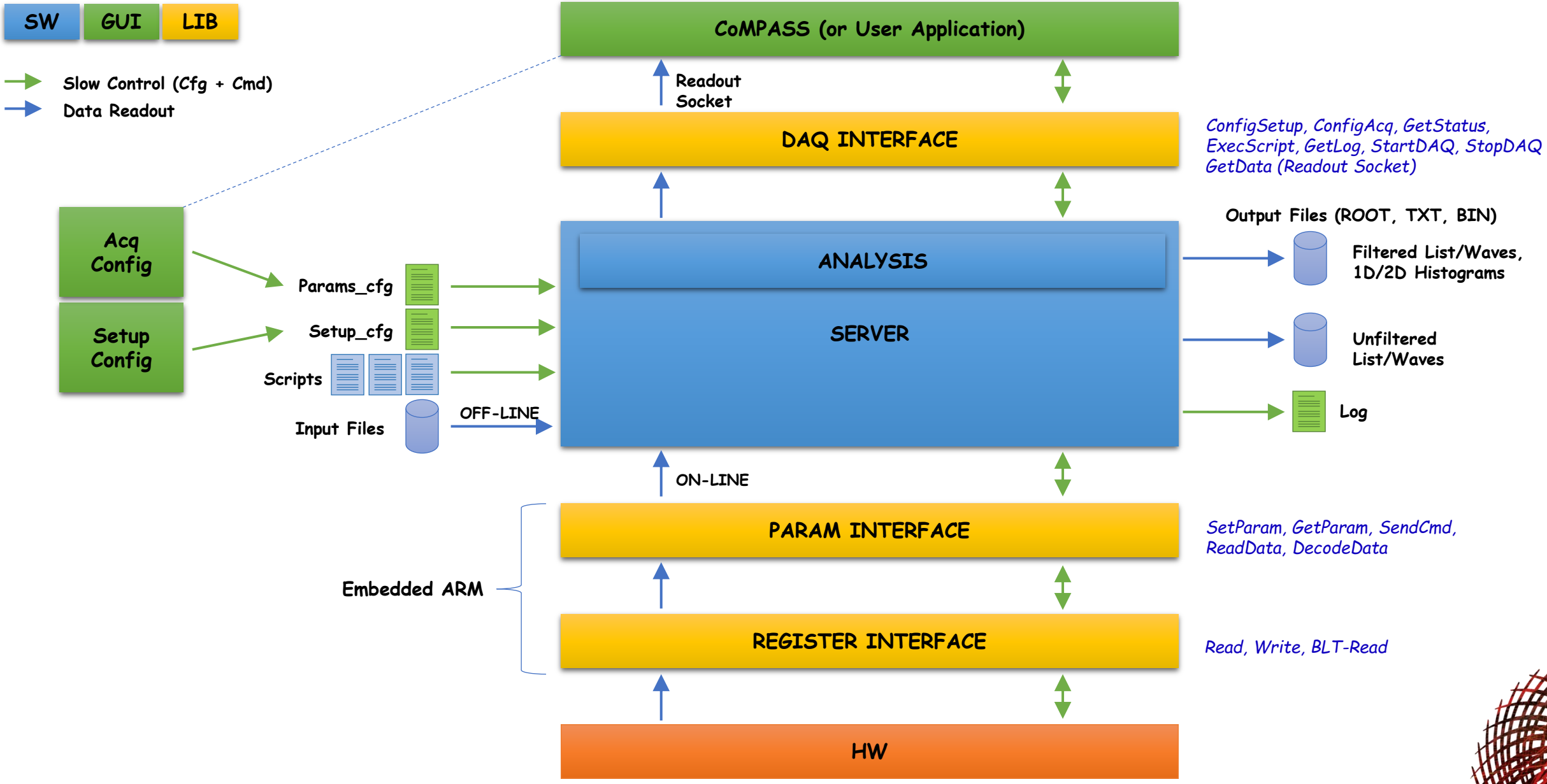
Digitizers 2.0: Firmware

- Single FPGA: 653 kLE (Zync US+ XCZU11EG). Upgrade to 1143 kLE available (Zync US+ XCZU19EG)
- Waveform Readout Modes:
  - Common Trigger (programmable pre/post trigger, record length up to hundreds of Msamples)
  - Common Trigger + ZLE (in-window zero suppression)
  - Independent self-triggers with adaptive record length (DAW)
- DPP Modes (include waveforms too):
  - Independent self-triggers (common trigger also available)
  - BLR: Baseline restorer
  - PHA: pulse height of CSP signals (trapezoidal filters)
  - QDC: self-gated integrator (pulse charge)
  - PSD: pulse shape discrimination (dual integrator for fast/slow components or Rise Time discriminator for CSP)
  - CFD/LED: digital discriminators with programmable threshold, delay and attenuation
  - TDC: time stamping with fine timing interpolation (~ 10 ps RMS @ 500 MS/s)
  - PUR: pile-up detection/rejection, dead time calculation
  - Coincidence/Anti-Coincidence
- Embedded ARM with Linux allows for further online data processing/concentration
- **Open FPGA** (Firmware Development Kit)
- All firmware types are resident in Flash Memory: live reboot from SW command

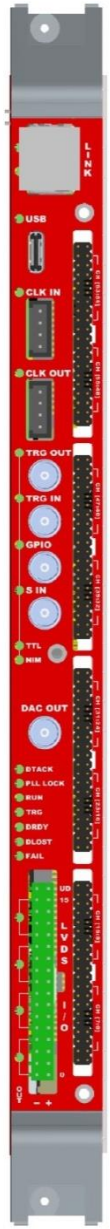
Digitizers 2.0: Software

- Middleware in embedded ARM: provides slow control and readout
- High Level API with set/get parameters. Same for embedded SW or Host PC
- Data Readout: polling or streaming (ZeroMQ Transfer Protocol)
- DAQ Server with API for user remote control:
  - Multi-board readout and synchronization
  - Manages old and new digitizers, as well as different models and firmware types
  - GUI to configure setup and parameters for the acquisition => Config Files
  - GUI for acquisition control (Start/Stop/Data files/Statistics)
  - Data Analysis and correlation: coincidences, cuts, 1-D and 2-D histograms, add-back, etc…
  - Output Data Files: raw, lists (T, E, PSD), histograms, waveforms; filtered and unfiltered
  - TCP-IP socket for on-line data readout (from user applications)
  - Off-line runs from Data Files previously acquired
- WEB services and applications
- “WaveDump like” readout demo (simple C programs)
- CoMPASS for multi-parametric DAQ (spectroscopy)

Digitizers 2.0: Software Layers



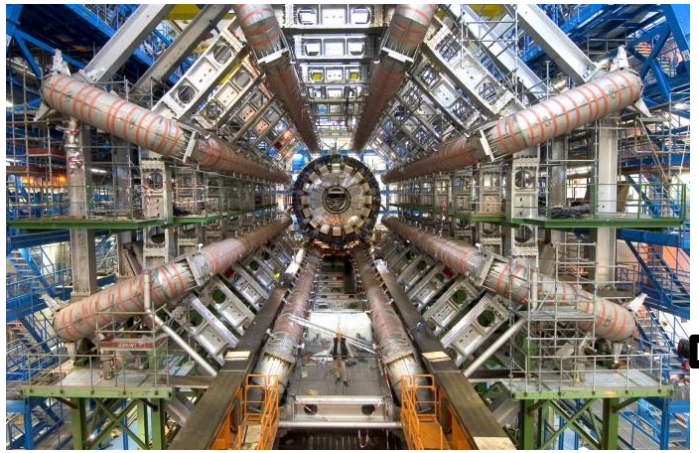
Digitizers 2.0: V2740

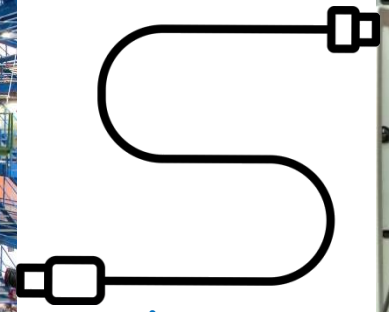


- 64 channel, 125 MS/s, 14 bit waveform digitizer
- Four 40 pin, 2 mm header connectors
- Adapters to 1.27 mm flat cables or coax
- Differential or SE inputs
- 1 GbE or 10 GbE
- USB 3.1
- CONET 2.0 (optional)
- Common Trigger (waveforms) or Individual Self-trigger modes
- DPP options: PHA, QDC, PSD, CFD
- Advanced Waveform Readout modes: ZLE, DAW
- Open FPGA
- 4 LEMOs + 16 LVDS programmable I/Os
- 1 DAC output (signal inspection or trigger sum)
- Available in desktop form factor

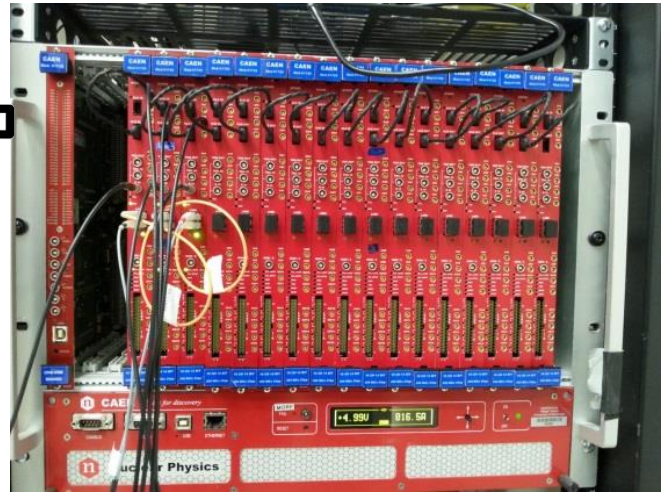
Rack electronics vs Distributed readout

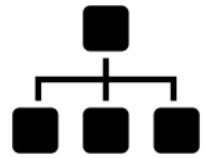
- **Rack Readout Electronics:**
  - Front End Preamplifiers close to the detectors
  - Long cables bring analog signals to readout electronics (ADC, TDC, etc.)
  - A/D conversion, online data processing and communication concentrated in racks
  - Typically based on standard busses (VME, xTCA, PXI…)
  - DAQ computers close to racks with readout electronics





Long Multiwire Cables

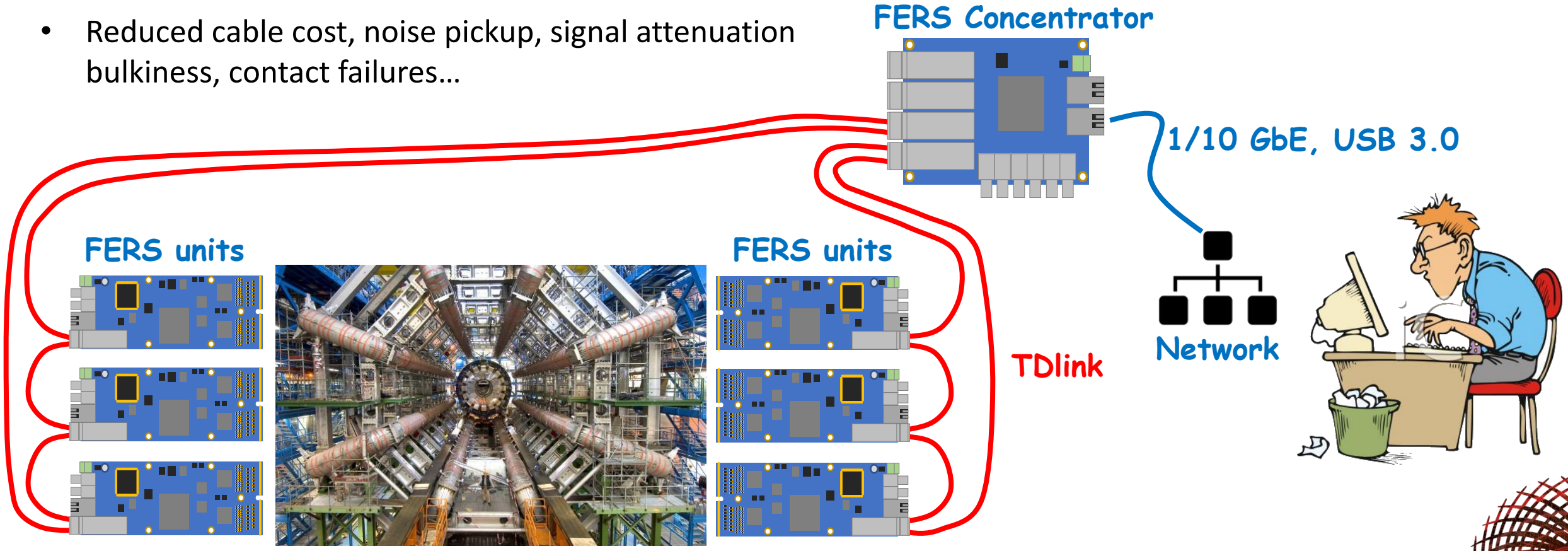




Network

Distributed Front End Readout System

- Front End Preamplifiers, A/D conversion and data processing in small **FE card**
- **TDlink**: synchronization, readout and slow control over optical fibers
- Concentrator Board: provides global synch + data sorting, formatting and storage
- Easy scalability to thousands channels
- Reduced cable cost, noise pickup, signal attenuation bulkiness, contact failures…

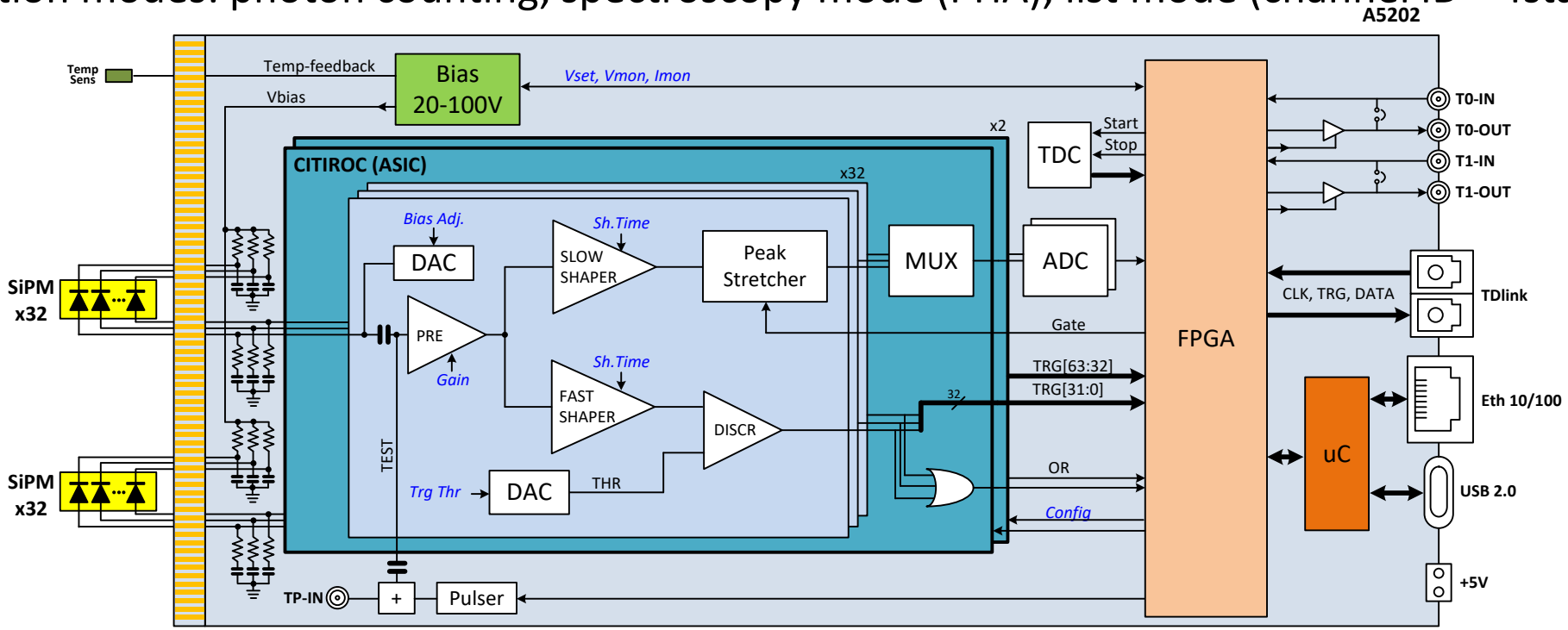


FERS platform

- **FERS unit**: single card housing Front End ASICs, ADC and/or TDC, FPGA, I/Os, interfaces and, in some cases, detector power supply
- **FERS communication interfaces**: TDlink (sync + commands + data) or Ethernet, USB 2.0 (data only, mainly used for evaluation)
- Auxiliary **I/Os** for sub-ns timing and low latency trigger distribution (alternative to TDlink)
- Different FERS units will be part of a unique **family**, all sharing the same architecture and readout protocols
- **A5202**: first member of the family, based on **Citiroc-2A** (by Weeroc). 64 channel readout for SiPMs.
- Potential future developments:
  - **Maroc** (PMTs)
  - **Petiroc** (SiPM readout with high timing resolution)
  - **Sampic** (10 GS/s SCA waveform digitizer and ps TDC) from LaL, D. Breton
  - **AARDVARC** (13 GS/s) and **ASOC** (3.2 GS/s) SCA waveform digitizer and ps TDC from Nalu Scientific
  - Digital readout for discrete components preamps (e.g. **A1442**, 16 channel preamp for Silicon Strip Detectors)
  - and others…

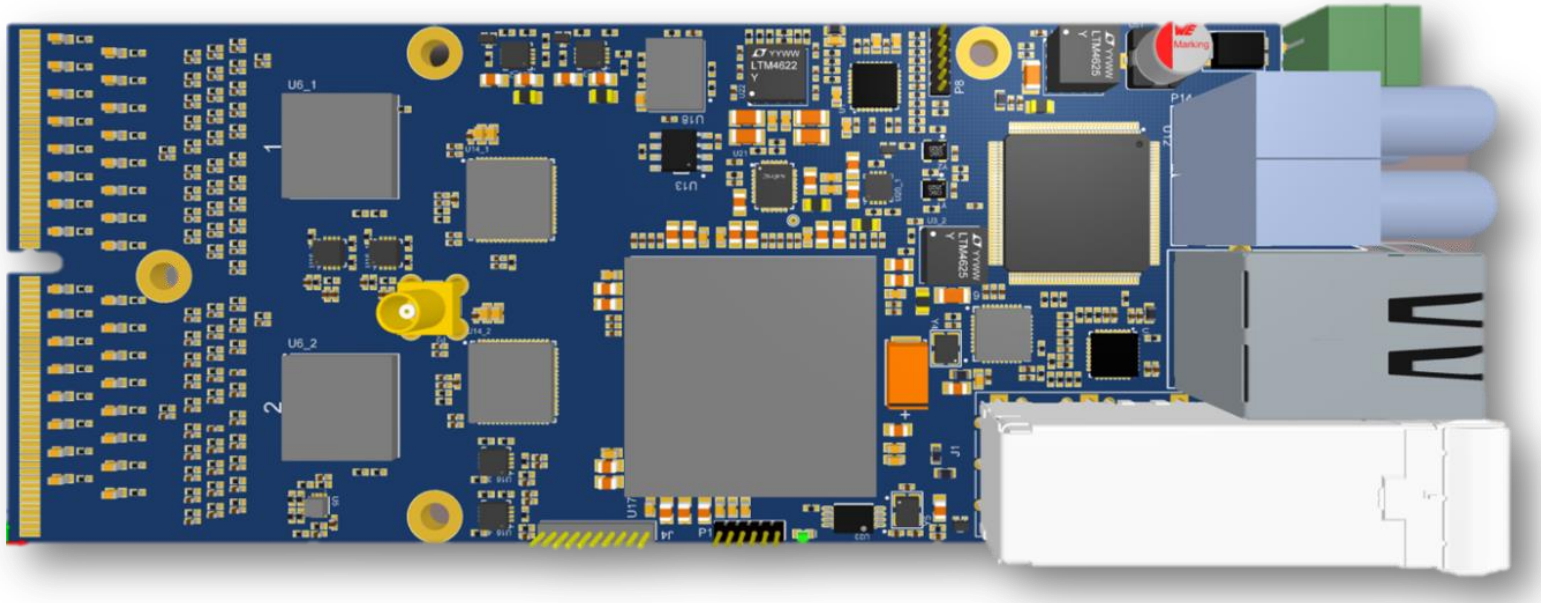
A5202: 64 channel SiPM readout (Citiroc 2A)

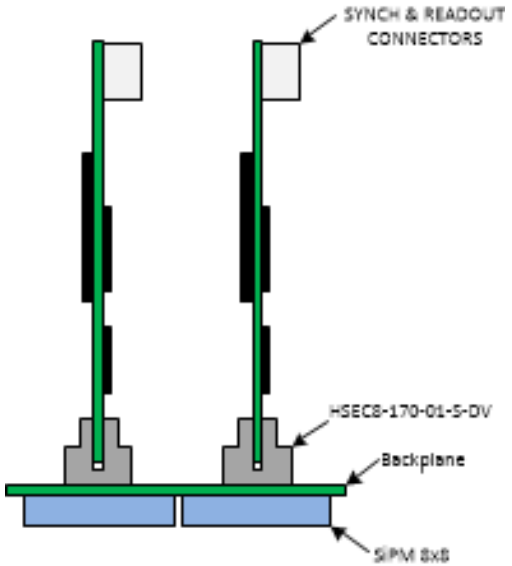
- Based on two ASICs Citiroc 2A (Weeroc): 64 channel SiPM readout
- Up to 4096 channels managed by a single concentrator board
- Embedded HV bias (20-100V) with temperature feedback. Individual HV adjust per channel
- Programmable gain and shaping time
- Individual discriminator thresholds: down to 1/3 pe
- 50 ps TDC for high resolution time stamping (OR trigger to Reference Input on LEMO)
- Acquisition modes: photon counting, spectroscopy mode (PHA), list mode (channel ID + Tstamp + ToT)



Mechanics

- The size of the FERS unit is ~15 x 6 cm (for the A5202)
- The inputs (signals from the detectors) comes through 0.8 mm edge contacts mating a Samptec HSEC8-170-01 connector
- When used “stand alone”, the card can be housed in a box with an adapter to 2.54 mm header connector for the inputs
- For experiments, a custom backplane or cable adapter can be designed to fit the mechanics of the detector

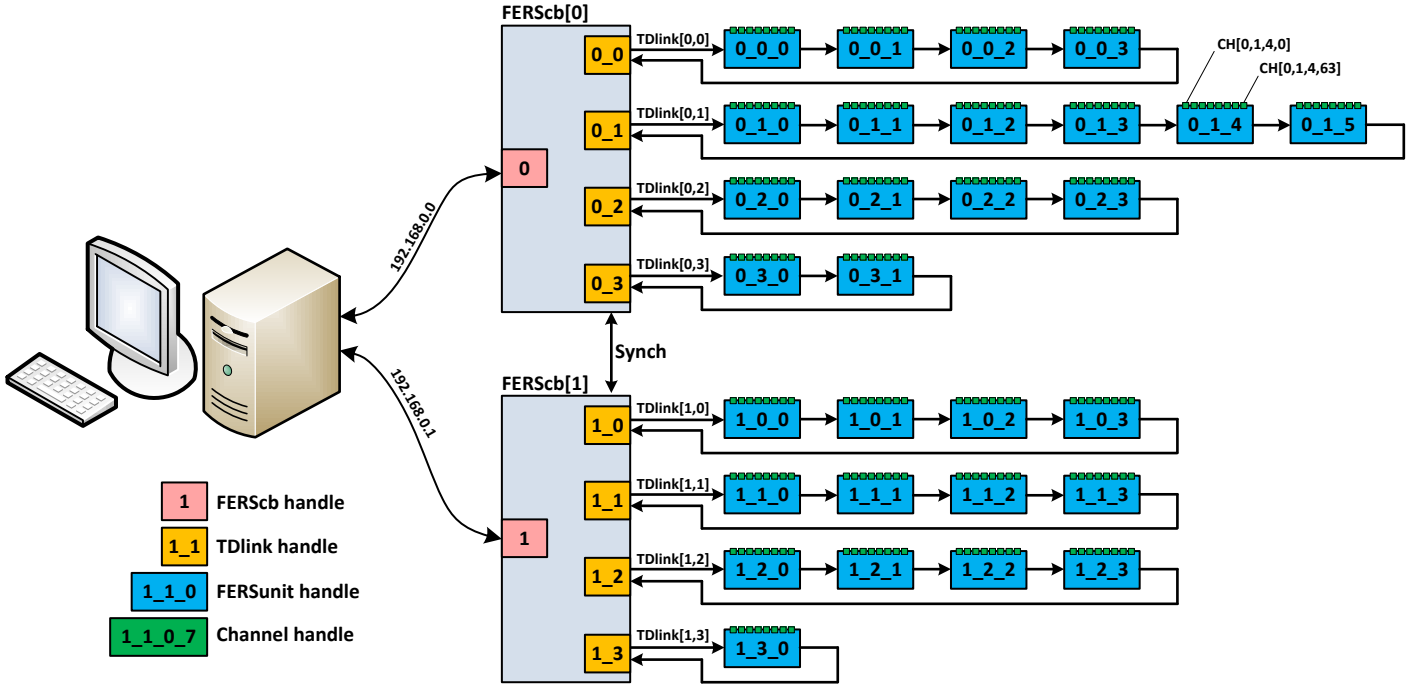




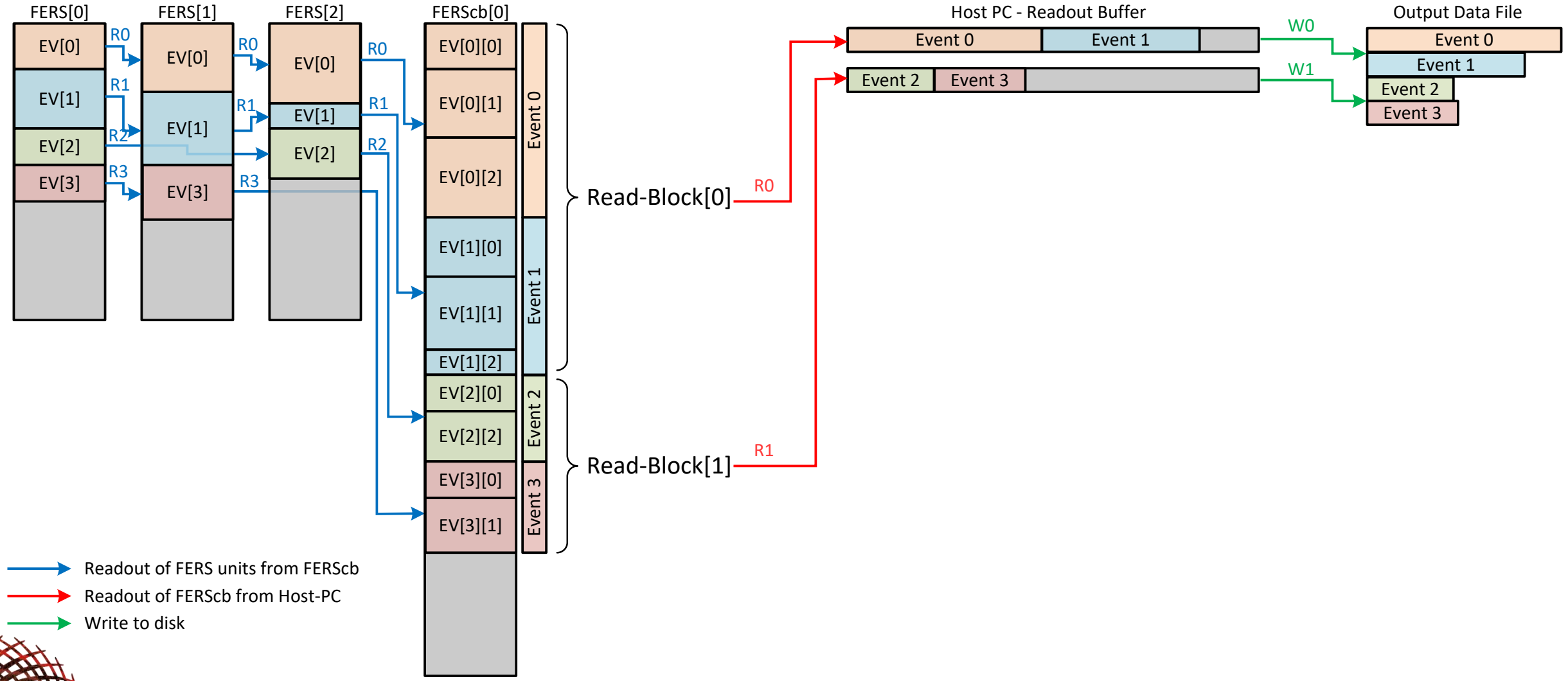
Acquisition and Readout Modes

- Acquisition modes:
  - **MCS Mode** (e.g. photon counting in SiPMs): uses fast discriminator signals. Counters are simultaneously latched, saved to memory and cleared. No dead time in counting, up to ~20 Mcps/ch.
  - **Spectroscopy Mode**: A/D conversion of the pulse height (preamp + shaper + peak hold + 14 bit ADC). Common trigger (int. or ext.), zero suppression. Max trigger rate = 100 KHz.
  - **Timing Mode**: independent hit recording: channel ID + timing (deltaT, 0.5 ns resolution) relative to a common start or common stop (T-ref signal from LEMO input). Gating mode (coincidence window). Max total hit rate = ~50 Mcps/board.
  - **Timing + ToT**: same as timing mode, with added Time Over Threshold (low resolution spectroscopy). Linearization LUT. Max total rate = ~20 Mcps.
  - Other acquisition modes for other ASICs (e.g. waveforms readout of SCA digitizers => 1024 samples per trigger)
- **FERS unit**: formatted data packets created by FPGA. Little data buffering.
- **FERS concentrator**: two readout strategies:
  - **Common trigger** => Readout based on Trigger Number or Trigger Time Stamp. **Event Building** in the concentrator board: data packets belonging to the same trigger (coming from all FERS units) are merged into a single event data block saved to the concentrator memory.
  - **Individual self-triggers** => each channel pushes data asynchronously, typically at different rates. Data aggregated in small packets in FERS units, then bigger packets in FERS concentrator. Data correlation demanded to DAQ software in computers.
- The concentrator board provides an ARM processor running Linux and huge DDR memory for data buffering and efficient transfer to host computers

- Daisy chainable serial link on fiber optic (up to **6 Gb/s**).
- Provides data transfer (readout + slow control), clock distribution, synchronized commands for time stamp reset, acquisition control, trigger distribution and/or validation, busy management
- One link connects up to 16 FERS units
- One concentrator board with 4 links can read 64 FE units, that is 4096 channels!
- **FERS-tree**: Multiple concentrator boards can be synchronized to build large readout systems



Event Building in Concentrator Board



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Thank you!