A new readout electronics for the LHCb Muon Detector Upgrade

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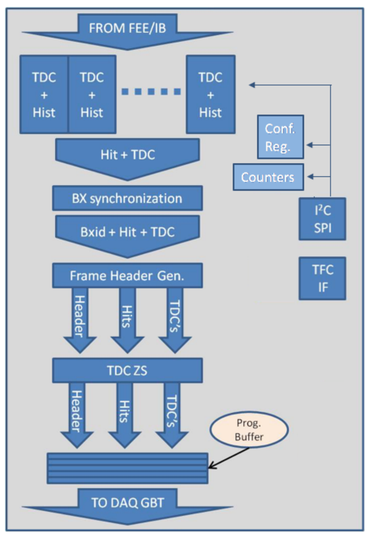
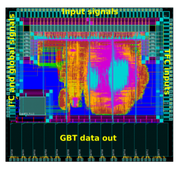
Introduction: the new Readout System

The 2019 upgrade of LHCb Muon System foresees a trigger-less 40 MHz readout scheme and requires the development of a new Off Detector Electronics (nODE) board, based on the nSYNC, a radiation tolerant custom ASIC developed in **UMC 130 nm technology**. The muon readout electronics has the purpose to process the digital signals from the front-end electronics, performing bunch crossing alignment, data zero suppression, time measurements. With respect to the current system, the new boards will allow a muon system readout at 40 MHz (the bunch crossing frequency at LHC), thanks to the nSYNC functionnalities, and the new optical communication system based on the GBTx driver/serializer chipset.

nSYNC Architecture

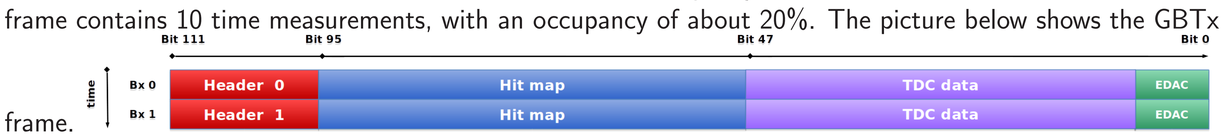
The nSYNC, an ASIC in UMC 130 nm technology, is the main component of the nODE board. It receives, through 48 input channels, the digital signals coming from the front-end electronics of the muon chambers.





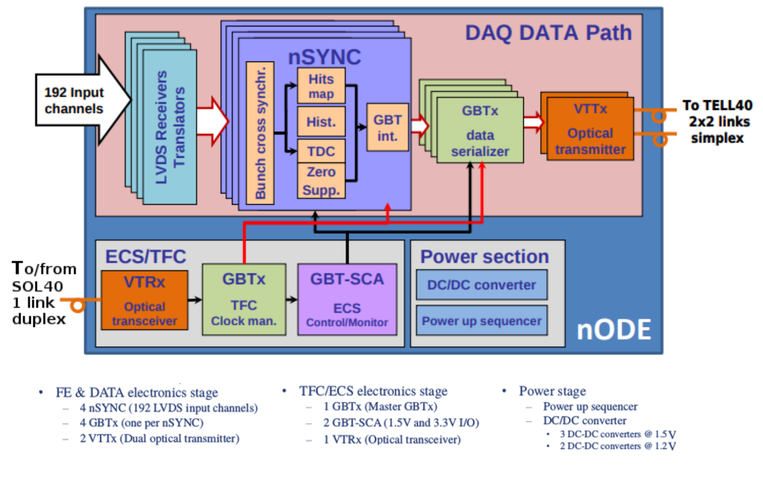
- The arrival time of the signals is measured by a fully digital TDC (one for each input), measuring the phase with respect to the LHC 40 MHz master clock. The TDC can work with several time resolutions, i.e. the number of slices on which the master clock can be divided, from 8 to 32 (16 nominal).
- The output data of each TDC channel consist of a binary flag (the Hit/NoHit information) and a 5 bits-wide word with the measured phase time (if any). This information is available every 25ns.
- These data go through a programmable-lenght pipeline in order to align hits from different channels related to the same bunch-crossing. This allows to uniquely associate the correct 12 bits-wide bunch-crossing identification number (BXid) to the all aligned data and pack these information together.
- The nSYNC creates then the extended frame, composed by Header + HitMap + TDCdata. The data are then Zero Suppressed (ZS)/truncated in order to fit the built frame into the GBTx frame, to be sent through the optical link. The HitMap, that represents the physical information and identifies the channel of the transmitted TDC measurement, is always sent non zero-suppressed, regardless the occupancy. The TDC data instead will be truncated if necessary.

The last 8 bits of the frame are dedicated to the Hamming code, used to correct single-errors or detect double errors. This feature can be disabled to increase the TDC occupancy in the frame. At nominal resolution the frame contains 10 time measurements, with an occupancy of about 20%. The picture below shows the GBTx frame.

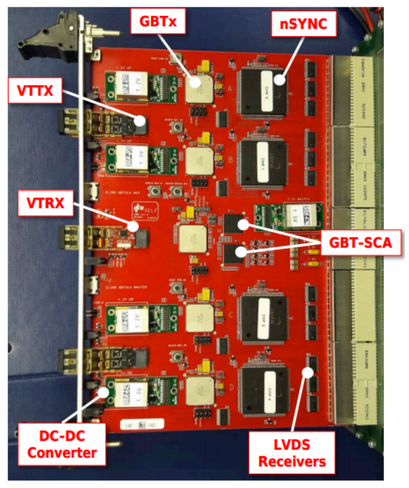


nODE Architecture

The main component of the new readout is the new Off-Detector Electronics Board (nODE) that will be equipped with 4 nSYNC chips.

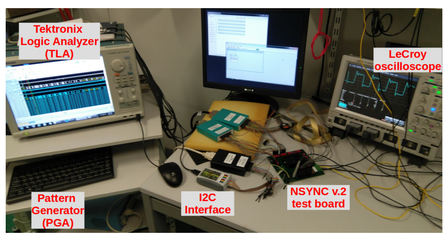


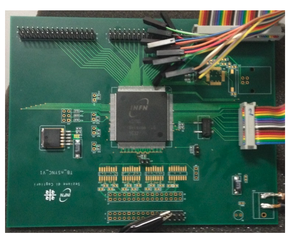
- FE & DATA electronics stage
  - 4 nSYNC (192 LVDS input channels)
  - 4 GBTx (one per nSYNC)
  - 2 VTTx (Dual optical transmitter)
- TFC/ECS electronics stage
  - 1 GBTx (Master GBTx)
  - 2 GBT-SCA (1.5V and 3.3V I/O)
  - 1 VTRx (Optical transceiver)
- Power stage
  - Power up sequencer
  - DC/DC converter
    - 3 DC-DC converters @ 1.5V
    - 2 DC-DC converters @ 1.2V



- The nODE has 192 input channels that receive LVDS signals from the front-end electronics.
- Only optical interfaces - based on the **GBT** (GigaBit Transceiver) chipset and Versatile link components - are used to communicate with the data acquisition system, the Timing and Fast Control (**TFC**) framework and Experimental Control System (**ECS**).
- Each nSYNC communicates to its own GBTx chip, using an e-link data rate of 320 Mb/s, to transmit data to the DAQ system.
- An additional GBTx (the Master GBTx) is used to receive the master 40 MHz clock and the TFC commands (i.e. fast reset, synchronization signals ecc.) and to distribute them to the nSYNCs and to the other GBTx.
- Slow control and configuration of the board (i.e. configuration of GBTx and nSYNC chips, voltages monitoring ecc.) is managed by two GBT-SCA chips, that are interfaced with the Master GBTx, sharing the same TFC optical link to perform the slow communication, at 80 Mb/s.

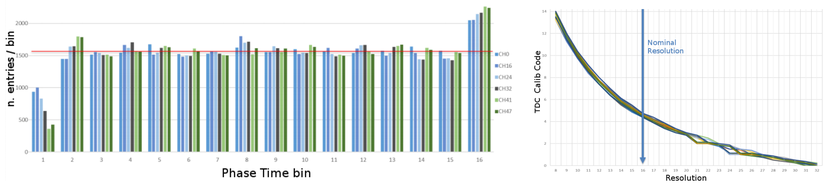
nSYNC test and results





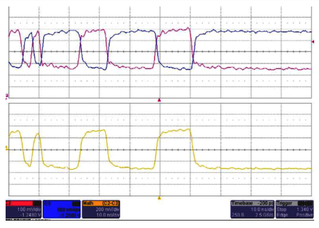
Various tests were performed on the nSYNC before the production phase. The test setup composed by a Logic Analyzer, a pattern generator (PGA), the **I²C** interface, the oscilloscope and the nSYNC test board, shown on the picture nearby.

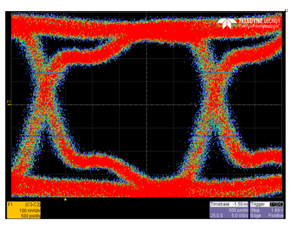
- **TDC calibration**: The TDCs, after automatic calibration procedure, show, for all resolution, the right code value. The channel uniformity is shown on the right plot.



- **TDC bin width** (plot on the left): to verify TDC bins uniformity 10 signals has been sent to each channel, every 10 ps using the pattern generator (synchronous with the 40 MHz master clock) scanning all the period (0 - 25ns). Wrong clock cycle and missing hits behaviours are compatible with results achieved from test on TDC prototype.

- **GBT Interface**: tested with the oscilloscope and Logic Analyzer; LVDS signals are compliant with standard specification and communication works as expected at 320 Mb/s .



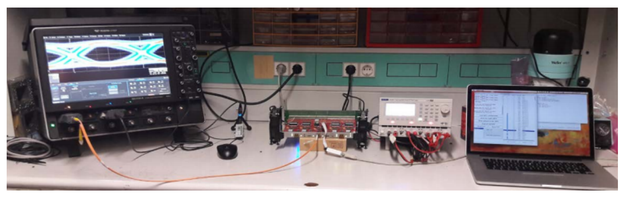


- **E-link eye diagram**: An eye diagram has been acquired sending a PRBS signal on GBT lines, triggering on input master clock. The well opend eye demonstrate the driver quality.
- **GBT Frame Test**. The nSYNC frame building capability in normal mode has been tested pulsing input channels. Verification of the nSYNC test features (fixed pattern and pseudo-random pattern) have been also succesfully performed, with LVDS channels uniform and words perfectly recognizable.
- **Slow Control/Fast commands**. All the procedures controlled via **I²C** (access configuration registers and "slow" commands) have been tested using custom LabVIEW routines. All fast commands are recevied correctely and act as expected.

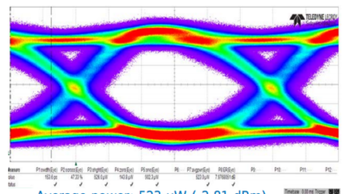
nODE test, results and readout chain test

Validation tests have been performed on Slow/Fast control of the board (Master GBTx local configuration, optical link, ECS/TFC interface) and data path (slave GBTx optical link, GBTx-nSYNC phase alignement, e-links characterization).

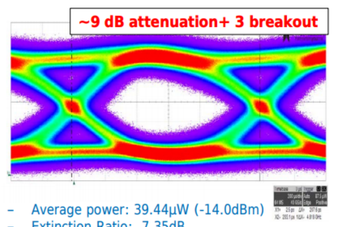
Experimental setup for link characterization: LeCROY SDA 816Zi-B (16 GHz Bandwidth, 40 GS/s, continuous acquired data stream of 200 μs at 40 GS/s), Optical to electrical converter (LeCroy mod.OE425).



- **Master GBTx Optical link**: tested with PRBS (pseudorandom binary sequence) produced internally by master GBTx. From a well opened diagram (image on the left) to still acceptable opening using 9dB attenuation and three breakouts on fibre (right). Similar results obtained for slave GBTx.

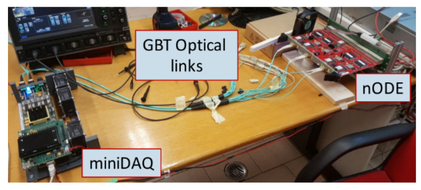


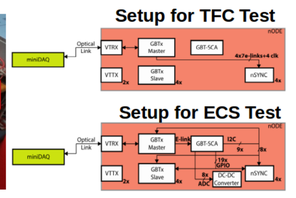
- Average power: 523 µW (-2.81 dBm)
- Extinction Ratio: 7.9 dB
- Eye opening ~50% @ BER<1E-16
- Total jitter ~ 110ps @ BER=1E-13

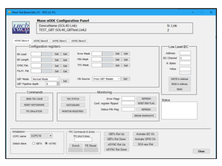


- Average power: 39.44µW (-14.0dBm)
- Extinction Ratio: 7.35dB
- Eye opening ~35% @ BER<1E-16
- Total jitter ~ 122ps @ BER=1E-13

- **TFC/ECS interface**: tested with miniDAQ (a complete emulation of the LHCb upgraded readout/control system). Used custom routines for nSYNC/GBTx control, configuration and monitor.

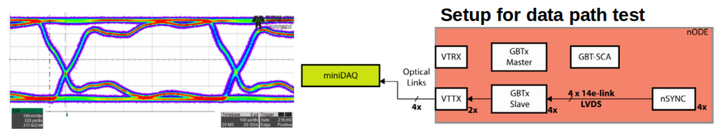






Each **I²C** bus tested performing 1024 read/write operations on each nSYNC and slave GBTx, with no errors. Tested the GPIO lines, in both I/O modes. ADC lines successfully used to monitor all power supply voltages. TFC commands continuously sent from miniDAQ to all nSYNCs for 2h: checked the number of sent/received commands and alignement of counters.

- **Data path**: custom PRBS checker module loaded in the miniDAQ firmware to check the nSYNC internal PRBS, on each of 14 e-links at 320 Mbps.



All 56 links tested for 64 hours without error (BER$< \mathbf{1 \cdot 10^{-13}}$). Also e-link eye diagram with probe on receiver side: well open diagram and compatible with the one obtained from the nSYNC test.

Future prospects

The production phase of nSYNC (around 1500 chips, spare included) has recently started. The next steps concern the test bench setup for post-production phase. In parallel the nODE production will start: the boards test will be based on similiar test done in validation phase, using miniDAQ v.2.

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