Performance of a high-throughput tracking processor implemented on Stratix-V FPGA

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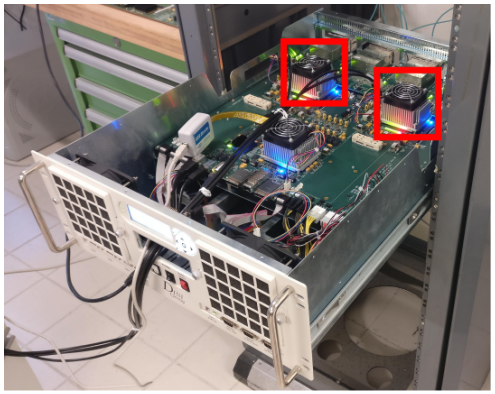
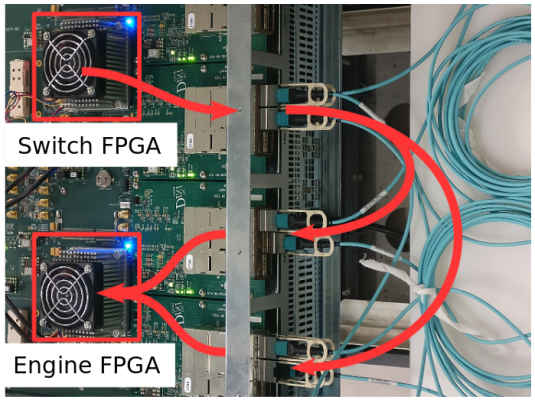
WHAT - The "Artificial Retina" tracking processor

- A **high speed, low latency** tracking processor
- Mathematically related to **“Hough transform”**
- Implemented on **FPGAs**
- **Highly-parallel** architecture
- Prototype with 2 FPGAs connected with **optical fibers**



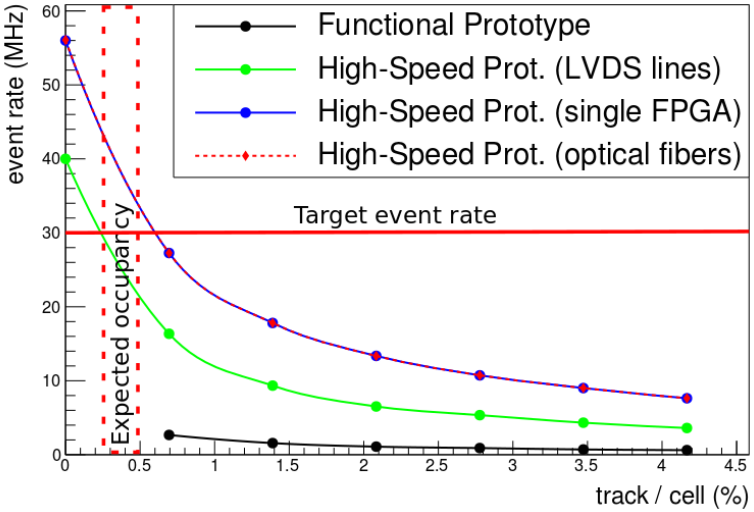


WHY - Tracking at very high rate

- Reconstruction of high quality tracks at beam crossing rate (30 MHz @ LHC)

PROTOTYPE RESULTS

- **High event rate** (> 30 MHz at expected occupancy)
- **Very low latency** (< 500 ns)



AUTHORS

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