Performance of a high-throughput tracking processor implemented on Stratix-V FPGA

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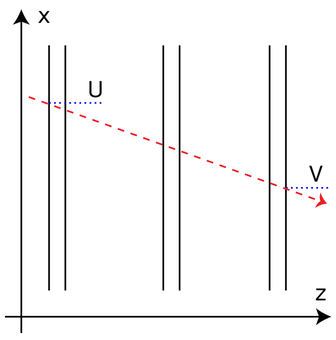
WHY - Tracking at very high rate

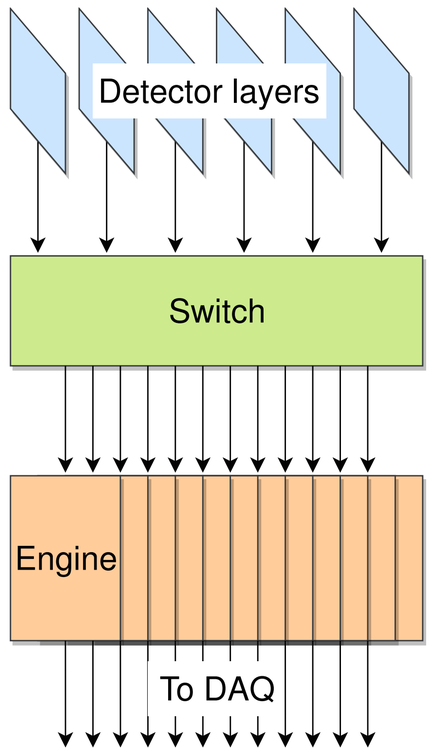
- In hadronic colliders at high luminosity (>10^{34} $cm^{-2}s^{-1}$) a heavy flavor particle will be produced at every beam crossing
- It is not possible to trigger events efficiently using simple parameters
- It is necessary to reconstruct high quality tracks at beam crossing rate (30 MHz @ LHC)

TRACKER CONFIGURATION[3]



- Generic tracker with 6 layers
- Single coordinate layers (x silicon strip)
- Layers grouped in 3 stations
- Track parameters: first and last layer coordinate
- Typical number of track @ LHCb SciFi: 200[4]
- Number of cells in the parameters space: 80k
- Occupancy (track/cell): 0.25%

HOW - The "Artificial Retina" Architecture[1]



- Mathematically related to **"Hough transform"**[2]
- Map tracks parameters space into an matrix of cells

Data flow from Detector

Custom **Switch** delivers hits only to appropriate cells

For each cell, the corresponding **Engine** performs a **weighted sum** of hits near the track trajectory

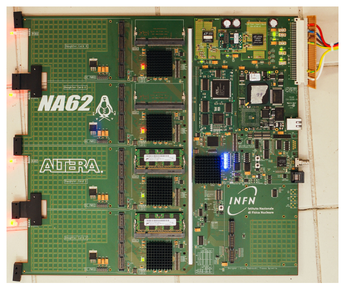
Parameters are obtained interpolating responses of nearby cells

Engines work in a fully parallel way

Track are forwarded to DAQ system

FUNCTIONAL PROTOTYPE

- 5 Altera Stratix III FPGA
- 200K LE per FPGA
- Maximum clock 350 MHz



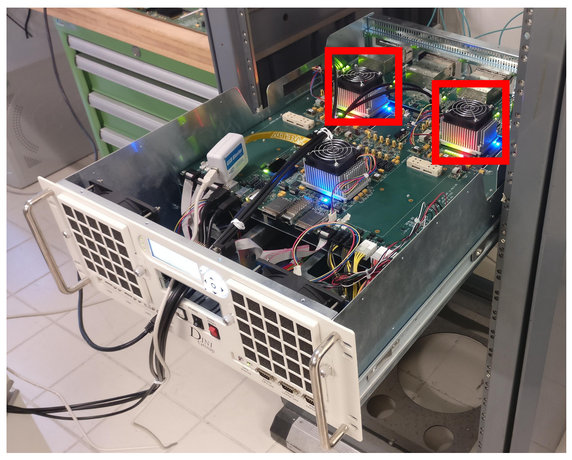
Two boards connected with LVDS lines

- Demonstrate system functionality

Switch board → LVDS → Engine board

HIGH-SPEED PROTOTYPE

- 2 Altera Stratix V FPGA
- 952K LE per FPGA
- Maximum clock 650 MHz
- 48 external 12.5 Gbps serial lines per FPGA



FPGAs connected with LVDS lines

- Test performances improvement after porting to newer FPGAs

Switch FPGA → LVDS → Engine FPGA

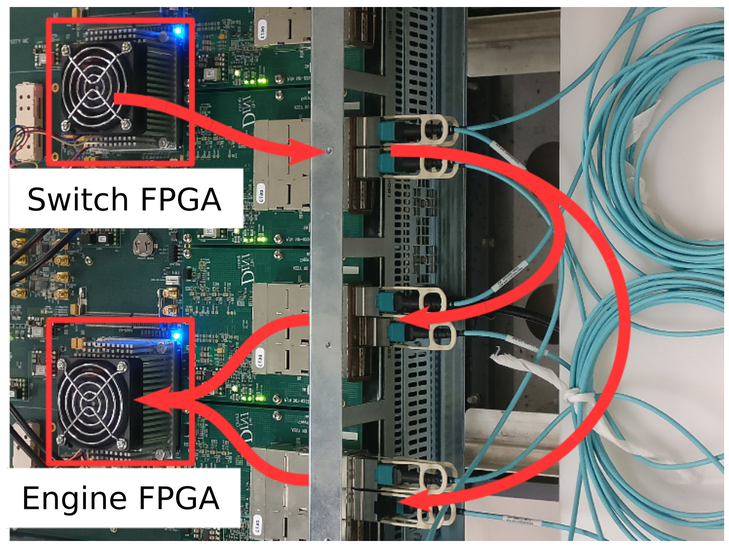
Single FPGA design

- Measure the maximum reachable event rate

Switch → Internal → Engine

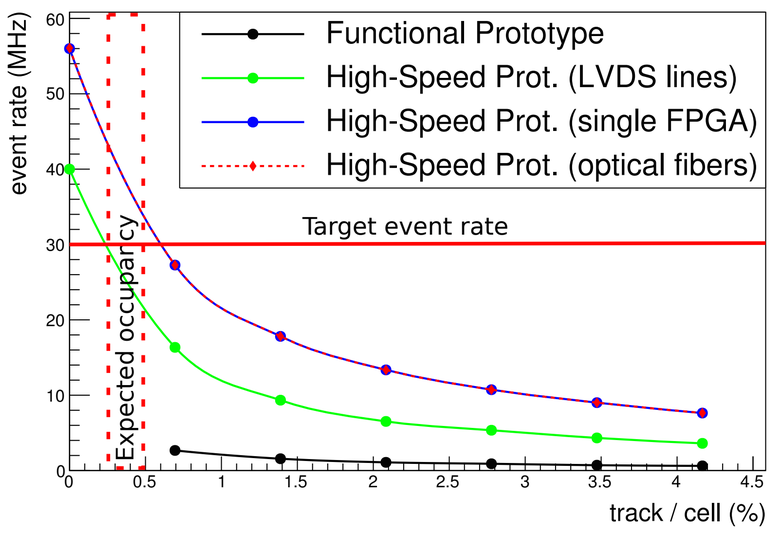
FPGAs connected with optical fibers

- Demonstrate the possibility of multi-board implementation

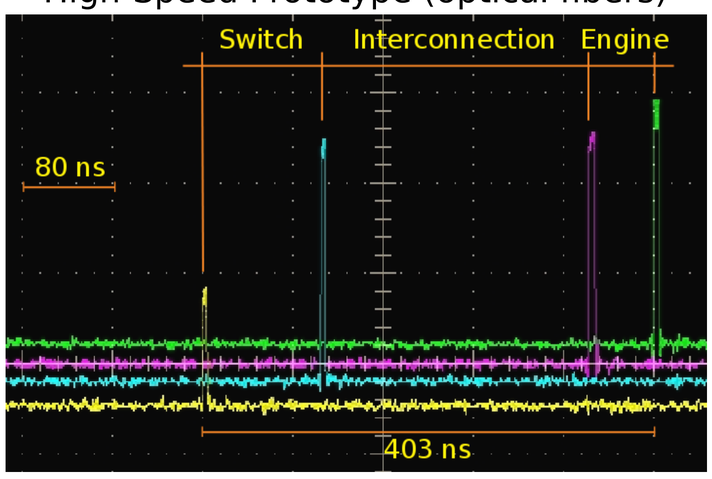


RESULTS

- **High event rate** > 30 MHz with occupancy < 0.5%[5]
- **Very low latency**, < 500 ns
- Multi-board implementation with optical fibers has the same event rate as single-device configuration
- This tracking processor has been included in the recent LHCb Expression of Interest for future upgrades presented to LHCC[6]



Latency measurement
High-Speed Prototype (optical fibers)



PROJECT DETAILS

Results achieved by "Retina", a 3-year project funded by INFN, Division of technological research experiments

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[1] A. Abba, F. Bedeschi, M. Citterio, F. Caponio, A. Cusimano, A. Geraci et al., *A specialized track processor for the LHCb upgrade, Tech. Rep. LHCb-PUB-2014-026, CERN, Geneva, Mar, 2014*

[2] P. Hough, *Machine analysis of Bubble Chamber Pictures, Proc. Int. Conf. High Energy Accelerators and Instrumentation* **C590914**, 1959

[3] R. Cenci, F. Bedeschi, P. Marino, M. Morello, D. Ninci, A. Piucci et al., *First Results of an "Artificial Retina" Processor Prototype, EPJ Web Conf.***127** (2016) 00005

[4] LHCb Collaboration, LHCb Tracker Upgrade Technical Design Report, CERN-LHCC-2014-001; LHCB-TDR-015

[5] R. Cenci, F. Lazzari, P. Marino, M.J. Morello, G. Punzi, L.F. Ristori, F. Spinella, S. Stracka, J. Walsh, *Development of a High-Throughput Tracking Processor on FPGA Boards, PoS(TWEPP-17)* **136**

[6] LHCb collaboration, *Expression of Interest for a Phase-II LHCb Upgrade: Opportunities in flavour physics, and beyond, in the HL-LHC era*, Tech. Rep. CERN-LHCC-2017-003, CERN, Geneva, Feb, 2017