Summary

Off-detector electronics in TDAQ systems of HEP experiments is often implemented by means of SRAM-based FPGAs, due their high-performance in real-time data processing and transfer. On-detector usage of FPGAs is mostly limited by their sensitivity to radiation induced upsets in the configuration (Fig. 1). In fact, these effects may disrupt the intended functionality and there is the need to correct, i.e. scrub, the configuration memory periodically.

In this work, we describe a simple yet effective scrubber core designed for Xilinx FPGAs based on configuration redundancy. The core does not require any external memory for hosting the golden configuration, yet the redundancy makes it possible to correct a significant number of upsets per frame. The scrubber is able to correct the configuration of a given design and its own.

2. Scrubber Architecture & Implementation

- Test firmware w/ benchmark design and scrubber (Fig. 5)
- Fully redundant configuration (Fig. 6)
- Scrubber w/ tiny logic footprint (nearly 500 slices in a 7-Series FPGA)
- Based on Xilinx PicoBlaze & ICAP
- Supports correction of the full device
- No custom design flow needed
- Portable on most Xilinx devices
- Provides detailed information about detected upsets (FRAD, offset, timestamp, polarity)

3. Proton Beam Test

- Test with a 62-MeV proton beam at Superconducting Cyclotron at Laboratori Nazionali del Sud – Catania, Italy (Fig. 7)
- Total fluence 6.7×10⁵ cm⁻², 110 runs, flux between 2.2×10⁹ cm⁻² s⁻¹ and 3.5×10⁹ cm⁻² s⁻¹
- Custom DUT board FPGA loaded with test firmware (Fig. 8)
- Tester board (Xilinx KC705) runs same benchmark circuit as DUT and it verifies DUT output
- Multichannel Power Analyzer (PA) powers DUT board
- Test controller logs upsets from scrubber, functionality test results from test board, and power logs for PA
- Remote PC accesses test controller from control room

4. Test Results

The scrubber has been proven to
- Repair the configuration (any number of upsets per frame) (Fig. 9 and 10)
- Keep the power consumption stable within few mA at any power input of the FPGA
- Improve the mean absorbed proton fluence before a persistent failure of a benchmark design by 42% (benchmark w/ TMR) and 290% (benchmark w/o TMR) (Fig. 11)

References