DESIGN OF THE ATLAS PHASE-II HARDWARE-BASED TRACKING PROCESSOR

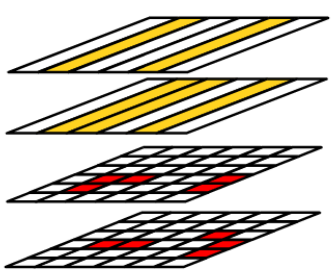
GOAL

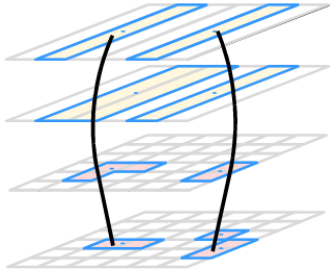
High-luminosity LHC
- Peak luminosity
  - 7.5×10^{34} cm^{-2} s^{-1}
- ATLAS experiment will increase early stage trigger selection power

Hardware-based tracking for the trigger (HTT)
- A combination of
  - Associative Memory ASICs
  - FPGAs
- Provide the software-based trigger system with access to tracking information

Physics Goals
- Allow for reduced pT trigger thresholds
  - Primary lepton selections
- Contribute to pile-up mitigation
  - Essential for hadronic signatures

KEY POINTS

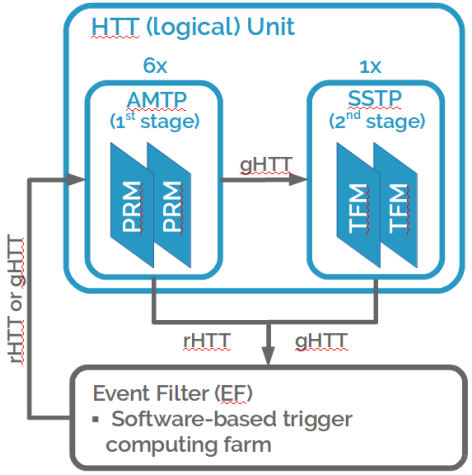




Track Reconstruction
- Pixel and strip detectors
- Cluster aggregation
- Pattern matching and track fitting

Regional tracking
- Hits from 8 outermost ITk layers
- Only 1st stage

Global tracking
- Full ITk coverage
- Two stages



ABOUT ME

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On behalf of the ATLAS Collaboration