DESIGN OF THE ATLAS PHASE-II HARDWARE-BASED TRACKING PROCESSOR

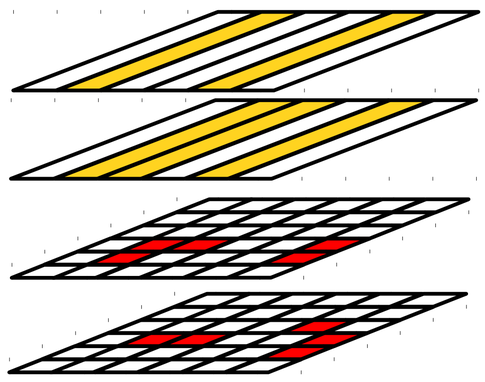
XIV Pisa Meeting on Advanced Detectors – La Biodola, Isola d'Elba (Italy), 27 May - 2 Jun 2018

GOAL

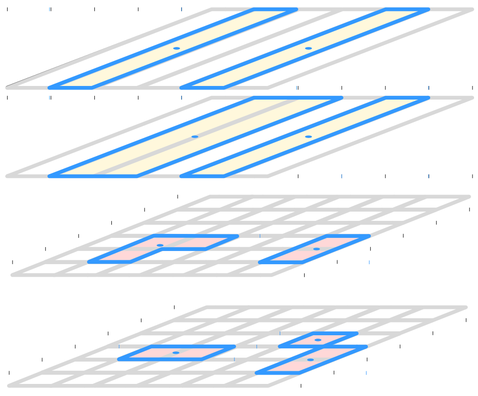
The expected increase in peak luminosity of 7.5×10^{34} cm^{-2} s^{-1} of the upgraded high-luminosity LHC will force the ATLAS experiment to increase early stage trigger selection power. The agreed strategy is to implement precise hardware track reconstruction. The **hardware-based tracking for the trigger (HTT)** will use a combination of Associative Memory ASICs and FPGAs to provide the software-based trigger system with access to tracking information, allowing for reduced p_T trigger thresholds for primary lepton selections, while contributing to pile-up mitigation, essential for hadronic signatures.

KEY POINTS

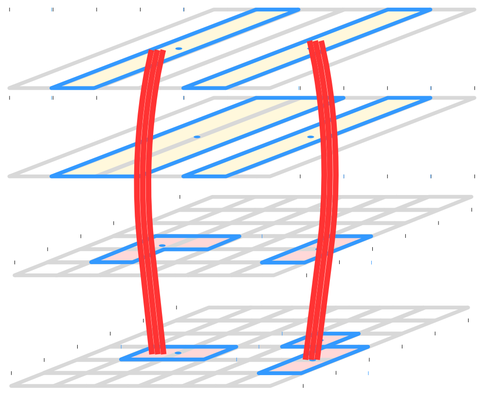
HARDWARE TRACK RECONSTRUCTION



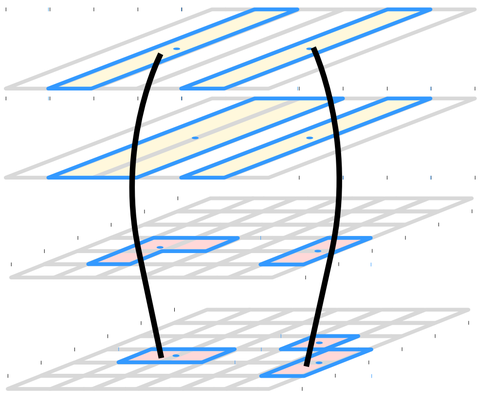
Hits in the Inner Tracker
- Pixels detector layers
- Strip detector layers



Clustering
- All clusters are aggregated and sent for processing



Associative Memory
- Pattern matching
- Identify track candidates



FPGA
- Track fitting (χ^2)
- Track parameters (d_0, etc)

DESIGN

THE HTT SYSTEM

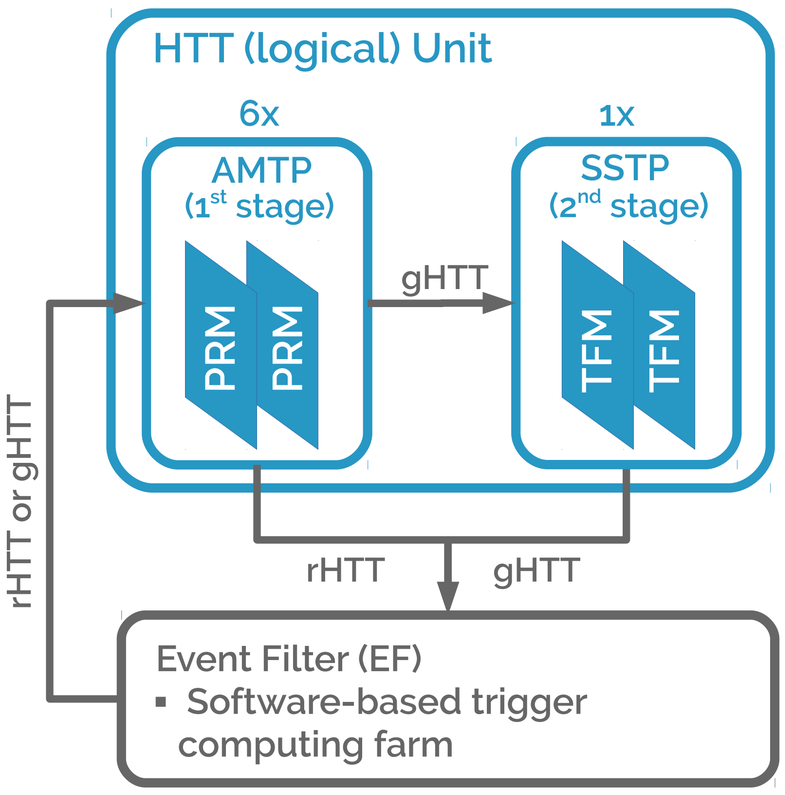
Regional tracking (rHTT)
- Hits from 8 outermost ITk layers
- Tracks with $p_T > 2$ GeV
- Request rate of 1 MHz
- Only 1st stage processing

Global tracking (gHTT)
- Full Inner Tracker coverage
- Tracks with $p_T > 1$ GeV
- Request rate of 100 kHz
- Two stage processing

HTT to EF Interface
- Based on FELIX cards
- Optical links (120 Gb/s)

1st stage – AM Tracking Processors (AMTP)
- Housing two *Pattern Recognition Mezzanine* (PRM) cards
- Hit clustering and data organisation
- Uses *Associative Memories* (AMs) for pattern matching
- Track fitting performed in FPGAs

2nd stage – Second Stage Tracking Processors (SSTP)
- Housing two *Track Fitting Mezzanine* (TFM) cards
- Hit clustering in new layers
- Track extraction and re-fitting performed in FPGAs

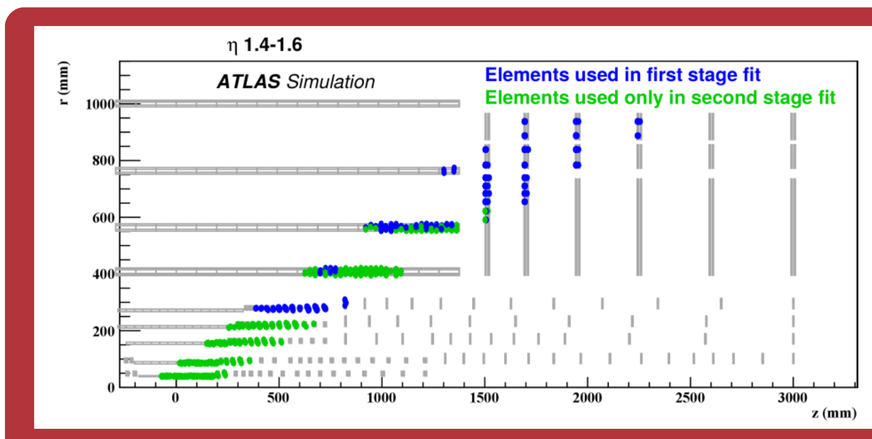


SIMULATION

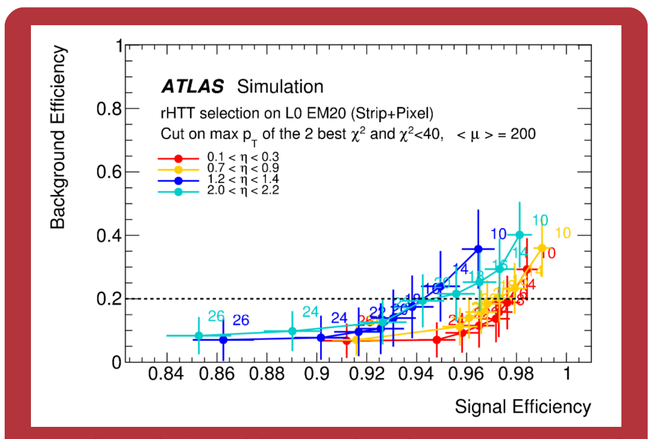
TRACKING CAPABILITY

Choice of # layers affects:
- Number of patterns required
- Number of false matches
- Resolution of the fitted tracks

Regional Tracking Performance
- Electron case
- Single electron signal sample overlaid with minimum bias
- Factor ~5 background rejection for ~95% signal efficiency



Inner Tracker (ITk) Layers used for 1st and 2nd stage fitting corresponding to the 1.4-1.6 eta region.



Regional tracking rejection on top of calo-only electrons ($p_T > 20$ GeV). Track p_T threshold indicated next to the lines.

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