First test results of the CHIPIX65 asynchronous front-end connected to a 3D sensor

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Introduction

FUTURE pixel readout chips at the CERN High-Luminosity LHC (HL-LHC) will be exposed to extremely high levels of radiation and particle rates. In the future upgrades, the main experiments will need completely new tracker detectors, complying with the very demanding operating conditions and the delivered luminosity. The pixel ASIC designer community identified the 65 nm CMOS technology as the candidate technology for the development of new generation readout chips at the HL-LHC. Such a technology allows the designer to integrate very dense in-pixel analog and digital functions, crucial when operating with hit rate of the order of some GHz/cm.

A low noise, asynchronous front-end has been designed and integrated in a small scale demonstrator, also integrating a synchronous architecture, in the framework of the CHIPIX65 project, funded by the INFN. The demonstrator has been bump-bonded at SLAC with 3D pixel sensors developed by FBK.

In this work, the design and experimental characterization of the asynchronous architecture is reported.

CHIPIX65 demonstrator

Features:

- 64 x 64 pixels with 50 µm pitch
- two different, synchronous and asynchronous, analog front-end architectures working in parallel (two 32x64 submatrices) interfacing with a common digital readout and configuration scheme
- A novel digital architecture
- On-chip bias network and monitoring
- Chip configuration based on SPI protocol
- Usage of CERN I/O library

Design flow:

- Digital-On-Top chip assembly
- Top-down hierarchical flow
- Pixel matrix composed of 16x16 pixel regions
- A pixel region contains the digital architecture and the analog FE

Asynchronous Analog Front-end

- Single amplification stage for minimum power dissipation
- Krummenacher feedback to comply with the expected large increase in the detector leakage current
- High speed, low power current comparator
- Relatively slow ToT clock ~ 80 MHz
- 5 bit counter – 400 ns maximum time over threshold
- 30000 electron maximum input charge, ~450 mV preamplifier output dynamic range
- Selectable gain and recovery current
- Overall current consumption: ~4 µA

Test results of sensorless front-end

- All pixels tested and fully working. Front end can be operated at 600 e- threshold
- ~50 e RMS trimmed threshold dispersion, ENC=100 e RMS
- Per-pixel DAC codes extracted from untrimmed S-curves using a set of 800 macro's and then loaded into the chip
- Very good linearity for the 5-bit ToT for input charge larger than ~2000 e

Results for the bump-bonded chip

- Bump-bonding performed at SLAC with FBK 3D pixel sensors
- Sample prototypes coupled to both 50 µm x 50 µm and 25 µm x 100 µm sensors
- Results shown in this work are for the 50 µm x 50 µm sensor

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