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A low cost, high speed, Multichannel Analog to Digital converter board

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Abstract

We developed a highly configurable digitizer board including 12 complete acquisition channels: the board analog to digital converters (ADC) components can be chosen to tailor the specific application, ranging from 12 bit 65 MHz up to 14 bit 250 MHz.
In this application the front-end circuit is dedicated to the Silicon Photomultipliers (SiPM) of the BDX detector.
The control is made by a commercial FPGA module to guarantee the scalabilty of the system.
Having the possibility to choose the ADC and the "size" of the FPGA on the control module the price can be reduced to the minimum for a given application.
The board permit the time synchronization using various methods including GPS and White Rabbit.
The configurability of the board and the various options implemented permit to use it in a triggerless data acquisition system.
Up to 240 channels can be hosted in a single 6U crate.

DETAILED DESCRIPTION

FRONT-END

The front-end sensors (SiPM) are connected to the board through coaxial cables and MCX connectors; the analog signal can be amplified by two fixed gain values, 4 or 80. Each front-end sensor can be powered by the board itself with a High Voltage (HV) up to 100 V. The HV can be sourced either from an onboard step-up DC/DC converter or using an external power supply. Then each channel has a dedicated HV regulator for a fine tuning dependant on the specific sensor. The HV feed can be completely disconnected from the input path removing a resistor to increase noise immunity.
The offset of the analog signal can be set using a DAC, which spans the whole ADC input range. Thanks to this feature, sampling both positive and negative signals is possible.
The digitizer is a dual true differential ADC from Texas Instruments; the ADC family members are pin to pin compatible and allow a resolution of 12 or 14 bit and sampling frequencies of 65, 125, 160, and 250 MHz, depending on the family member chosen. Selecting the proper ADC during the production phase makes a big change in price, since the cost of the device scales of one order of magnitude from the 12 bit@65 MHz to the 14 bit@250 MHz.

TIMING

The board has two UFL connectors in order to receive on a coaxial cable both a clock and a timing signal, typically produced by a GPS receiver, and used to align the system to a common reference. The clock is a single-ended signal whose electrical levels can be adjusted with a resistive partition. The timing signal is fed directly to the FPGA and can be either a slow reference (e.g. a Pulse Per Second (PPS) signal) or a digital timing protocol (e.g. NMEA or IRIG). This signal is used to impose the same clock phase to all the boards in the system: this feature is required by the needs to timestamp the sampled signal in a coherent way all over the detector.
To meet the performance required by sampling frequency and ADC resolution, a Phase Locked Loop (PLL) device is used to eventually multiply the input clock, to reduce the input clock jitter, and to distribute it to each ADC and to the FPGA. The PLL is accounted of a 0.4 ps of total output jitter.
A White Rabbit interface is also present, as an alternative way to distribute timing over a fiber link still allowing data exchange on Ethernet protocol on the same medium.
The board has two output connectors which, in turn, can be used to drive a clock and a timing reference signal: adjacent boards can be setup in a daisy chain configuration scheme to easy timing distribution reducing cabling burden.

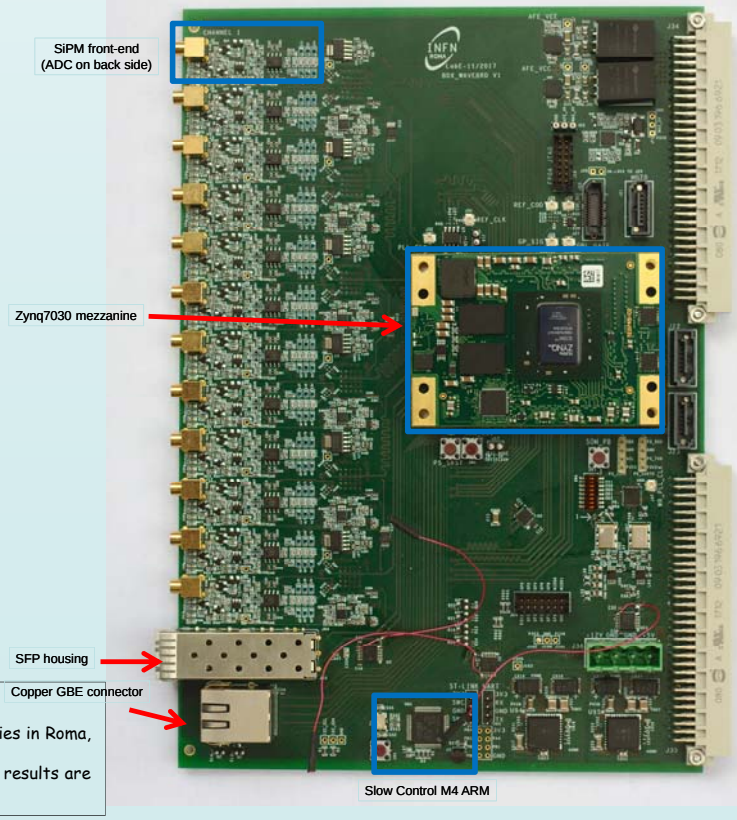
BOARD CONTROL

Data collection and manipulation is accomplished by a commercial System-on-Module (SoM) mezzanine board, based on a Zynq7030 FPGA, from Trenz Electronics. The SoM equips the board with DDR3 memory, Flash memory, SD card, high-performance interfaces (GbE, USB 2.0, MGT transceivers), slow communication peripherals (e.g. I^2C, RS232). Connectors (e.g. micro USB, RJ45) are provided on the main board while PHYs are on the SoM.
Depending on project needs (i.e. computing power required and logic size), the same SoM can be purchased with three different Zynq devices: 7030, 7040, and 7045. This choice, again, makes big difference in price. A custom mezzanine module could be in principle built around a simpler and cheaper FPGA, if the project is less demanding in terms of processing power.
The control of the many DACs, ADCs, HV regulators, is implemented by a M4 ARM processor, which communicates through a RS232 with the Zynq and behaves as a low-level driver of the board. Even without the SoM, the board can be tested and debugged in many aspects of its functionalities.
One of the FPGA MGTs is used for SFP laser interface, three are individually connected to SATA connectors to implement a daisy-chain architecture between adjacent boards; for bigger FPGAs, the remaining 4 MGTs are connected to a high speed SAMTEC board-to-cable connector for future expansions.
The board form factor is 6U VME B-size and mounts J1 and J2 standard VME connectors; power can be supplied using either J1/J2 connectors or a 4-pin connector. Required voltages are +5 V and +12 V, with a power consumption of, respectively, 3 A and 0.5 A.

SUMMARY

In the framework of the Beam Dump eXperiment (BDX) at Jefferson Laboratory (Jlab) we developed a highly configurable digitizer board.
The board includes 12 complete acquisition channels dedicated to SiPM readout.
The SiPM bias voltage is also generated and regulated on channel basis on board.
The ADC can be tailored for different applications ranging form 12 bit 65 MHz up to 14 bit 250 MHz.
The front end is now dedicated to the SiPM for the BDX CsI(Ti) crystal calorimeter, but can be easily reimplemented for different detectors, having fixed the backend structure hence saving a lot of time in the new development.
The board is controlled using a commercial FPGA module hosting a Xilinx Zynq device and all related peripherals, mainly memory and communication interfaces.
The board has been thought to be used in a triggerless system: all data passing some programmable selection criteria are sent out to a computing farm using gigabit Ethernet standard. To be effective, this methods need to guarantee a good timing synchronization between all the boards: we foresee various approaches. The entire data acquisition system can be synchronized using GPS standard protocols (like NMEA or IRIG) or using the more sophisticated White Rabbit system.
One of the design target was to minimize the channel cost: we can have a very competitive product compared with commercial devices, noting that here the front-end is included on-board.

WaveBoard first prototype



CONCLUSIONS

The system has been prototyped and now the boards are under extensive testing in 3 laboratories in Roma, Bologna and Genova.
All low level tests have been passed and now we are focusing on data conversion handling: first results are encouraging showing a channel noise in the order of 1.5-2 LSB (RMS)