Low Latency serial communication for MEG II Trigger system

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The WaveDAQ: Trigger and Data Acquisition System

A new custom-designed integrated Trigger and Data Acquisition System (TDAQ) \cite{1} is being developed to cope with the increased number of channel of the MEG II upgrade \cite{2}. Trigger serial connection constitute the backbone of the whole system.

Digitizer cards: WaveDREAM2

The WaveDREAM2 Board hosts two Domino Ring Sampler 4 (DRS4), and requires a very fast trigger (~500ns) to be operated at 2 GSPS sampling speed.

These boards also act as trigger frontend digitizing signals at 80 MHz and doing first-level trigger processing in the onboard Xilinx Spartan6 FPGA.

The Trigger Tree

Trigger informations are processed by custom designed Xilinx Kintex7 FPGA boards arranged in a 3-layer tree structure.

The first layer performs a 16:1 merging, the second a 4:1 and the last one a 1:6:1 merging to than generate the trigger signal.

The Xilinx SerDes primitive

Each serial connection is composed by eight 8:1 serializer blocks available in FPGA input banks \cite{3}, for a total bandwidth of 64 bit each clock cycle.

To establish a stable connection a programmable input delay is used and an additional gearbox of the data is also provided.

Total transmission latency is 3 clock ticks in addition to the track length.

Prototype system

Small 2-6 crate TDAQ systems have been assembled and operated over the last year. They consist of few WaveDREAM2 Crates also including the first layer of the trigger tree and a Trigger Crate housing the last two layers, connected to the first one by means of 5 m long Serial Trigger Cables made by FCI. Other cables distribute trigger and clock from the Ancillary system to the WaveDREAM2 crates.

An automatic calibration FSM

Having to calibrate thousand of serial links, we implemented a dedicated Finite State Machine to select the appropriate control signals for a stable transmission.

Each links sends a “0xAX” pattern where X counts from 0x0 up to 0xF, so that the fixed part can be used for delay adjustment while the variable part is used for latency monitoring and automatic compensation.

The MEG II Experiment

The MEG II \cite{1} goal is to reach a sensitivity of 6 \times 10^{-14} on the $\mu \rightarrow e\gamma$ branching fraction, a factor 10 better than MEG: the newly design positron spectrometer will consist in a low-radiation length drift chamber coupled to plastic scintillator tiles for fast timing. The MEG photon detector will also be improved by substituting the former PMTs on the inner face with silicon-based MPPCs.

The upgrade is designed to increase by ~2 the resolution on all observables while having an higher segmentation to help coping with higher rates from an increased muon stopping rate.

Bibliography

[1] L. Galli poster at this conference
[4] K. Satoru poster at this conference

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