Low Latency serial communication for MEG II Trigger system

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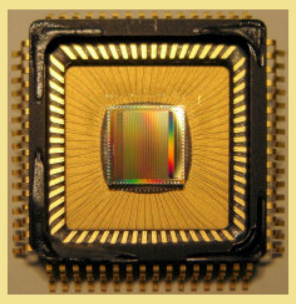
The WaveDAQ: Trigger and Data Acquisition System

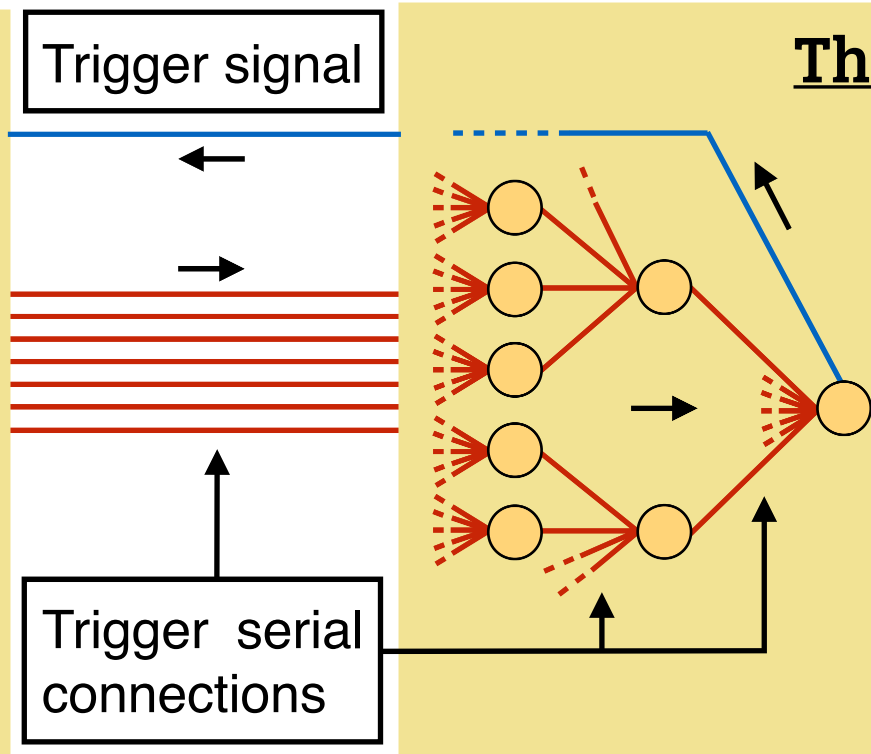
A new **custom-designed** integrated Trigger and Data Acquisition System (TDAQ) [1] is being developed to cope with the increased number of channel of the **MEG II upgrade** [2]. Trigger serial connection constitute the **backbone** of the whole system.

Digitizer cards: WaveDREAM2

The WaveDREAM2 Board hosts two **Domino Ring Sampler** 4 (DRS4), and requires a very **fast trigger** (~500ns) to be operated at 2 GSPS sampling speed.



These boards also act as **trigger frontend** digitizing signals at 80 MHz and doing **first-level trigger processing** in the onboard Xilinx Spartan6 FPGA.



The Trigger Tree

Trigger informations are processed by custom designed **Xilinx Kintex7 FPGA** boards arranged in a **3-layer tree structure**.

The first layer performs a 16:1 merging, the second a 4:1 and the last one a 16:1 merging to than generate the trigger signal.

Ancillary System: Clock Distribution

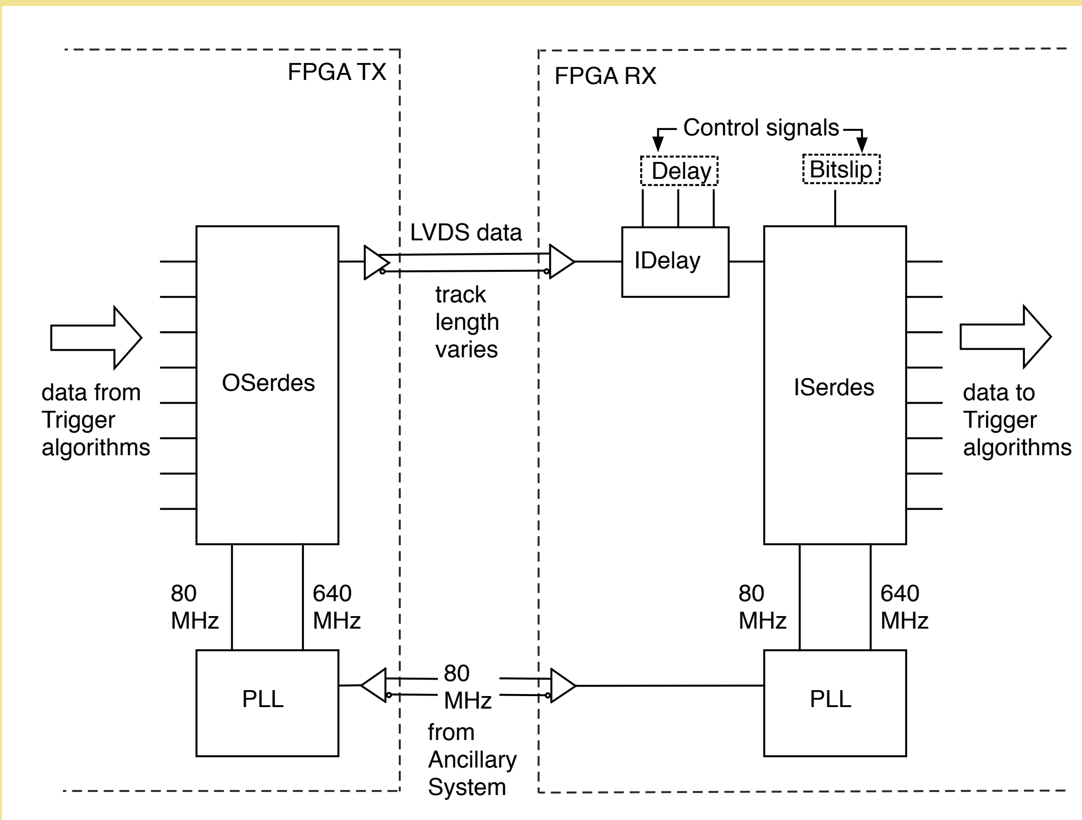
The Ancillary system performs the fanout of the trigger signals and distributes the system clock with a design jitter **less than 10ps** to be used for DRS4 sampling and for serial transmission.

The Xilinx SerDes primitive

Each serial connection is composed by **eight 8:1 serializer** blocks available in FPGA input banks [3], for a total bandwidth of **64 bit each clock cycle**.

To establish a stable connection a **programmable input delay** is used and an additional **gearbox** of the data is also provided.

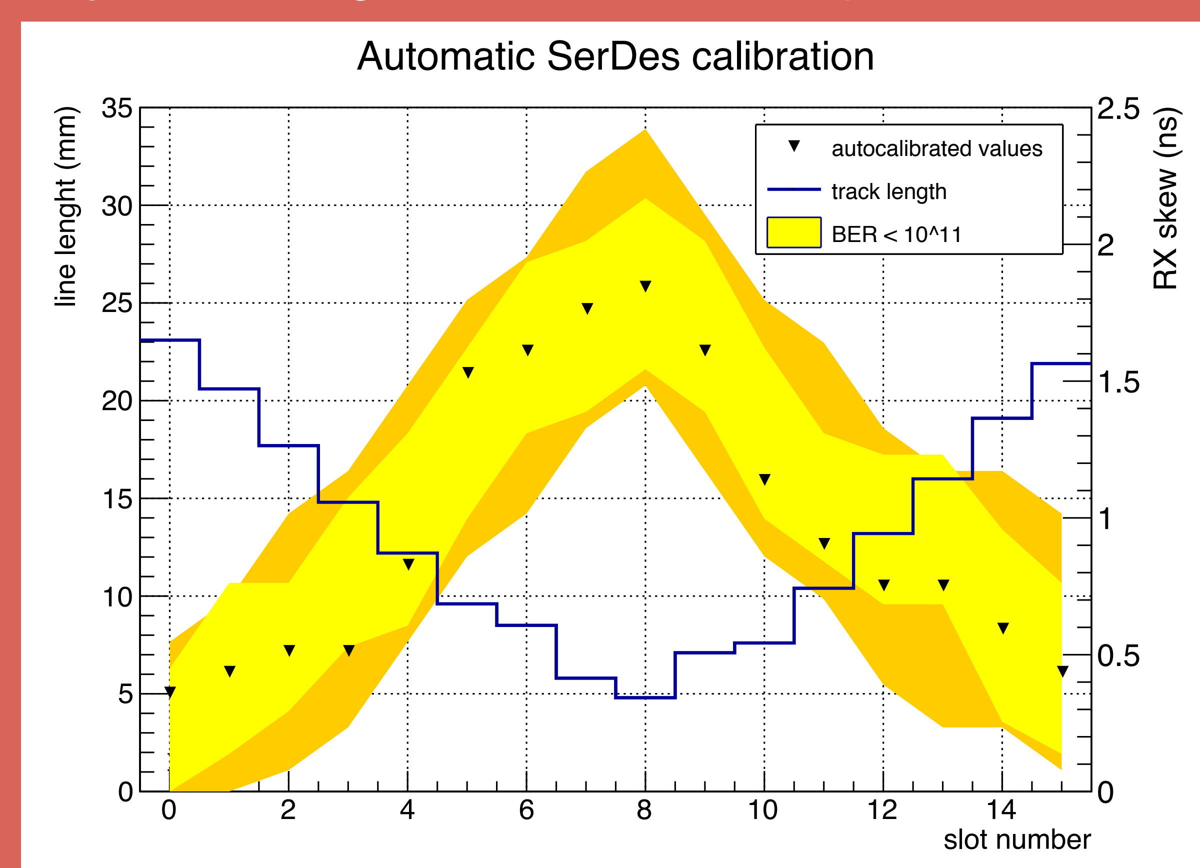
Total transmission latency is **3 clock ticks** in addition to the track length.



An automatic calibration FSM

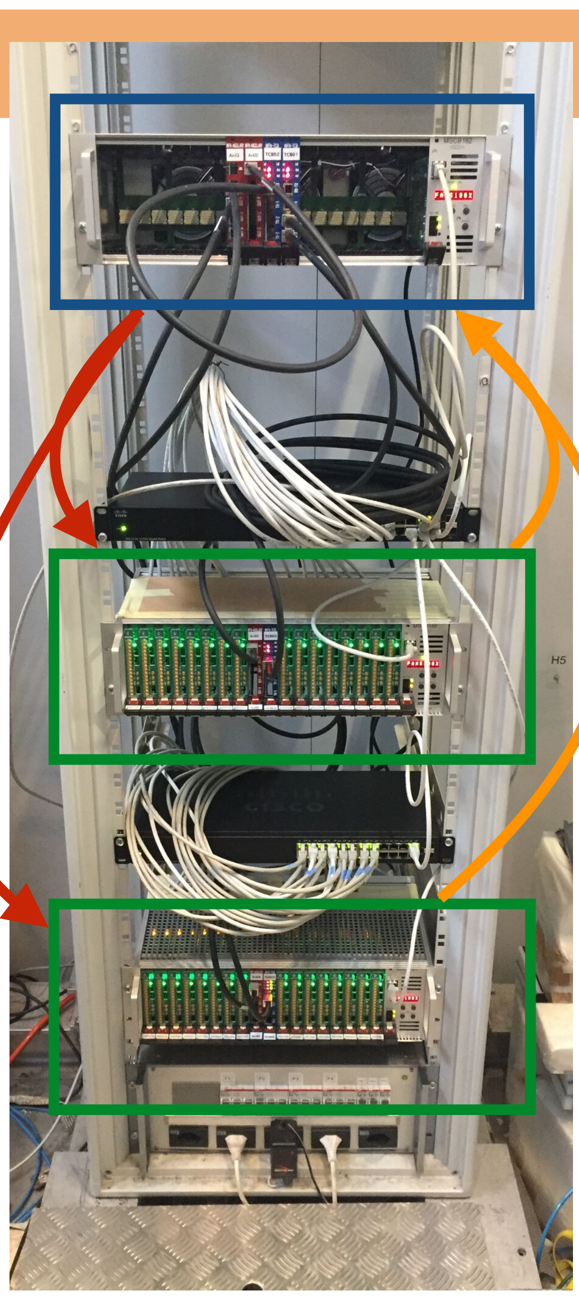
Having to calibrate **thousand of serial links**, we implemented a dedicated **Finite State Machine** to select the appropriate control signals for a stable transmission.

Each links sends a "0xAX" **pattern** where X counts from 0x0 up to 0xF, so that the **fixed part** can be used for delay adjustment while the **variable part** is used for latency monitoring and automatic compensation.

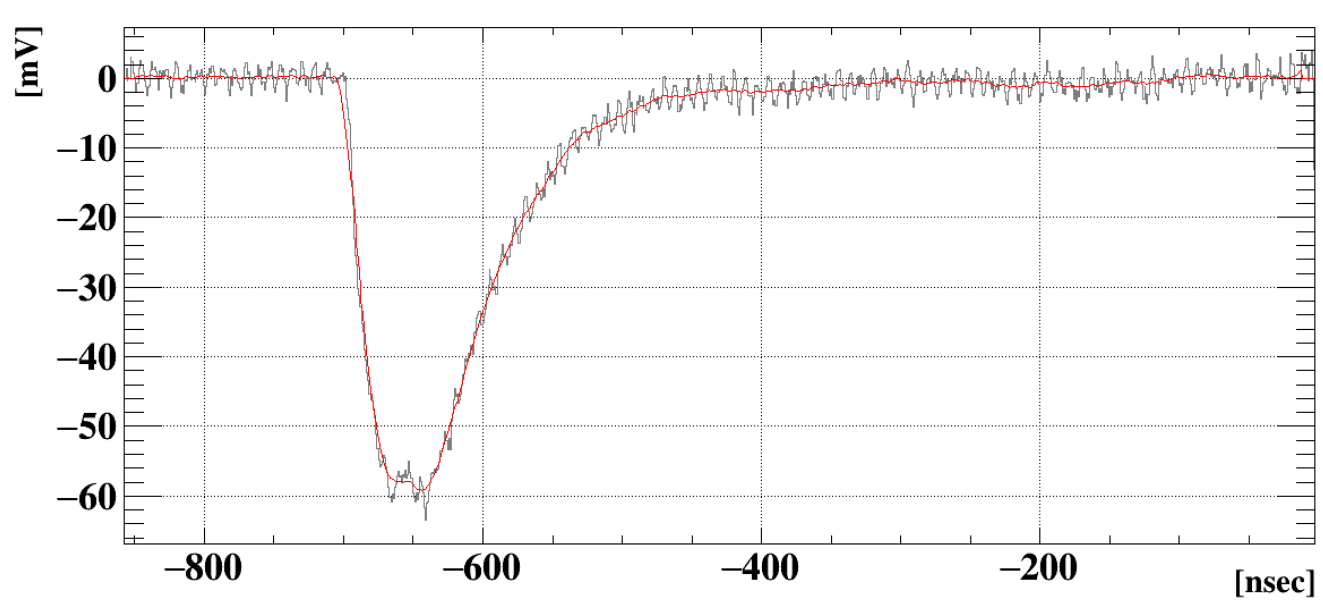


The calibrated delay values anti correlate well with backplane track length. The Bit Error Rate contour is shown in yellow for comparison.

Prototype system



Small 2-6 crate TDAQ systems have been **assembled and operated** over the last year. They consist of few **WaveDREAM2 Crates** also including the first layer of the trigger tree and a **Trigger Crate** housing the last two layers, connected to the first one by means of 5 m long **Serial Trigger Cables** made by FCI. Other **cables** distribute trigger and clock from the Ancillary system to the WaveDREAM2 crates.



A system of 4 crates has been tested by connecting WaveDREAM2s to the **MEG II Liquid Xenon Detector** [4]. **Total trigger latency** can be easily measured to be **700 ns** by trigger position in DRS4 w.r.t. the signal pulse.

Total waveform summing and trigger generation through the 3-layered trigger tree happens in 56 clock ticks out of which **14 clock ticks are due to trigger data transmission including track length**.

The MEG II Experiment

The MEG II [1] goal is to reach a **sensitivity of 6 10^{-14}** on the **$\mu \rightarrow e\gamma$ branching fraction**, a factor 10 better than MEG: the newly design **positron spectrometer** will consist in a low-radiation length **drift chamber** coupled to **plastic scintillator tiles** for fast timing. The MEG photon detector will also be improved by substituting the former PMTs on the inner face with **silicon-based MPPCs**.

The upgrade is designed to **increase by ~2 the resolution** on all observables while having an higher segmentation to help coping with higher rates from an **increased muon stopping rate**.

Bibliography

[1] L. Galli poster at this conference
[2] Eur. Phys. J. C (2018) 78:38
[3] Full documentation at https://www.xilinx.com
[4] K. Satoru poster at this conference

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